



HAL
open science

Rigorous extraction tunability of Si-integrated Ba_{0.3}Sr_{0.7}TiO₃ thin film up to 60 GHz

Freddy Ponchel, Jean-François Legier, Caroline Soyer, Denis Remiens, Jean Midy, Tuami Lasri, Guillaume Guégan

► **To cite this version:**

Freddy Ponchel, Jean-François Legier, Caroline Soyer, Denis Remiens, Jean Midy, et al.. Rigorous extraction tunability of Si-integrated Ba_{0.3}Sr_{0.7}TiO₃ thin film up to 60 GHz. Applied Physics Letters, 2010, 96, pp.252906-1-3. 10.1063/1.3454772 . hal-00549520

HAL Id: hal-00549520

<https://hal.science/hal-00549520v1>

Submitted on 22 Nov 2021

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Rigorous extraction tunability of Si-integrated $\text{Ba}_{0.3}\text{Sr}_{0.7}\text{TiO}_3$ thin film up to 60 GHz

Freddy Ponchel,^{1,a)} Jean-François Legier,² Caroline Soyer,² Denis Rémiens,² Jean Midy,¹ Tuami Lasri,² and Guillaume Guéguan¹

¹ST Microelectronics, SAS 16, rue Pierre et Marie Curie, 37071 Tours, France

²Institute of Electronics, Microelectronics, and Nanotechnology (IEMN), UMR CNRS 8520, Université des Sciences et Technologies de Lille, 59652 Villeneuve d'Ascq Cedex, France

(Received 8 February 2010; accepted 25 May 2010; published online 23 June 2010)

400-nm-thick $\text{Ba}_{0.3}\text{Sr}_{0.7}\text{TiO}_3$ thin films are deposited on high resistivity silicon by *in situ* radio frequency magnetron sputtering. Coplanar waveguides with 1 μm slot width are designed, with accurate knowledge frequency losses behavior, to determine ferroelectric thin-films properties up to 60 GHz. Permittivity, loss tangent, and tunability are extracted through measurements and home made finite element analysis. Tunability of 33% and 29%, with 30 V maximum applied voltage (electric field of 300 kV/cm), are measured at 5 GHz and 60 GHz, respectively, while the dielectric losses evolve from 0.5% to 5%. A brief highlight is proposed about tunable silicon integrated quarter wavelength transformer potentialities for impedance matching. © 2010 American Institute of Physics. [doi:10.1063/1.3454772]

Advances in perovskite oxides $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$ (BST) thin-film growth techniques have stimulated important attention because of the very interesting physical properties of this kind of materials for applications, such as dielectrics in semiconductor memories and dielectrics in frequency agile devices.¹⁻³ However, the growth of BST films with good crystallinity directly onto high resistivity silicon (hrSi) substrate, for the development of silicon integrated circuits, poses a formidable challenge because of inherent incompatibility of the two materials. Introducing a seeding layer has been identified as one of the best ways to fabricate BST films on silicon with significantly enhanced crystallization properties.⁴ A complete microwave characterization of BST films, i.e., permittivity, tunability, and associated losses up to 60 GHz is reported. We use original codes based on vector finite element method and proper de-embedding software to determine these properties from scattering parameters ($[S]$ matrix) measurements. The design of specific micro coplanar waveguides (MCPWs) (with slot width of 1 μm) is developed thanks to a previous characterization of similar BST film.⁵

The $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$ films, with $x=0.3$, are deposited on hrSi substrates. $\text{Ba}_{0.3}\text{Sr}_{0.7}\text{TiO}_3$ presents a good compromise between high dielectric constant, low loss, and high accordability.⁶ The films are grown *in situ* by radio frequency magnetron sputtering. As the BST is deposited directly onto silicon, the crystallization is poor even at high substrate temperature. Typical x-ray diffraction is presented Fig. 1 (gray line) for films deposited at 700 °C. To get better film properties, we can use a buffer layer in order to control the film orientation and to improve the film crystallization.^{7,8} The thickness of the buffer layer is an important parameter regarding the electrical properties. If the thickness is too important, a degradation of the electrical performances is currently observed. We decide in this work to deposit first a very thin layer of BST of the same composition as the “active” film but this layer is deposited at higher growth temperature

than the “active” film. Typically, this layer (100 nm thick) is deposited at 800 °C (this high temperature is necessary to initiate the crystallization) while the “active” layer is identically sputtered as the previous conditions but the growth temperature is set to 700 °C. The “total” film thickness (buffer +active layers) is in the order of 0.4 μm . Figure 1 (black line) shows the x-ray diffraction of BST film with the buffer layer. It demonstrates that the film is polycrystalline without a preferred orientation, pure perovskite phase is observed, i.e., no second phase is noticed.

This study outlines the tunability behavior of this 400-nm-thick BST film up to 60 GHz at room temperature. For tunability evaluation, it is necessary to apply a large electric field (a few hundreds of kilovolt per centimeter) in order to observe the change in the permittivity. In this context, we

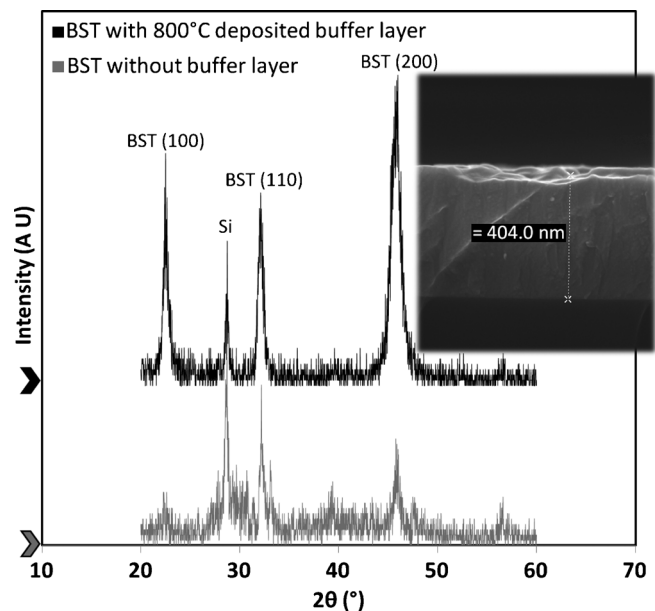


FIG. 1. X-ray diffraction patterns of BST films. Black line: crystallization of BST deposited on hrSi at 700 °C with buffer layer deposited at 800 °C. Gray line: crystallization without buffer layer. The inset shows a SEM view of the sample with buffer layer (corresponding to the black line).

^{a)}Author to whom correspondence should be addressed. Electronic mail: freddy.ponchel@univ-lille1.fr.

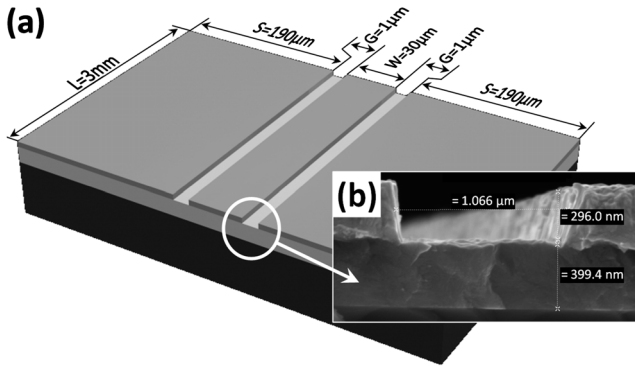


FIG. 2. (a) Three-dimensional scheme of the coplanar strip electrodes and (b) SEM view of a part of the tested coplanar structure and cross-section dimensions. We have magnified the corner of the central conductor to get information on shape and thickness of conductor and BST layer.

have designed a specific MCPW of 1 μm slot width. From a microwave measurement point of view, this required parameter has a significant impact on the characteristic impedance, return, and insertion losses. Consequently, all the other dimensions have been optimized to ensure acceptable [S] parameters dynamics owing to the transmission and reflection uncertainties of the microwave network analyzer in standard configuration and full two port calibration. The central conductor and the planar ground plane have a width of 30 μm and 190 μm , respectively, while the MCPW length is 3 mm [Fig. 2(a)]. With this topology, we predict that [S] parameters dynamic are approximately lower than -35 dB at 60 GHz for a film thickness lower than 1 μm . This design takes into account the frequency behavior of the complex permittivity of BST thin films realized in a previous work.⁶ The gold electrodes are patterned by conventional optical ultraviolet lithography, evaporation, and lift-off process. Figure 2(b) depicts MCPW slot cross section where widths and thicknesses (film, metallization) are precisely measured by scanning electron microscopy (SEM).

All the measurements are performed, in ambient temperature, by means of an Agilent E8361A PNA microwave network analyzer coupled to a Cascade Microtech ground-signal-ground probe station. The scattering parameters are measured in the 1 to 60 GHz frequency band. For the dc electric field control, we use an Agilent E5263A 2-channel high speed source monitor unit, and the set is driven by IC-CAP device modeling software v2009. The bias voltage is swept between +30 and -30 V following the sequence $0 \text{ V} \rightarrow 30 \text{ V} \rightarrow 0 \text{ V} \rightarrow -30 \text{ V} \rightarrow 0 \text{ V}$ by step of 5 V. In a previous work, we ran our home made de-embedding software to extract the complex propagation constant from [S] parameters measurements on a multilayered CPW structure.⁵ This complex value is also the solution of an eigenvalue problem based on a full wave home made vector finite element method.⁹ We match these numerical propagation constants to the measured ones by varying the unknown complex permittivity or permeability or conductivity of the layer of interest. Before measuring the BST thin-film properties, our objective is to define, with the corresponding measurement file, the conductivity of the electrodes and the permittivity of the hrSi substrate using the MCPW (without BST layer) localized on the same wafer, just near the BST/Si-integrated structure described above. We found typically $\sigma = 3.2 \times 10^5$ S/cm for the conductivity of the gold metalliza-

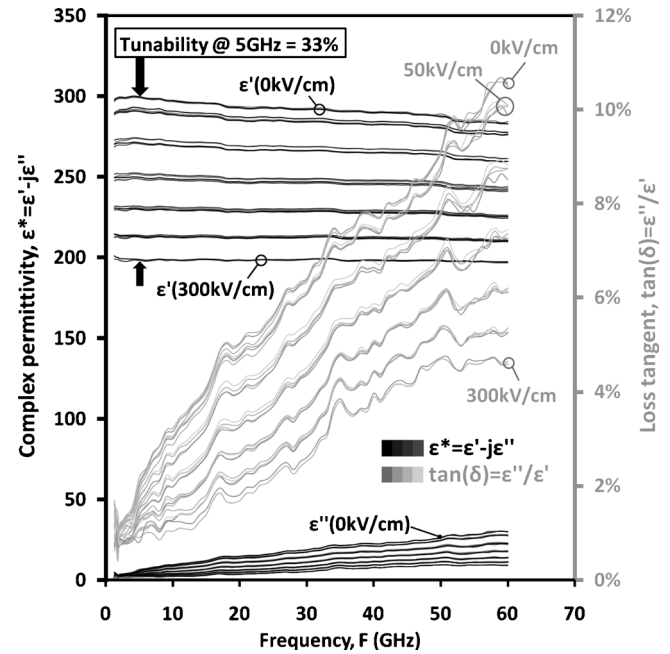


FIG. 3. Frequency behavior of the complex permittivity ($\epsilon^* = \epsilon' - j\epsilon''$) and loss tangent ($\tan \delta = \epsilon''/\epsilon'$) of a 0.4 μm thickness BST layer deposited on a 600 μm hrSi substrate. These values have been extracted and computed from 401 [S] parameters measure points and for each frequency points, 25 bias voltage points following the sequence $0 \text{ V} \rightarrow 30 \text{ V} \rightarrow 0 \text{ V} \rightarrow -30 \text{ V} \rightarrow 0 \text{ V}$ by step of 5 V.

tion and $\epsilon' = 11.2$ for the relative dielectric permittivity of the substrate at low frequencies up to 2 GHz. The conductivity is kept as a constant value over the whole frequency band while the real part of the permittivity decreases slowly to reach $\epsilon' = 11.06$ at 60 GHz. The frequency characteristics behavior of electrodes and hrSi act now as input data in our home made software, the sole unknown being the BST accordability. Let us note that we start here from a file including measurements corresponding to 25 bias voltages steps (from -30 to $+30$ V or 0 to 300 kV/cm) for 120 frequency samples. The results are presented in Fig. 3 for the permittivity and the losses versus frequency. In this graph, different numbers of curves are observed owing to the description of bias voltage cycle. This means that we encountered four times, in absolute value, the voltages 5, 10, 15, 20, and 25 V, three times the zero dc value, and two times the maximum voltage (-30 and $+30$ V).

With or without external electric field, the relative dielectric permittivity is continuously diminishing. At zero dc bias, it starts with a value of 300 at 5 GHz and attains 284 at 60 GHz. We have a maximum of 5% relative decreasing of the relative dielectric permittivity, so the dispersion in this frequency range is very weak. The loss tangent ($\tan \delta$) stays small, even at high frequency, and evolves from 0.022 to 0.105 at 5 GHz and 60 GHz, respectively. Let us note that with the Agilent E8361A network analyzer, there is a measurement uncertainty of about 0.15–0.2 dB on the dynamic range of our MCPW [S] parameters (0–35 dB). This implies a relative uncertainty on $\tan \delta$ of approximately 2% at 60 GHz, this value increases when the frequency decreases while ϵ' determination is always better than 1%. At 5 GHz, with a 10 V bias voltage corresponding to a field of 100 kV/cm into the coplanar slot, the permittivity and the $\tan \delta$ drop to 273 and 0.015, respectively (198 and 0.009 at 30 V). All these observations are presented in a more comprehen-

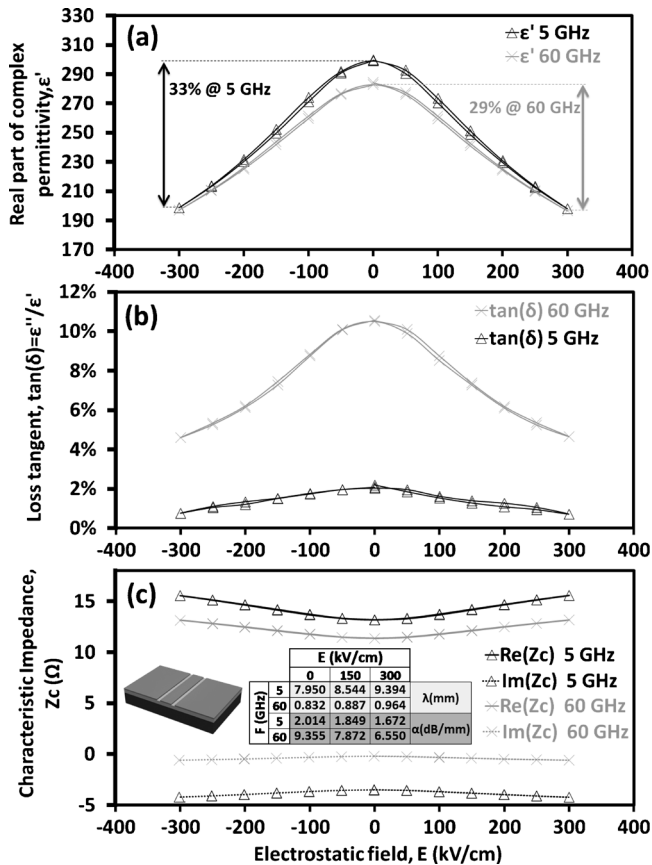


FIG. 4. Electrical field dependence at 5 GHz (black line) and 60 GHz (gray line) of (a) ϵ' and (b) loss tangent ($\tan \delta = \epsilon''/\epsilon'$) of BST thin films deposited on a 600 μm hrSi substrate. (c) Impact of dielectric BST layer accordability on characteristic impedance tunability of the MCPW structure. The table recapitulates electrical field and frequency behavior of guided wavelength and attenuation of MCPW structure.

sive way on Fig. 4. We exhibit, Fig. 4(a), the behavior of the relative dielectric permittivity with dc field variation at 5 GHz and 60 GHz, where we obtain a tunability of 33% and 29%, respectively. As we can see, no hysteresis is observed. Indeed, for $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$ films with $x=0.3$, we are near the ferroelectric–paraelectric transition at room temperature. For these two frequency cases, more than 50% decreasing for the $\tan \delta$ from 0 to 300 kV/cm is observed Fig. 4(b). These results also show that we loose very little accordability with weak losses. At this step, it is clear that low loss tangent and good accordability are very important for capacitance design and manufacturing but they are not as significant as insertion losses and characteristic impedance in circuit theory and design needs. So, we want to give briefly some highlights in term of schedule of conditions in circuit design. It is all the easier since our structure is a waveguide and not an interdigitated or metal-insulator-metal (MIM) capacitor. To this end, we have deduced, from our measurements and dedicated software, the attenuation of the MCPW depicted Fig. 2 and the impedance accordability which is linked to dielectric permittivity tunability. Some results are recapitulated in Fig. 4(c) where the 10–15 Ω range of impedance variation gives approximately -5 dB return loss or 30% reflected power. This mismatch (70% of injected power at the input of the MCPW) has very little incidence on the degradation of [S] parameters accuracy because we always take care not to attain the minimum power that can be measured by the analyzer at the output of the MCPW. Typically, at 60 GHz and 0

V dc polarization, the attenuation (α) reaches approximately 10 dB/mm with $\tan \delta=0.105$ while it attains 2 dB/mm at 5 GHz for $\tan \delta=0.022$. From a design point of view, the 2 dB/mm attenuation with 8 mm guided wavelength (λ) begins to be acceptable if we imagine tunable quarter wavelength impedance transformer for matching active or passive devices. For such circuit, the matching can be done over 15% relative impedance variation [Fig. 4(c)] with approximately 4 dB insertion loss in the whole range of bias polarization. At this step, we must not forget that all the previous attenuation are not entirely due to dielectric losses of the BST film, but, for a great part here, are inherent to metallic losses. It also, strongly, depends upon thickness layers. These rough results in term of impedance matching tunability are very encouraging because initially our structure has been designed, only, to ensure maximum accuracy from [S] parameters and consequently complex permittivity measurements point of view. It can be optimized for impedance matching tunability in a large extent. It can also be improved for minimizing insertion losses, especially for the 5 GHz point which corresponds to wireless carrier frequency in telecommunication system, but it was not our aim in the present paper. This trial and rough estimates exhibit another way for tunable circuit in silicon environment.

In summary, we have shown that the $\text{Ba}_{0.3}\text{Sr}_{0.7}\text{TiO}_3$ thin film sputtered onto buffered hrSi substrate presents excellent properties up to 60 GHz. Without external voltage bias, the dielectric permittivity and $\tan \delta$ values evolve from 300 (5 GHz) to 284 (60 GHz) and 0.022 (5 GHz) to 0.105 (60 GHz), respectively. When we applied an external dc polarization of 30 V (300 kV/cm), we obtained a tunability of 33% and 29%, respectively, at 5 GHz and 60 GHz with a significant reduction in $\tan \delta$ (more than 50%). Our work has been planed around wave propagating structures and not interdigitated or MIM capacitor measurements. So, we can speak about characteristic impedance, wavelength, and attenuation which are some key parameters in circuit design. We deduced, for our studied structure, that 30% dielectric accordability produced approximately 15% tuning on characteristic impedance with 2 dB/mm attenuation at 5 GHz. These data are very promising for tunable quarter wavelength adaptor of 2 mm length around 5 GHz because they can be optimized a lot. It opens the way for the fabrication of compact agile integrated devices based on this kind of materials in silicon environment.

- ¹J. Im, O. Auciello, and S. K. Streiffer, *Thin Solid Films* **413**, 243 (2002).
- ²M. W. Cole, P. C. Joshi, M. Ervin, M. Wood, and R. L. Pfeffer, *J. Appl. Phys.* **92**, 3967 (2002).
- ³G. Houzet, L. Burgnies, G. Velu, J.-C. Carru, and D. Lippens, *Appl. Phys. Lett.* **93**, 053507 (2008).
- ⁴B. Xiao, H. R. Liu, V. Avrutin, J. H. Leach, E. Rowe, H. Y. Liu, Ü. Özgür, H. Morkoç, W. Chang, L. M. B. Allredge, S. W. Kirchoefer, and J. M. Pond, *Appl. Phys. Lett.* **95**, 212901 (2009).
- ⁵F. Ponchel, J. Midy, J. F. Legier, C. Soyer, D. Rémiens, T. Lasri, and G. Guéguan, *J. Appl. Phys.* **107**, 054112 (2010).
- ⁶T. Yamada, K. F. Astafiev, V. O. Sherman, A. K. Tagantsev, P. Mural, and N. Setter, *Appl. Phys. Lett.* **86**, 142904 (2005).
- ⁷T. Yamada, P. Mural, V. O. Sherman, C. S. Sandu, and N. Setter, *Appl. Phys. Lett.* **90**, 142911 (2007).
- ⁸E. Cattani, G. Velu, B. Jaber, and D. Rémiens, *Appl. Phys. Lett.* **70**, 1718 (1997).
- ⁹F. Ponchel, J. F. Legier, E. Paleczny, C. Séguinot, and D. Deschacht, "Proximity effect of neighbour victim lossy interconnects on a single attacker and vice versa," IEEE International Symposium on Integrated Circuits (ISIC 2007), Singapore, 2007, p. 406.