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Self-consistent electrothermal Monte Carlo simulation of single InAs nanowire channel metal-insulator field-effect transistors

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Electron transport and self-heating effects are investigated in metal-insulator field-effect transistors with a single InAs nanowire channel, using a three-dimensional electrothermal Monte Carlo simulator based on finite-element meshing. The model, coupling an ensemble Monte Carlo simulation with the solution of the heat diffusion equation, is carefully calibrated with data from experimental work on these devices. This paper includes an electrothermal analysis of the device basic output characteristics as well the microscopic properties of transport, including current-voltage curves, heat generation and temperature distributions, and electron velocity profiles. Despite the low power dissipation, results predict significant peak temperatures, due to the high power density levels and the poor thermal management in these structures. The extent of device self-heating is shown to be strongly dependent on both device biasing configuration as well as geometry. © 2010 American Institute of Physics. [doi:10.1063/1.3496658]

I. INTRODUCTION

The miniaturization of device features has led to the fabrication of integrated circuits with increased packing density and functionality, resulting in a considerable growth in the semiconductor industry allowing faster and more sophisticated electronic products to be commercialized. However, with state-of-the-art device sizes reaching the nanometer range, the application of traditional scaling methods (by maintaining the devices basic geometry while shrinking its size) is facing numerous technological roadblocks and fundamental challenges. With the traditional scaling techniques approaching their limits, further improvements in device performance should be expected from the production of innovative designs, with a profound change in geometry, rather than reduction in device dimensions. Improvements in nanodevice manufacturing processes allowed the fabrication of several advanced electronic nanostructures. For example, while advances in nanolithography allowed the manufacturing of complex-geometry nanodevices such as ballistic switches¹ and fin-shaped field effect transistors (FinFETs),² recent developments in “bottom-up” fabrication techniques led to the realization of a wide variety of nanowire structures.³ Therefore, the development of reliable three-dimensional (3D) simulation models allowing an accurate theoretical study of complex-geometry nanostructures is necessary, first to help designing structures with an optimum performance, and second to provide insight into their physical behavior which is still incompletely understood.^{4,5}

The increased importance of self-heating is considered to be one of the major challenges facing device designers in developing reliable nanoelectronic structures with optimal performance. In this paper, we report results from the study of omega-shaped gate metal-insulator field-effect transistors

(MISFETs) based on a 50 nm diameter InAs nanowire channel,³ using a suitably calibrated 3D electrothermal Monte Carlo (MC) simulator. By means of this thermally self-consistent simulation model, we present a study of electron transport including a reliable prediction of self-heating effects in these devices. InAs nanowire MISFETs are attractive devices, as they show superior transport properties compared to InAs channel heterostructure FETs. In fact, these nanowire structures are characterized by excellent saturation behavior, high breakdown voltage, current density, and transconductance.³

The purpose of this work is twofold: improving the understanding of transport at the microscopic scale, and demonstrating the role played by thermal effects in these devices. The effect of device self-heating may be important for two main reasons. In areas where the electric field is high, the high current densities in the nanowire are accompanied by significant heat generation. Moreover, material factors, such as the poor thermal conductivity of nanowires⁶ and silicon nitride (SiN_x, which is the used gate-oxide material),⁷ negatively affect device thermal management. High power densities combined with poor thermal management naturally results in a considerable temperature rise affecting transport and device reliability. By studying transport at the microscopic level, we demonstrate how the extent of self-heating may be dependent on biasing conditions as well as device geometry.

In general, this work presents a 3D microscopic analysis of electron transport and electrothermal effects in nanowire MISFETs, to provide a more accurate insight into their operation. By employing finite-element meshing, our model correctly accounts for the geometrical features of the simulated devices, and is suitably calibrated with experimental data to provide reliable results. Although nanowire structures are widely considered as one-dimensional structures, 3D

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finite-element based simulations, correctly accounting for the real device geometry, including the form of the metallic contacts as well the nanowire diameter, gate-oxide thickness and the buffer and substrate layers, are necessary for an accurate analysis of the performance of these devices. As well as extracting the macroscopic and microscopic characteristics of the simulated devices, the self-heating phenomenon is investigated in the structures. The influence of device biasing configurations and important geometrical parameters, such as the gate-oxide thickness, on the electrothermal behavior is established. This paper is organized as follows. Section II describes the simulation model used in this study. Section III includes a detailed description of the simulated nanowire MISFET structure. Section IV includes a thorough analysis and discussion of the simulation results.

II. SIMULATION DETAILS

The simulation method is an iterative procedure using phonon statistics to self-consistently couple a 3D MC trajectory simulation method with the solution of the 3D time-independent heat diffusion equation (HDE). At the end of a MC simulation (iteration), the power density distribution is calculated by counting the net phonon emission in the device active region (in this case the nanowire), as employed in Ref. 8. The power density distribution is then fed into a HDE solver to determine the temperature distribution in the device. The calculated temperature distribution is then employed in the subsequent MC simulation as the lattice condition of the device, and the simulation process is repeated until electrothermal convergence is achieved. The number of MC iterations needed for the device terminal currents to converge to their electrothermal value does not normally exceed five. Each MC iteration (lasting approximately 60 to 70 ps) includes a transient period (30 to 40 ps) to allow the electronic characteristics to reach a steady state, and an equilibrium period (25 to 30 ps) where electronic statistics (such as the drain current, electron velocity, and energy distributions) and thermal statistics (such as the heat generation distribution) are taken. During a MC simulation, Poisson's equation is solved every 0.5 fs. An important issue arising from the coupling of an electronic transport simulation to any thermal model is the significant difference in the characteristic time scales of electronic and thermal transport: electronic transients in III-As systems are of the order of picoseconds, whereas thermal transients may be of the order of nanoseconds, microseconds, or even longer. While performing MC computations for the duration of thermal transients would not be feasible, it is also not necessary when studying static dc electrothermal characteristics, as is the case here. Consequently, the simulator used in this work extracts steady-state thermal device characteristics only, by solving the time-independent HDE (Ref. 9) once at the end of each MC iteration. A description of the general concept of self-consistent electrothermal MC modeling can be found in Ref. 9.

Substantial efforts have been invested to carefully integrate into our simulator a finite-element package [NETGEN/NGSOLVE (Ref. 10)] to solve for Poisson's and the heat diffusion equations. This package provides efficient device

meshing and a reliable solution of these equations, irrespective of the level of complexity of the simulated device geometry. The electrothermal MC method has been successfully employed to study transport in conventional heterostructure FET devices based on several material systems, including Si,^{11,12} III-As,⁹ and III-N (Refs. 13 and 14) compounds, using our two-dimensional (2D) in-house simulator. Other simple electrothermal MC models have also been developed and used for different purposes, such as the validation of hydrodynamic simulation models.¹⁵ In simple heterostructure field effect transistor (HFET) geometries, employing 2D solvers based on analytical models or finite-difference meshing is sufficient for a reliable study of the coupled effect of electron transport and heat diffusion. However, for the nanowire-based FET structures simulated here, 3D modeling using finite-element meshing is essential for the correct inclusion of the shape of the metallic contacts as well as the nanowire diameter and gate-oxide thickness in the simulations.

Since the main aim of this work is to demonstrate electrothermal effects in the nanowire FET, we use a spherical nonparabolic model to describe the bandstructure of InAs. The simulator considers the effect of all the important scattering mechanisms, including intravalley acoustic and optical phonon scattering, intervalley phonon scattering, and ionized impurity scattering. The effect of nonequilibrium phonon distributions (hot-phonon effect),¹⁶ a phenomenon directly associated with thermal effects, is not expected to influence significantly the device thermal behavior, and hence is not included in the simulation model. Instead, equilibrium phonon occupation numbers, determined from the Bose–Einstein distribution, are used in the phonon scattering rate formulas. In spite of the relatively large length (few microns) and nanowire diameter (50 nm) of the experimental-based nanowire devices studied here, the presence of quantization effects (resulting from carrier confinement in the nanowire) may play a role in determining some aspects of the device characteristics, mainly the free-carrier distribution in the (2D y - z) plane perpendicular to the direction of transport (x -direction). Nonetheless, these effects are not expected to affect significantly the quantitative and qualitative conclusions made regarding electrothermal effects. Quantization effects may be considered by the coupling of the solutions of Poisson's and Schrodinger equations. However, the application of this procedure results in a significant increase in simulation time, and hence such effects are not accounted for in this work.

III. SIMULATED STRUCTURE

In this work, we present results from the study of the InAs nanowire MISFET investigated in Ref. 3, including an omega-shaped gate. The geometry of the simulated device is fully illustrated in Fig. 1. The structure incorporates an InAs nanowire with a diameter (D) of 50 nm, an omega-shaped gate with a length (L_G) of 1 μm , and a (SiN_x) gate-oxide layer with a thickness (T_{OX}) of 30 nm separating the gate from the nanowire surface. For the purpose of this study, the separations between the source and gate contacts (L_{SG}) and

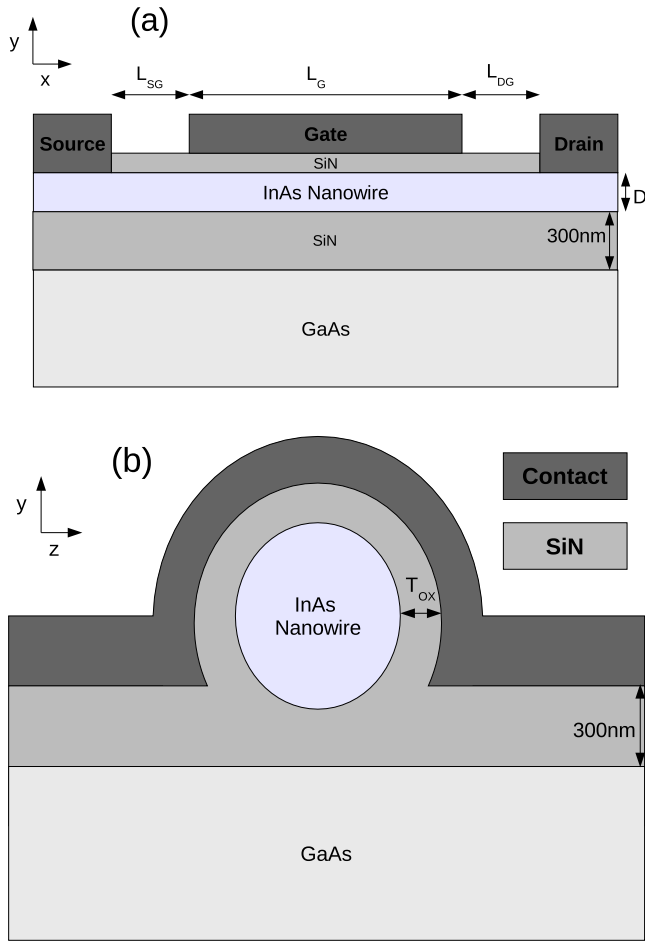


FIG. 1. (Color online) The geometry of the simulated InAs nanowire MISFET: (a) cross-section along the x -direction (direction of transport) and (b) cross-section along the z -direction under the gate terminal. In this case, the nanowire diameter (D) is set to 50 nm, the gate-oxide thickness (T_{ox}) is set to 30 nm and the gate length (L_G) is set to 1 μm . The source-gate (L_{SG}) and the drain-gate (L_{DG}) separations are both taken to be 0.5 μm .

the drain and gate contacts (L_{DG}) are both set to be 0.5 μm . The nanowire and the contacts lie on top of a 300 nm SiN_x buffer layer, as shown in Fig. 1. The complete structure is assumed to be built on top of a single GaAs die. A fixed-temperature (300 K) heat-sink is placed at the die base to allow heat removal. For the solution of the HDE, adiabatic thermal boundary conditions are applied at the other die surfaces, allowing heat to flow out of the device only through the base surface of the die. The length (L_D), width (W_D), and depth (D_D) of the die are all set to 100 μm . It is of note that the simulated structure shown in Fig. 1 is symmetrically located at the center of the die. In this case, the center of the structure is located at a perpendicular distance of $L_D/2$ from the die side walls normal to the x -direction (direction of transport), and at a perpendicular distance of $W_D/2$ from the die side walls parallel to the x -direction. The simulator includes carefully the thermal conductivity properties of the GaAs substrate, the InAs nanowire, the SiN_x layers, and the Ti/Au metallic contacts incorporated in the device. Table I shows thermal conductivity values of few materials at room temperature. The existence of a positive surface charge of a concentration of $\sim 10^{12} \text{ cm}^{-2}$ is assumed at the nanowire surface, which is similar to the values reported

TABLE I. Thermal conductivities of few materials at room temperature (300 K).

Material	Thermal conductivity ($\text{W m}^{-1} \text{K}^{-1}$)
GaAs (bulk)	55
InAs (bulk)	27
InAs nanowire ($D=50 \text{ nm}$)	$\sim 7^a$
SiN_x	$\sim 2^b$

^aReference 6.

^bReference 7.

experimentally.¹⁷ It is important to point out that the choice of studying experimental structures (with gate lengths ranging from one micron to few microns) is motivated by the need to validate our simulator and establish its reliability. This is to provide a reliable investigation of electron transport and a realistic prediction of the extent of self-heating in existing nanowire MISFET structures.

IV. RESULTS, ANALYSIS, AND DISCUSSIONS

To validate our simulation model, we show in Fig. 2 the measured and the simulated I_d-V_{ds} and I_d-V_{gs} characteristics of the 2 μm gate length MISFET studied in Ref. 3, with nanowire diameter and gate-oxide thickness of 50 nm and 30 nm, respectively. This figure illustrates the excellent agreement between the experimental data presented in Ref. 3 and the results we obtained from the simulation of this device. The relatively small deviations are believed to be due mainly to the slight difference between the simulated and real device geometries. Figure 3 shows the isothermal (at 300 K) and electrothermal I_d-V_{ds} and I_d-V_{gs} characteristics of the 1 μm gate length device described in Fig. 1. Figure 3 demonstrates self-heating effects at the macroscopic level, by showing the drain current reduction upon the inclusion of electrothermal self-consistency. Such reduction increases with the increasing gate and drain biases due to the increase in device temperature, as demonstrated below. At high gate biases (e.g.,

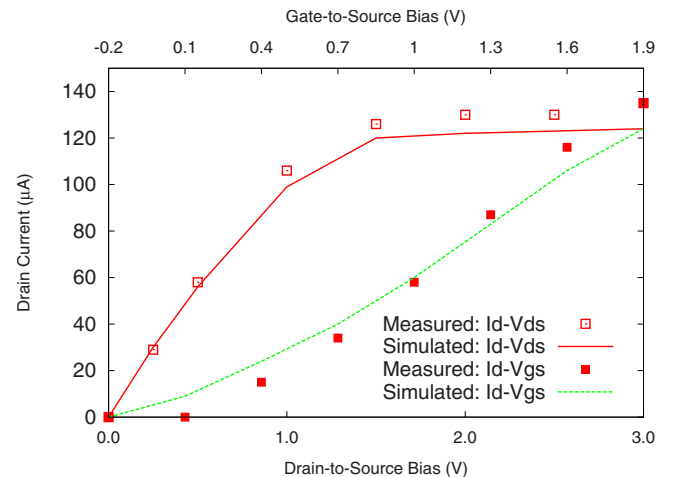


FIG. 2. (Color online) The measured and simulated I_d-V_{ds} characteristics of the 2 μm gate length MISFET studied in Ref. 3 at $V_{gs}=1.9 \text{ V}$, and the measured and simulated I_d-V_{gs} characteristics of this MISFET at $V_{ds}=3.0 \text{ V}$.

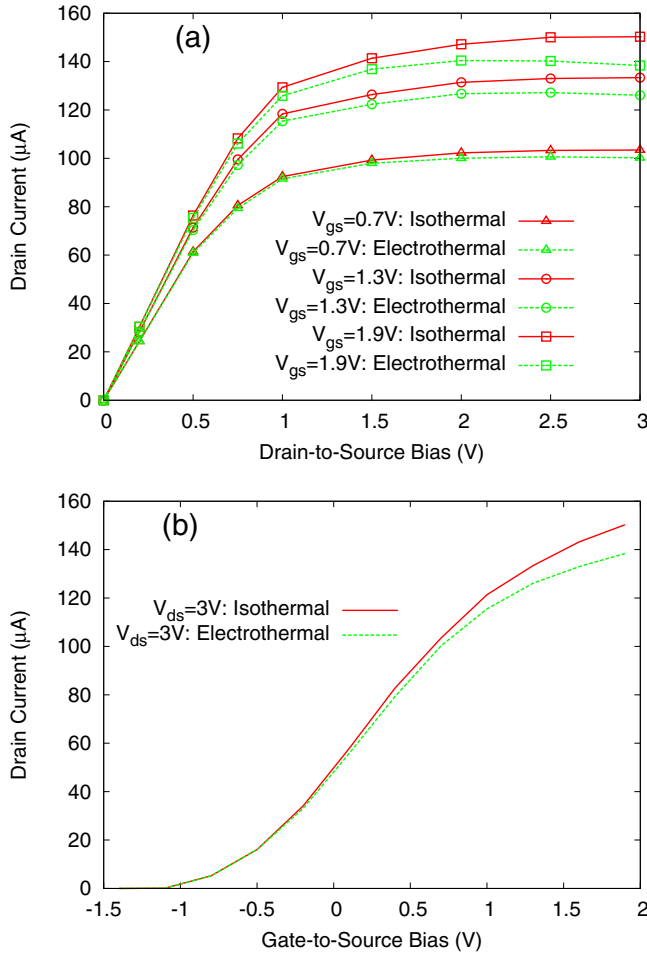


FIG. 3. (Color online) (a) The isothermal and electrothermal I_d - V_{ds} characteristics of the $1 \mu\text{m}$ gate MISFET studied here, for different gate biases (0.7, 1.3, and 1.9 V). (b) The isothermal and electrothermal I_d - V_{gs} characteristics of the device at $V_{ds}=3.0$ V.

1.9 V), the thermal droop effect, which corresponds to a negative output conductance at high drain biases, is observed from the I_d - V_{ds} characteristics in Fig. 3(a).

For a deeper understanding of the electrothermal behavior of the simulated devices, we show in Fig. 4 the average electron kinetic energy and power density calculated from counting the net phonon emission, along the nanowire for different gate and drain biases, as well as T_{OX} values. Figure 4 illustrates the existence of regions where heat generation may be significant: near the gate-end of the drain ($x \sim 2.1 \mu\text{m}$) and (to a lower extent) under the gate (and at both ends of the gate). Figure 4(a) shows how applying higher drain biases increases the kinetic energy along the nanowire, especially in the gate-side of the drain, where a peak value is generally observed. Figure 4(a) also illustrates how the power densities are affected in the same trend, with a peak value observed in the drain side. Figure 4(b) illustrates how increasing the gate biases gives rise to higher kinetic energies near the source-end of the gate, giving rise to more heat generation under the gate. In general, in the drain side (where the peak power density and energy occur), Fig. 4 illustrates how the location of the peak power density is always ahead of the location of the peak energy, corresponding to the time needed for the highly-energetic elec-

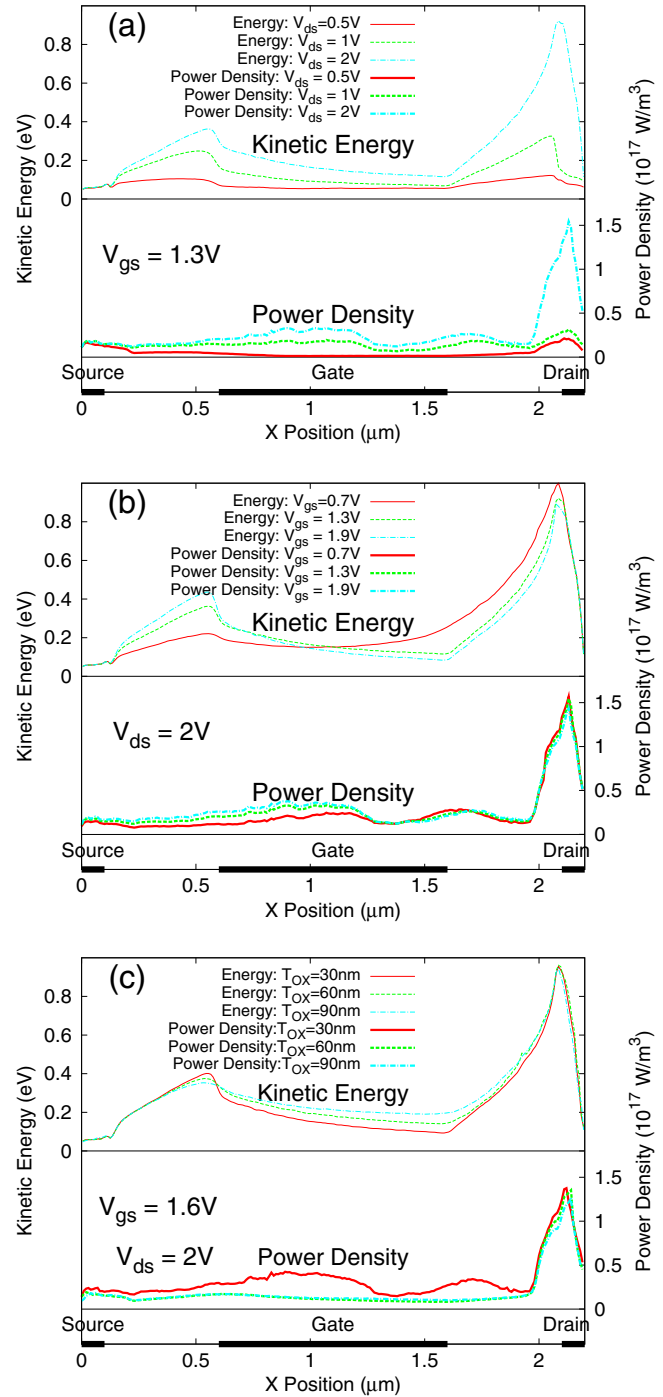


FIG. 4. (Color online) The average electron kinetic energy and power density along the nanowire, for different (a) drain biases, (b) gate biases, and (c) T_{OX} values.

trons to start emitting phonons. As can be seen from Fig. 4(c), heat generation is less important under the gate for thicker gate-oxides, due to the reduced gate-bias influence. However, a secondary peak in power density is still visible at the source-end of the gate.

Figure 5 shows the average temperature along the nanowire, for different gate and drain biases, and T_{OX} values. The distributions indicate how temperature generally increases at higher gate and drain biases. The temperature distribution profiles show two peak temperatures, one located near the gate-end of the drain and another one near the source-end of

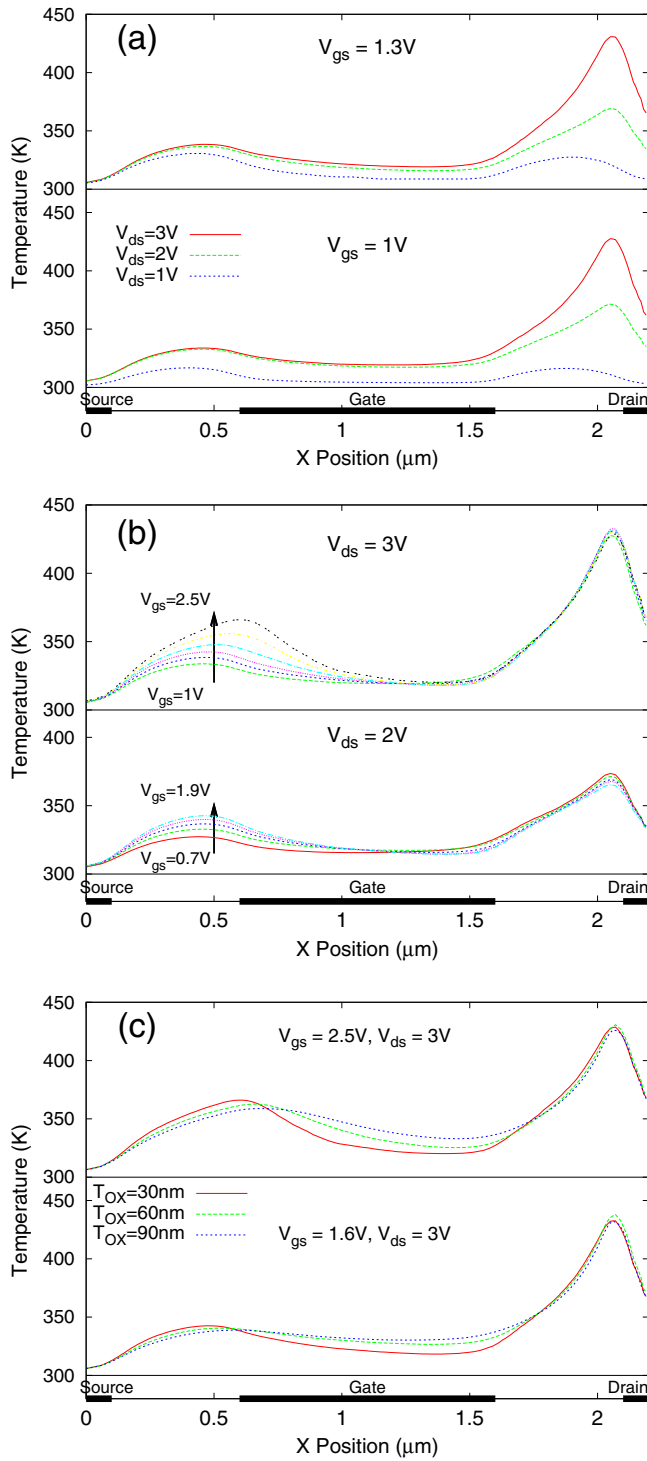


FIG. 5. (Color online) The average lattice temperature along the nanowire, for different (a) drain biases, (b) gate biases, and (c) T_{OX} values.

the gate ($x \sim 0.6 \mu\text{m}$). The former is mainly dependent on drain bias as illustrated in Fig. 5(a), and the latter is mainly dependent on gate bias as illustrated in Fig. 5(b). In spite of the significant amount of heat generated under the gate, relatively low temperatures are obtained in this region. This is due to the fact that heat is relatively easy to evacuate through the gate metallic contact, which is only separated from the nanowire by few tens of nanometers (T_{OX}). In spite of the relatively small amount of heat generation in the ungated regions (between source and gate, and gate and drain), tem-

perature rise is still significant in these areas. This is because heat removal is more challenging in these regions, where a very low thermal conductivity material (SiN_x) surrounds the nanowire. At biasing conditions where the influence of gate voltage is more important than that of the drain voltage, the location of the peak temperature shifts to the source-end of the gate (as illustrated, for example, in Fig. 5(a) at gate and drain biases of 1.3 V and 1 V, respectively). Figure 5(c) also demonstrates the important role played by T_{OX} ; in spite of the reduced heat generation under the gate in devices with higher T_{OX} values [see Fig. 4(c)], higher temperatures are obtained in this region since heat removal is more challenging at higher T_{OX} values.

Figure 6 shows the variation in the average temperature in the nanowire with gate bias, and the average and peak temperatures (in the nanowire) with the total macroscopic power dissipation (the product of the drain current and the drain bias $I_d \times V_{ds}$) for three T_{OX} values. The average temperature values (up to ~ 360 K) are considerably lower than the peak temperature values, explaining the visible but limited effect of self-heating on the device currents ($< 10\%$ for $T_{OX} = 30$ nm as shown in Fig. 3). However, the peak temperature values are significant (up to 450 K) due to the elevated power density levels, which may have serious effects on device long-term reliability and lifetime. One positive observation is the relatively small effect of self-heating on device currents for $T_{OX} = 30$ nm. However, Fig. 6 indicates that applying higher gate biases may significantly increase the average temperature, especially at higher T_{OX} values, possibly resulting in a much more significant device current reduction upon the inclusion of thermal effects.

To obtain a general idea about the thermal management of single InAs Nanowire channel MISFETs, we carry out a comparison of the thermal performance between the device and conventional InGaAs-channel heterostructure FETs. For this purpose, we show in Fig. 7 the variation in the peak temperature with the total power dissipation for the InGaAs/AlGaAs high electron mobility transistor (HEMT) simulated in Ref. 9. The HEMT has a $0.2 \mu\text{m}$ gate-length and a $100 \mu\text{m}$ gate-width. The much higher slope for the “peak temperature versus power dissipation” curves for the nanowire MISFET [see Fig. 6(c) as compared to Fig. 7] indicates that this device is characterized by significantly poor thermal management, as compared to conventional III-As HEMTs. This is, of course, due to the low thermal conductivity of the elements forming the structure, including the nanowire but most importantly the SiN layers surrounding the nanowire preventing efficient heat transfer in the structure.

Figure 8 shows the variation in the isothermal and electrothermal mean electron velocity in the x direction along the nanowire, for different drain and gate biases, and T_{OX} values. The expected reduction in the electron x velocity due to self-heating is illustrated, which is observed to be generally more important at higher drain biases. In Fig. 8(a), the visible reduction in both the isothermal and electrothermal velocity values near the gate-end of the drain (around $x \sim 2.1 \mu\text{m}$), at higher drain biases, is associated with the increased number of phonon scattering events in this region [as demonstrated in Fig. 4(a)], where high kinetic energy values encourage this

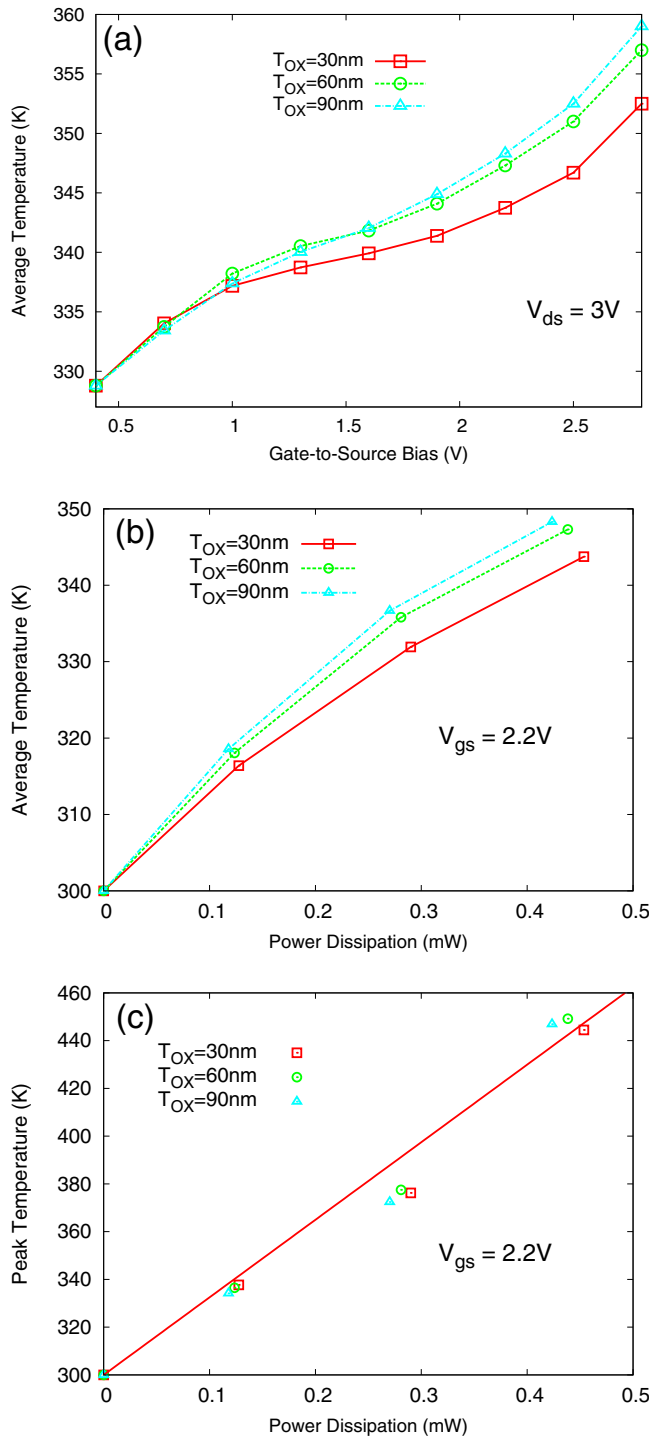


FIG. 6. (Color online) Variation in (a) the average temperature (in the nanowire) with gate bias, (b) the average, and (c) peak temperatures (in the nanowire) with the total power dissipation for different T_{OX} values.

type of scattering. In Fig. 8(b), lower isothermal and electrothermal velocity values are observed under the gate at higher gate biases, which is also associated with the increased number of phonon scattering events in this region [as illustrated in Fig. 4(b)]. Figure 8(c) shows how the gate-oxide thickness affects the electron velocity in the x direction, at the same biasing conditions. The effect of gate bias is weaker at thicker gate-oxides, corresponding to less phonon emission [see Fig. 4(c)] and hence higher velocities under the gate area.

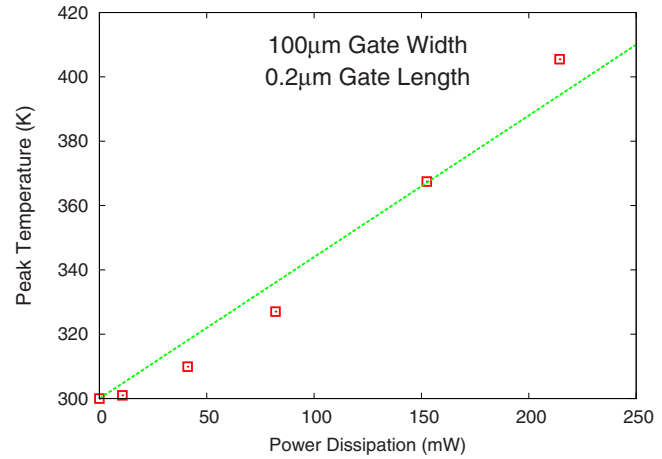


FIG. 7. (Color online) Variation in the peak temperature with power dissipation for the InGaAs-channel HEMT simulated in Ref. 9.

While this work focuses on studying thermally self-consistent electronic characteristics in the device active region (nanowire), it is interesting to discuss the effect of the semiconductor die dimensions on the device thermal behavior. As is well known, the temperature values in the device active region depends on both the thermal boundary conditions in place and the semiconductor die dimensions.¹¹ In general, and by considering the boundary conditions applied in this work (see Sec. III), it can be predicted that a reduction in the die length or width would result in an increase in the nanowire temperature, while a reduction in the die depth would result in a decrease in the nanowire temperature. Figure 9 shows the variation in the temperature along the depth (y -direction), at different x -coordinate values in the nanowire, at the z -coordinate corresponding to the center of the nanowire. The extremely low thermal conductivity of the SiN buffer represents a significant challenge for heat diffusion into the GaAs substrate. This gives rise to temperatures neighboring 300 K in the substrate, one micron below the nanowire, as shown in Fig. 9. This result indicates that temperature in the substrate is not significantly disturbed, and remains at approximately the heat-sink temperature (300 K). The result also leads to the conclusion that reducing the die depth (and hence moving the 300 K heat-sink location closer to the active region) would not affect seriously the device temperatures. Since most of the heat diffuses along the nanowire and in the contacts, one would expect that the reduction in the die length or width would result in a relatively more visible change (rise) in the nanowire temperature. It is noteworthy that the die dimensions used here ($100 \times 100 \times 100 \mu m^3$) are typical values for III-As FETs. While it has been established that even significant changes in the die depth would not significantly affect device temperatures, only a considerable (e.g., tenfold) reduction in the die length and width would result in a significant temperature increase. Temperature changes in the nanowire are expected to be insignificant in case of any small changes (in the order of few microns) in the die dimensions.

V. CONCLUSION

In this paper, electron transport and self-heating effects are investigated in single InAs nanowire channel MISFETs

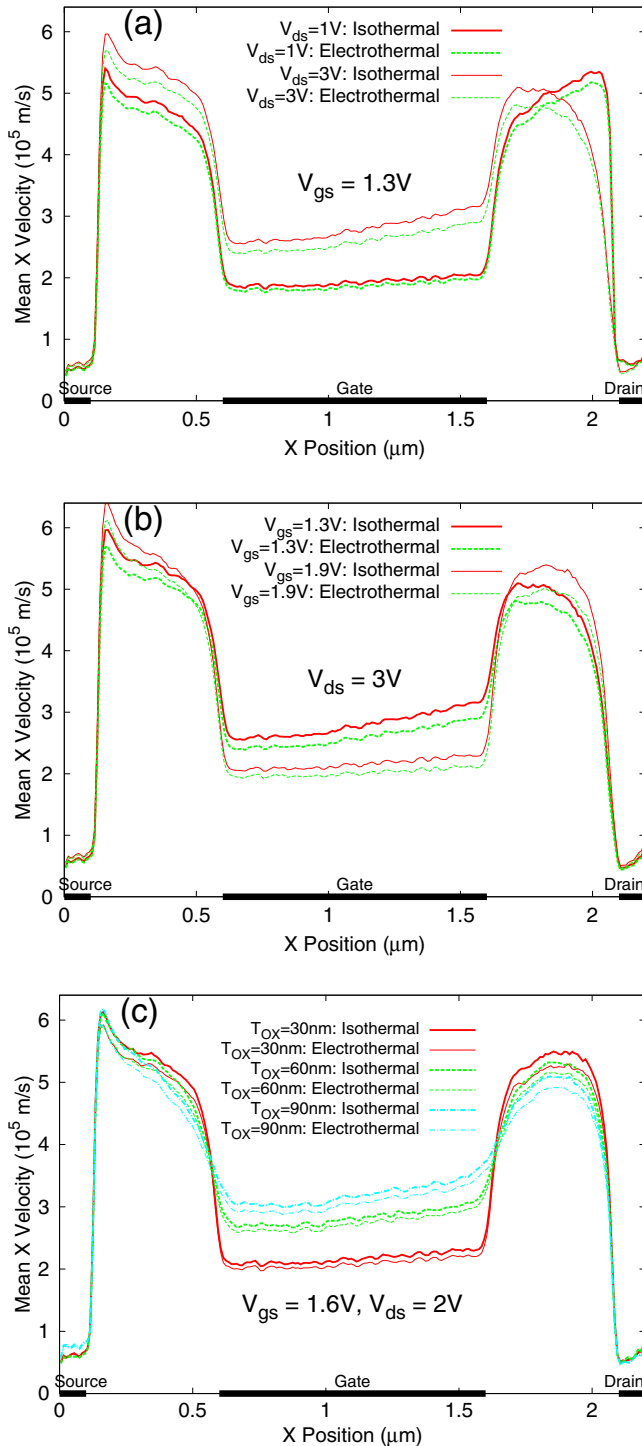


FIG. 8. (Color online) Variation in the mean electron velocity in the x direction along the nanowire, for isothermal and electrothermal conditions, for different (a) drain biases, (b) gate biases, and (c) T_{OX} values.

using a well-established 3D thermally self-consistent MC simulator based on finite-element meshing. The device basic output characteristics and the microscopic properties of electron transport were studied, and the electrothermal behavior of the device is analyzed demonstrating the dependence of the extent of self-heating on bias and geometrical param-

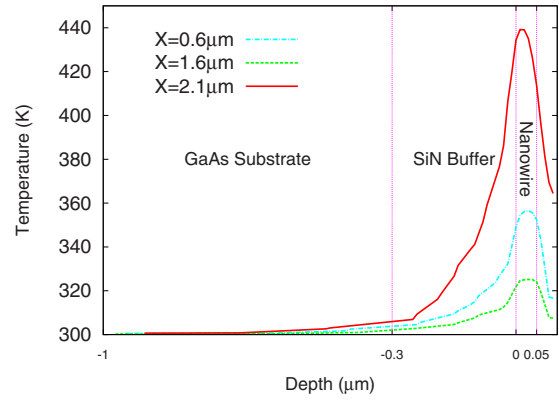


FIG. 9. (Color online) Variation in the temperature along the depth (y-direction) at $V_{gs} = 2.5\text{ V}$ and $V_{ds} = 3.0\text{ V}$. The profiles are taken at the z coordinate corresponding to the center of the nanowire, at different x coordinates in the nanowire.

eters. Despite the fact that these devices are characterized by a low power dissipation, significant temperature rise is observed in the structures (up to 450 K), which inversely affects the performance and reliability of these nanodevices. This is a result of the high power density levels combined with the poor thermal management in these structures, which is attributed mainly to the low thermal conductivity of SiN_x and the InAs nanowire. This study is performed for InAs nanowire MISFETs, but the findings may be extended to similar field-effect nanostructures.

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