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# **Carbon Nanotubes and Semiconductor Nanowires for Active Matrix Backplanes.**

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## **ABSTRACT**

*Carbon nanotubes (CNTs) and semiconductor nanowires (NWs) are a new class of materials currently being studied within the context of molecular electronics. Because of their excellent characteristics, CNT- and NW-based transistors could become the workhorse of the post CMOS era. Since CNTs as well as Si or Ge NWs can be grown at low temperature and on non crystalline and non refractory substrates, they could certainly be used in the near future for TFT and active matrix backplane fabrication. However, the development of these materials is hampered by the general problems posed by their manipulation, their placement and their in-plane organisation. In this paper, we first review the possible use of CNT random networks (that do not need to be organised) for the fabrication of thin film transistors (TFTs). We then present a new way of organising semiconductor NWs in a TFT, based on the use of lateral porous anodic alumina templates.*

## **INTRODUCTION**

Active matrix displays are based on planar arrays of thin film transistors (TFTs). Today, the most mature, simple and cost effective TFT technology makes extensive use of hydrogenated amorphous silicon (a-Si:H), as millions of squared meters of glass substrates are coated with this material. However, due to some drawbacks, such as gate instabilities [1] (particularly when the duty cycle is high), other TFT technologies are currently needed and have been developed, especially for addressing organic light emitters (OLEDs) or for fabricating flexible displays. Low temperature polysilicon technology (LTPS) is one of those, but its acceptance in industry is still low, because it is complex [2] (and expensive) and its productivity (the throughput in particular) is lower than that achieved in AMLCD factories with a-Si:H.

Also, organic semiconductors and TFTs made of such materials [3] are currently being studied, but device stability is still an issue.

In this paper, we will present some novel approaches to TFT fabrication (compatible with glass substrates) that use carbon nanotubes (CNTs) and semiconductor nanowires (essentially Si and Ge). We will also emphasise the possible use of carbon nanotubes “films” (or rather “mats”) as transparent electrode material in replacement of ITO or ZnO-based materials.

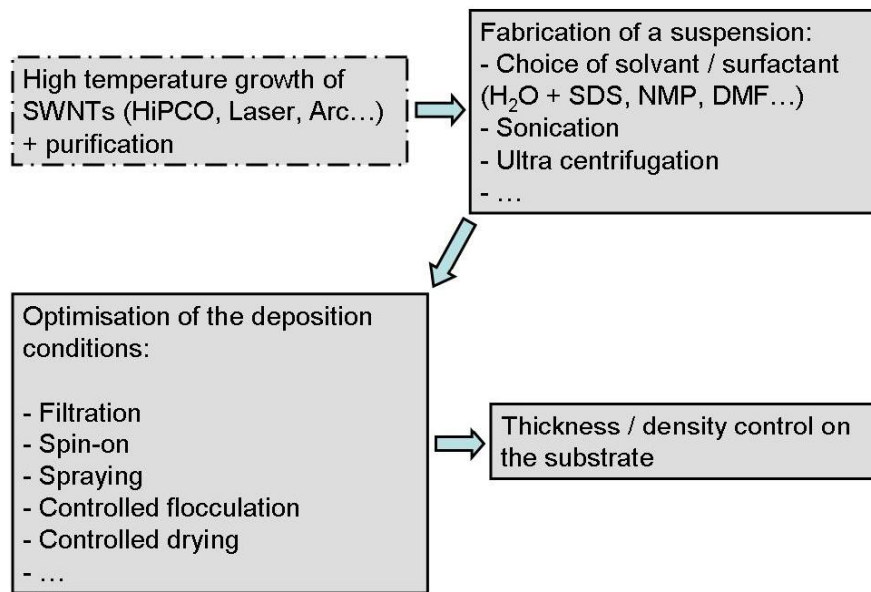
## **CARBON NANOTUBES**

Single wall carbon nanotubes (SWNTs) can be viewed as resulting from rolling-up a graphene sheet into a seamless cylinder with a diameter between  $\sim 0.7$  and several nanometers (nm). Depending on the way the C atoms connect when the cylinder is formed, SWNTs can be metallic or semiconductor [4]. For semiconductor specimens, the forbidden band gap is

inversely proportional to the diameter  $d$  ( $E_g \sim 0.9 \text{ eV}/d$ , with  $d$  expressed in nm). There is another category of CNTs, named multiwall carbon nanotubes (MWNTs). These are made up of several concentric cylinders and they are metallic [4]. They are materials of choice for field emission devices [5].

Various synthesis methods are used for carbon nanotubes [6], with growth temperatures down to  $\sim 450^\circ\text{C}$  [7]. However, as far as SWNTs are concerned, all these methods produce mixtures of metallic and semiconductor specimens. Complex post-growth separation procedures have to be used [8] if one wants one type of SWNT only (metal or semiconductor). Moreover, SWNTs tend to group into bundles under the action of van der Waals forces, which complicates their separation. Perhaps the simpler way of separating them is to eliminate the metallic ones by electrical breakdown, once a device has been fabricated [9].

Transistors made from *individual* semiconductor (s-) SWNTs are invariably p-type in air and they exhibit impressive properties, with hole mobility values of  $3000 \text{ cm}^2/\text{Vs}$ , very low threshold voltages and subthreshold slope values of  $\sim 70 \text{ mV}$  per decade of current [10]. Ballistic transport has also been demonstrated in short channel devices [11, 12]. The switching mechanism in these transistors is different from that of conventional CMOS devices, since carrier transport is controlled by Schottky barriers at the s-SWNT/metal contact [13]. As a consequence, p-type devices can transform to n-type transistors after annealing under vacuum [14], because the Fermi level alignment at the contacts (*i.e.*, the Schottky barrier heights) is modified by the out-gassing of adsorbed oxygen molecules from the contact regions. For a recent review on the properties of field-effect transistors based on individual s-SWNT, see refs. 15 and 16.



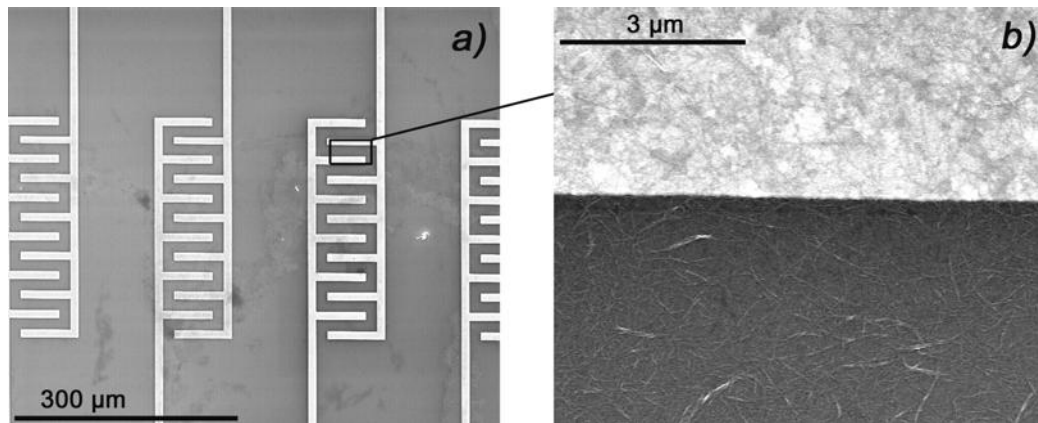
**Figure 1:** Schematics of the various steps needed for the preparation of a CNT suspension. The operations depicted in the upper box on the left-hand side of the picture are usually performed by the CNT supplier.

Devices made from individual s-SWNTs are usually prepared by spreading (typically by spin coating or dipping) a suspension of SWNTs onto a substrate, then indexing the position of specific specimens (by using scanning electron or atomic force microscopy) and subsequently performing e-beam lithography operations for the fabrication of the contacts. Controlling (or rather finding) the position and in-plane orientation of an individual SWNT is therefore a complicated task, which is not amenable to mass fabrication. Moreover, once a SWNT spotted on the substrate and contacted, its conductivity has to be measured in order to assess whether it is semiconducting or not. Finally, for semiconducting specimens, small variations in diameter (*ie.*, in the band gap) will induce irreproducibility in transistor characteristics.

As an alternative to the unrealistic process of using individual SWNTs for device fabrication, researchers have recently investigated the possible use of randomly organised CNT networks. Such networks are generally obtained by spraying, filtration, spin coating, etc... from a precursor suspension of CNTs in a solvent. They yield reproducible electrical

results because of the averaging of physical characteristics over a large number of CNTs. However, the fabrication of CNT suspensions is by no means an easy task, since as grown CNTs are not soluble in most solvents (see *e.g.*, ref. 17 for water-based suspensions). Figure 1 schematically shows the various operations necessary for the fabrication of a suspension. In brief, after growth and purification (operations usually performed by the company selling CNTs), the CNTs are mixed with the appropriate solvent (and surfactant), then they are sonicated, in order to break the bundles and yield individual CNTs. The mixture is subsequently submitted to ultra-centrifugation in order to separate individual SWNTs from the remaining bundles and catalyst impurities. Finally, the supernatant is carefully recuperated.

Once the suspension obtained, the next step is to optimise the deposition conditions, *i.e.*, chose the most convenient spreading method in order to get an easy control over the thickness or areal density of CNTs on the substrate, once the solvent eliminated. As quoted above (see fig. 1), various spreading methods have been used in the literature, such as spin coating, spraying, dipping *etc.*..., and even stamping [18]. The areal density of deposited SWNTs has to be controlled carefully, because above the threshold for percolation, for high areal densities (5 to 10 tubes/ $\mu\text{m}^2$ ), the conduction is practically ohmic [19, 20, 21] with no gating effect [19]. Recent studies show that the conductivity in the networks is controlled by the Schottky barriers at the contacts between metallic and semiconducting tubes [22]. As the thickness of the random CNT network increases, the number of intertube contacts with a low Schottky barrier also increases, providing easy conduction paths and leading to quasi ohmic behaviour [22]. When the films are ohmic, they can be used as transparent electrodes, exhibiting properties close (though still inferior) to ITO [23, 24].

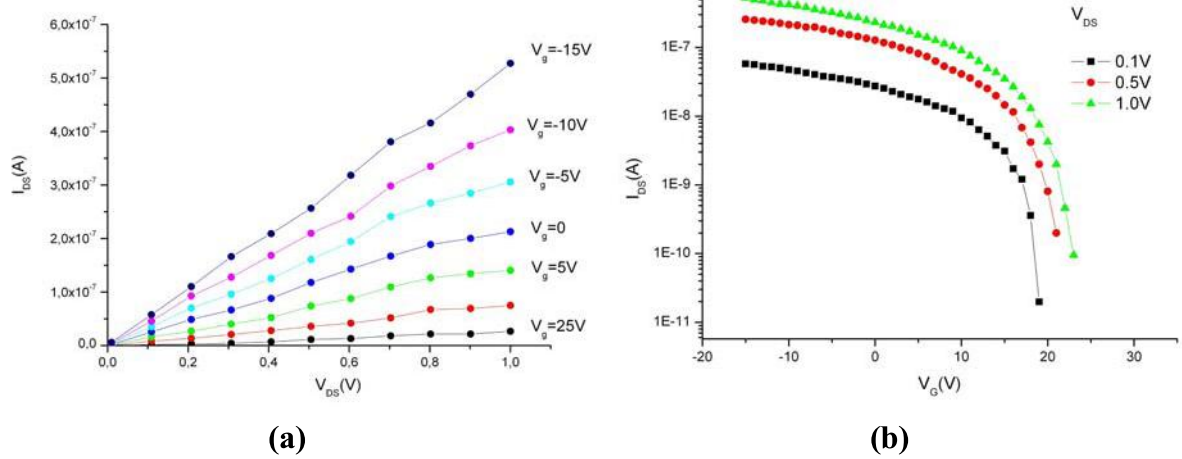


**Figure 2:** (a): Interdigitated bottom gate transistor structure ( $W/L = 15\mu\text{m}/700\mu\text{m}$ ). (b) Detail of the CNT random network between two adjacent contact (gold) electrodes. The bottom gate insulator and gate contact are respectively a 50 nm-thick thermal  $\text{SiO}_2$  film and a doped Si substrate.

Figure 2-a shows bottom gate test transistor structures with interdigitated gold electrodes (source and drain) fabricated in our lab ( $W/L = 15\mu\text{m}/700\mu\text{m}$ ). The random network (see fig. 2-b) was deposited from a CNT suspension in DMF (dimethylformamide,  $\text{C}_3\text{H}_7\text{NO}$ ). For these devices, the gold electrodes were deposited first (*i.e.*, before the CNTs), which is not ideal for obtaining a low contact resistance. The bottom insulator is a 50 nm thick thermal  $\text{SiO}_2$  film and the doped Si substrate is used as gate electrode. Of course, this can be translated to a glass or a plastic substrate, using a deposited metallic thin film for the gate electrode and a deposited insulating thin film as a gate insulator.

Figure 3 shows the corresponding TFT characteristics. These characteristics will be improved in the future, by depositing the source and drain electrodes on top of the CNT random network. Also, it is well known that the gate coupling is more efficient with a high- $\kappa$  top gate structure [10, 15] or with a very thin bottom gate insulator, such as an organic self-assembled monolayer (SAM) [25].

Some characteristics recently published in the literature show that such devices can outperform most TFT technologies (except LTPS, see ref. 2), with On/Off ratio of  $10^7$ , subthreshold slope of 250 mV/decade, threshold voltage of 1V and an effective mobility above  $10\text{ cm}^2/\text{Vs}$  [26, 27].



**Figure 3:** Typical characteristics of a TFT ( $W/L = 100\mu\text{m}/15\mu\text{m}$ ) made from a CNT random network. (a): output characteristics ( $I_{DS}-V_{DS}$ ). (b) transfer characteristics ( $I_{DS}-V_{GS}$ ).

Last but not least, TFTs fabricated from random CNT networks are highly bendable, which makes them ideal for flexible substrates [28] and they can be made transparent using indium tungsten oxide as contact electrodes [29].

## SEMICONDUCTOR NANOWIRES

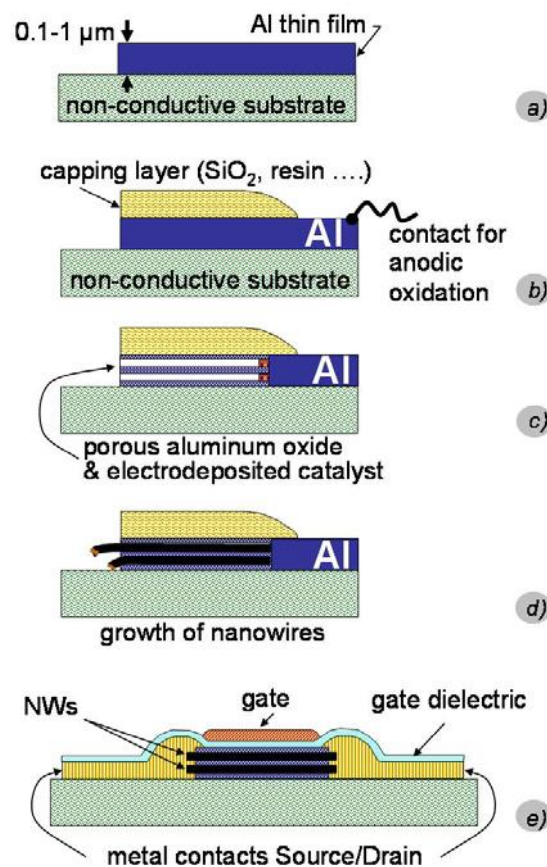
Semiconductor (column IV elements) nanowires (NWs) are currently being extensively studied for the replacement of traditional CMOS devices. Si or Ge NWs are usually grown by the vapour-liquid-solid (VLS) technique (using *e.g.*, gold catalyst particles), which was developed 40 years ago for growing single crystals [30]. A vapour-solid-solid (VSS) process has recently been demonstrated, using Al as catalyst material [31]. The VLS process (that can be tailored to be temperature-compatible with glass substrates) has recently been applied to the growth of NWs and high performance field effect transistors (made with individual NWs) have been demonstrated, exhibiting mobility values up to  $\sim 1300 \text{ cm}^2/\text{Vs}$  [32, 33, 34].

The problem here again is to organise these NWs on the surface of a substrate, in order to control their placement and in-plane organisation. For this purpose, fluidic methods based on



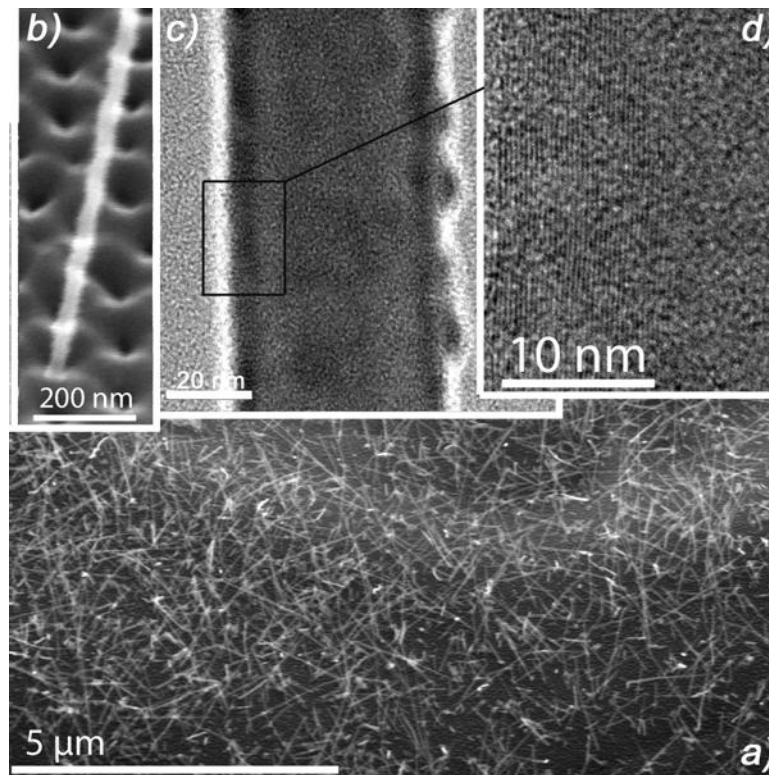
the use of Langmuir-Blodgett films have been developed [35], but they do not provide end-to-end registration.

We are currently developing a novel template-based method for the collective organisation of nanowires [36, 37]. This method makes extensive use of porous anodic alumina as a template material. However, the pores are synthesised parallel to the surface of the substrate (instead of perpendicular as usually done), which facilitates the contacting operations for a three terminal device (planar-type technology). Once the lateral template synthesised, the bottom of the pores can be filled with gold catalyst particles (using an electrodeposition process, fig. 4-c) and the VLS growth of Si NWs can subsequently be achieved inside the pores (fig. 4-d). Figure 4 summarises the overall process (see refs. 36 & 37 for details).



**Figure 4:** Major process steps used for the fabrication of lateral templates based on porous anodic alumina, followed by VLS growth of semiconductor nanowires. The bottom sketch (e) shows a planar TFT structure making use of the nanowires after their growth inside the lateral template.

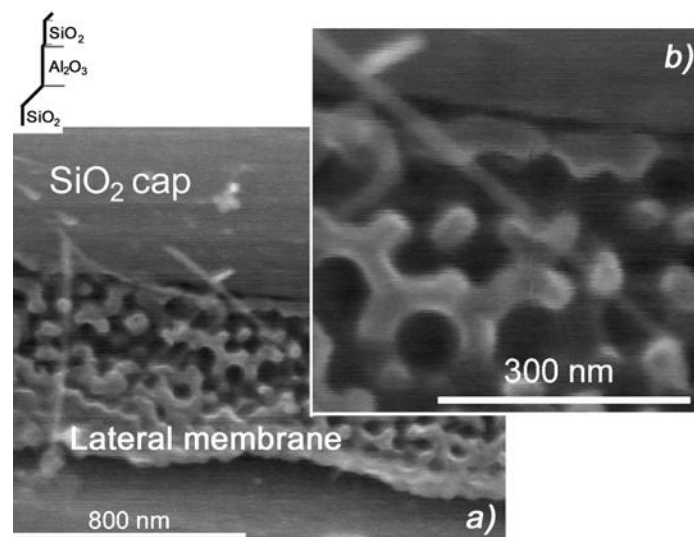
The feasibility of the VLS growth of Si NWs inside the pores of anodic alumina has already been shown for vertical templates [37, 38]. Figure 5 shows Si NWs grown in such a way..



**Figure 5:** (a): top view of Si nanowires grown in a vertical anodic alumina membrane. For easy observation, the growth time has been prolonged purposely, which results in NWs growing out of the membrane. (b): Close view of a nanowire emerging from a pore. (c) and (d): transmission electron microscope views of a nanowire. Crystallographic planes can be observed on (d).

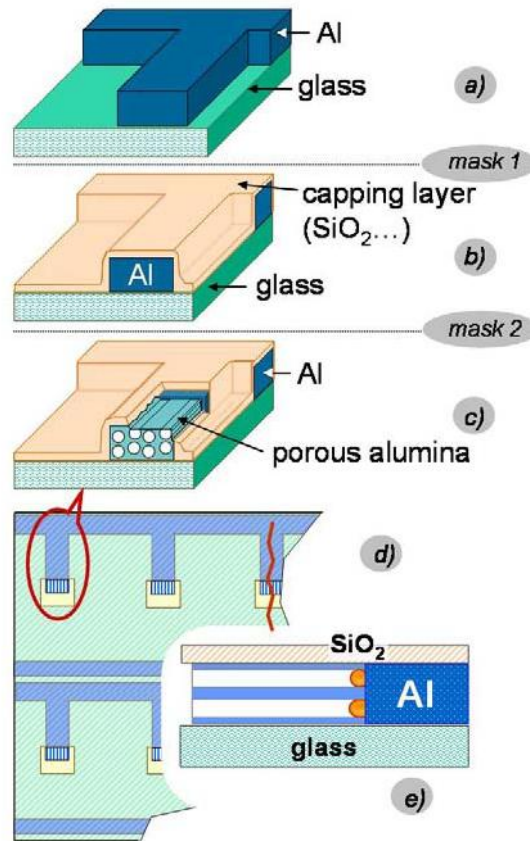
We are now adapting the process to the lateral situation depicted in figure 4-c & d. In particular, due to the fact that the Au catalyst surface exposed to the growth nutrients (e.g., SiH<sub>4</sub> for Si NW synthesis) is much smaller than for a vertical membrane, large amounts of atomic hydrogen have to be supplied to the deposition area in order to avoid parasitic Si deposition on the membrane. Such parasitic deposition would clog the pores, thus inhibiting further NW growth.

Figure 6 shows a preliminary result of Si NW growth in a lateral anodic alumina membrane. The VLS growth has been performed at 550°C with a mixture of 5% SiH<sub>4</sub> diluted in H<sub>2</sub> at a total pressure of 5mbar for a 100sccm total flow. Clearly, the process is not uniform yet and only few NWs emerge from the lateral membrane. Also, parasitic Si deposition is apparent, particularly on fig. 6-c, which means that the H<sub>2</sub> decomposition rate (which supplies atomic hydrogen) at the growth temperature is too low. We are presently studying the possibility of increasing this decomposition rate by fitting the CVD reactor with a hot tungsten filament, upstream of the deposition zone.



**Figure 6:** Growth of Si NWs in a lateral porous alumina membrane. (a): View of the membrane and SiO<sub>2</sub> cap, with some NWs emerging. (b): close up view of an emerging NW.

The interest of the NW growth method illustrated on figs. 4 & 6 is explained below on figs. 7 & 8, for the fabrication of an AMLCD backplane.

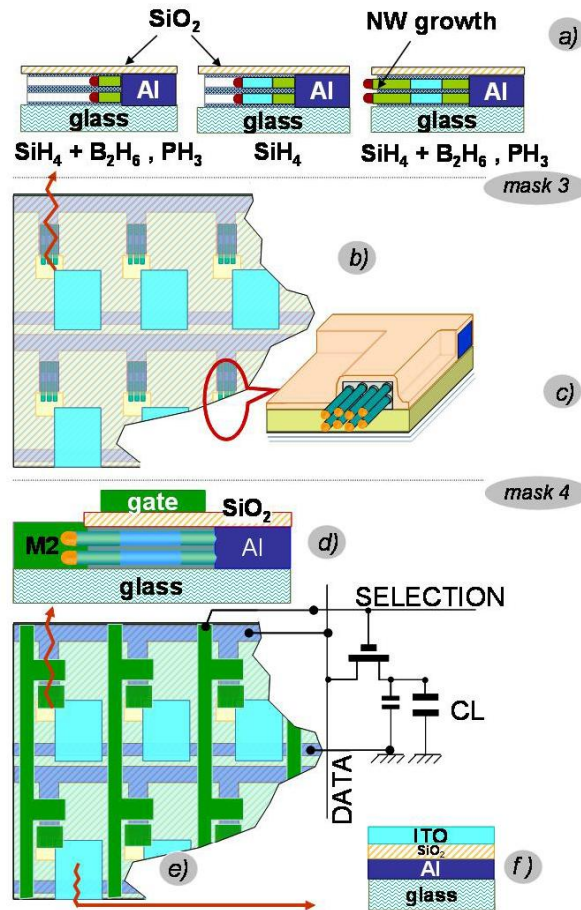


**Figure 7:** The first two masks used for the fabrication of an AMLCD backplane (see text for details).

An Al thin film (data lines) is first deposited and etched (mask # 1), so as to yield a “finger” in each pixel (fig. 7-a, and fig. 7-d which is a top view). The etched Al film is then capped with a deposited insulating layer (*e.g.*,  $\text{SiO}_2$ ). This capping insulating layer is etched (mask # 2) at the tips of the Al fingers in each pixel (figs. 7-b & d). Anodic oxidation of the Al film is then performed locally, at the end wall of the tip of the Al fingers, resulting in the structure shown on fig. 7-c. Gold nanoparticles are then electrochemically deposited (from a salt solution) at the bottom of the pores of the formerly synthesised porous anodic alumina (PAA) fingers (fig. 7-e, cross section).

After completion of the lateral templates and Au electrodeposition, growth of the Si NWs is performed inside the pores of the PAA (fig. 8-a), using sequentially a mixture of  $\text{SiH}_4$  + dopant gas [39] ( $\text{PH}_3$  or  $\text{B}_2\text{H}_6$ , depending on the type of doping desired), pure  $\text{SiH}_4$  and again

a mixture of  $\text{SiH}_4$  + dopant gas. This can be done in only one pump-down operation and results in the structure shown on fig. 8-a.



**Figure 8** : The last two masks used for the fabrication of an AMLCD backplane (see text for details).

An ITO film is then deposited and etched (mask # 3, see fig 8-b, top view), in order to define the pixel area. Finally, the gate metallization (select lines) is deposited and etched (mask # 4, fig. 8-e). Note that the gate metal also connects the drain of the TFT to the ITO of the pixel. For the sake of clarity, figs. 8-d & f show cross-sectional views of the TFT and storage capacitor in each pixel.

We emphasise that only 4 masks are used for the fabrication of the AMLCD backplane and that the TFT structure is fabricated during only one “pump-down” operation, as with the current a-Si:H TFT technology [40].

## CONCLUSIONS

We have reviewed some properties of carbon nanotube random networks and emphasised their interest in the area of active matrix backplanes. We have also presented a novel TFT concept, based on the use of semiconductor (Si, Ge, ..) nanowires and shown its interest for the fabrication of an AMLCD backplane with only 4 masks. This concept can also be applied to AMOLEDs with a reduced mask number, as well as to large area X-ray sensors [41].

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**Figure 8 :** *The last two masks used for the fabrication of an AMLCD backplane (see text for details).*

High temperature growth of SWNTs (HiPCO, Laser, Arc...)  
+ purification

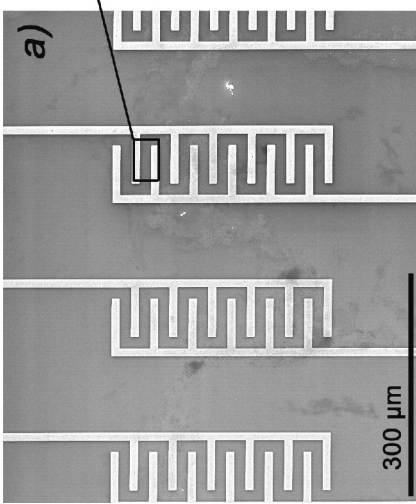
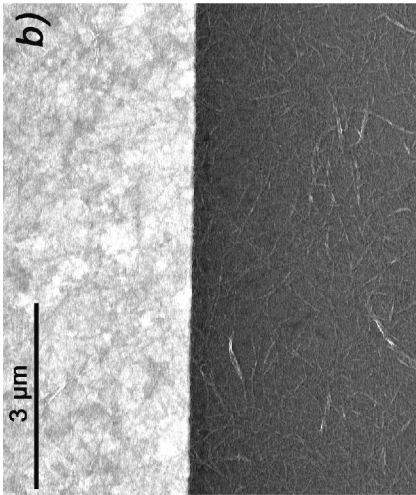
Fabrication of a suspension:

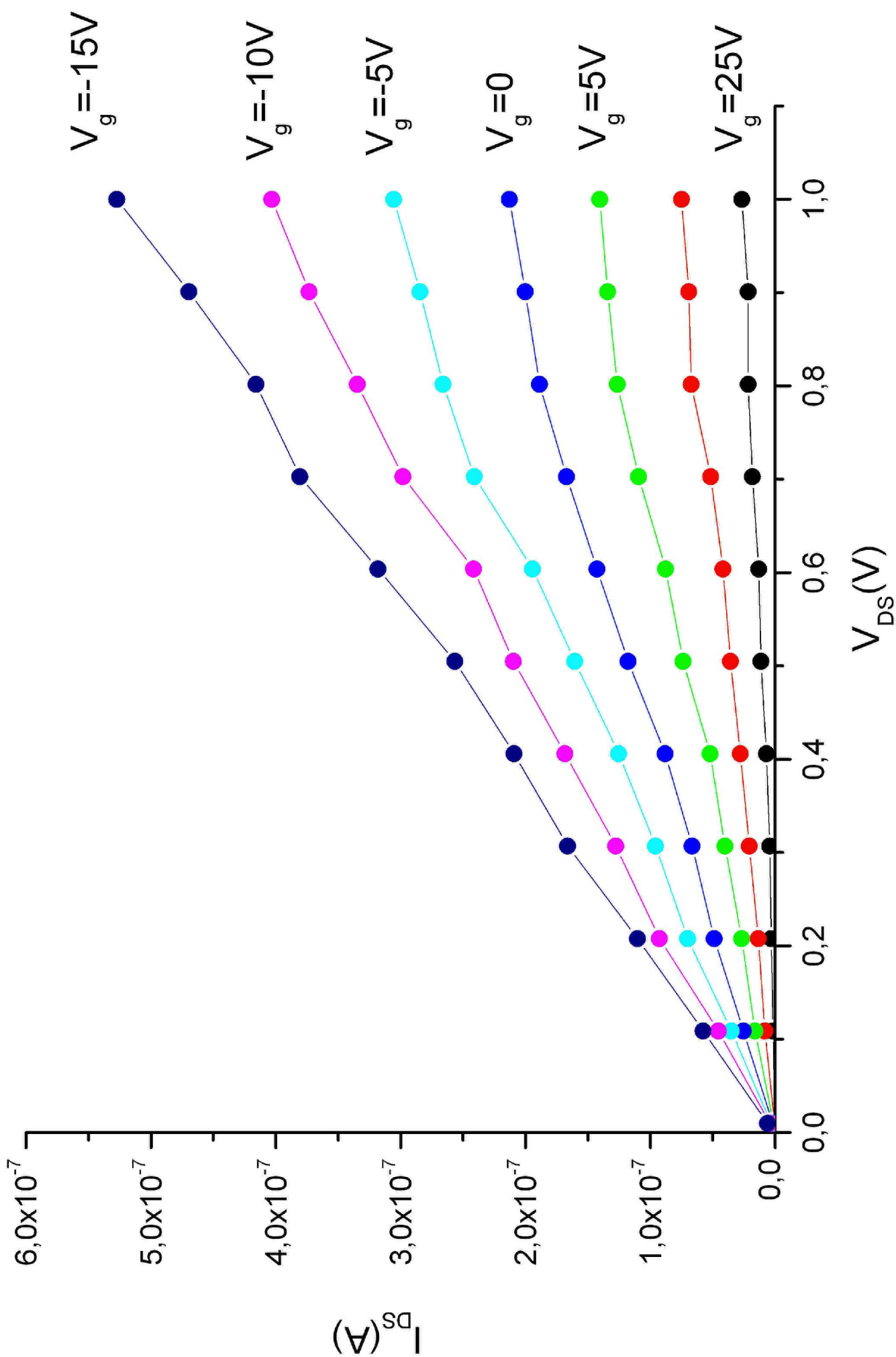
- Choice of solvent / surfactant (H<sub>2</sub>O + SDS, NMP, DMF...)
- Sonication
- Ultra centrifugation
- ...

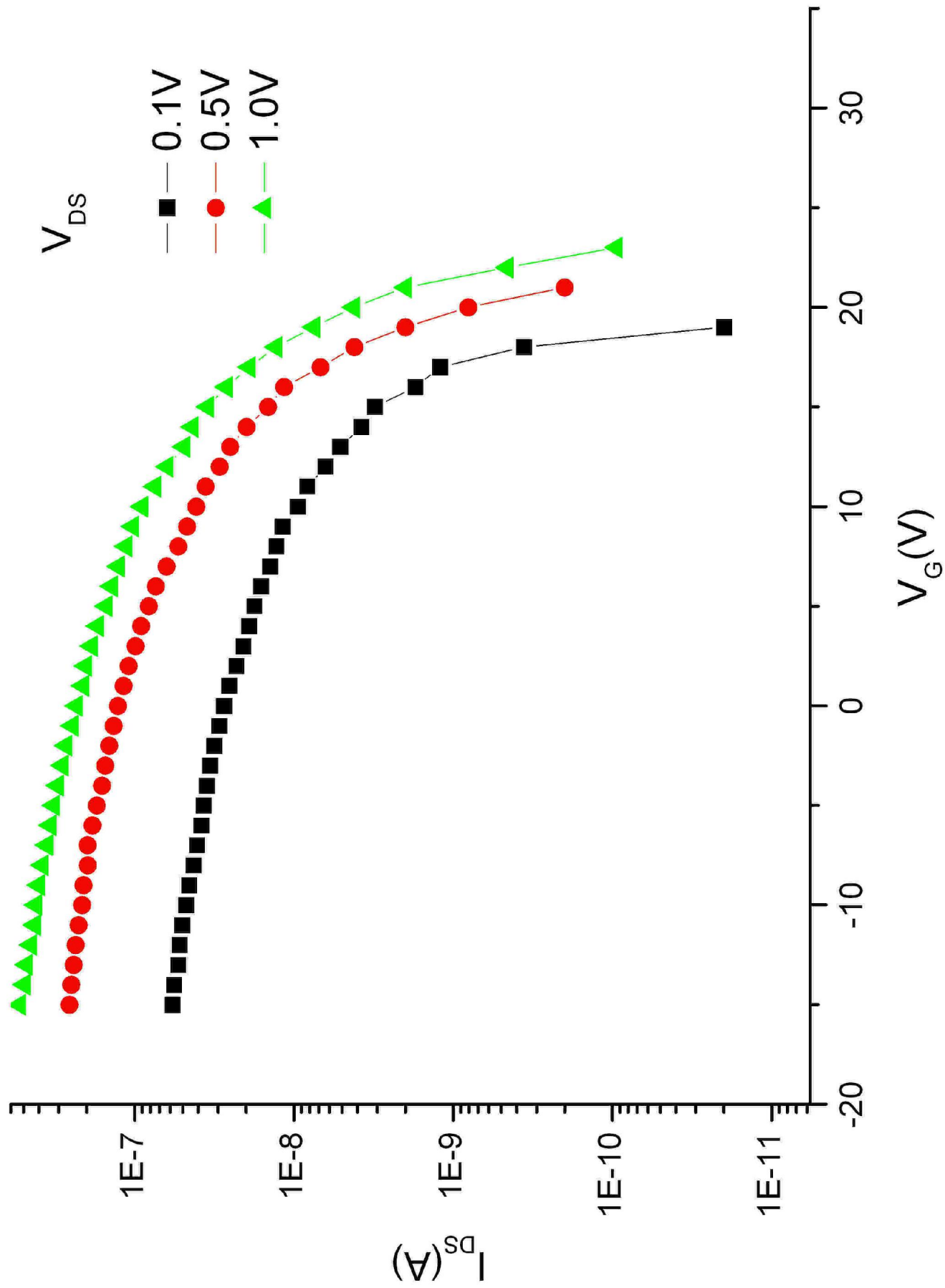
Optimisation of the deposition conditions:

- Filtration
- Spin-on
- Spraying
- Controlled flocculation
- Controlled drying
- ...

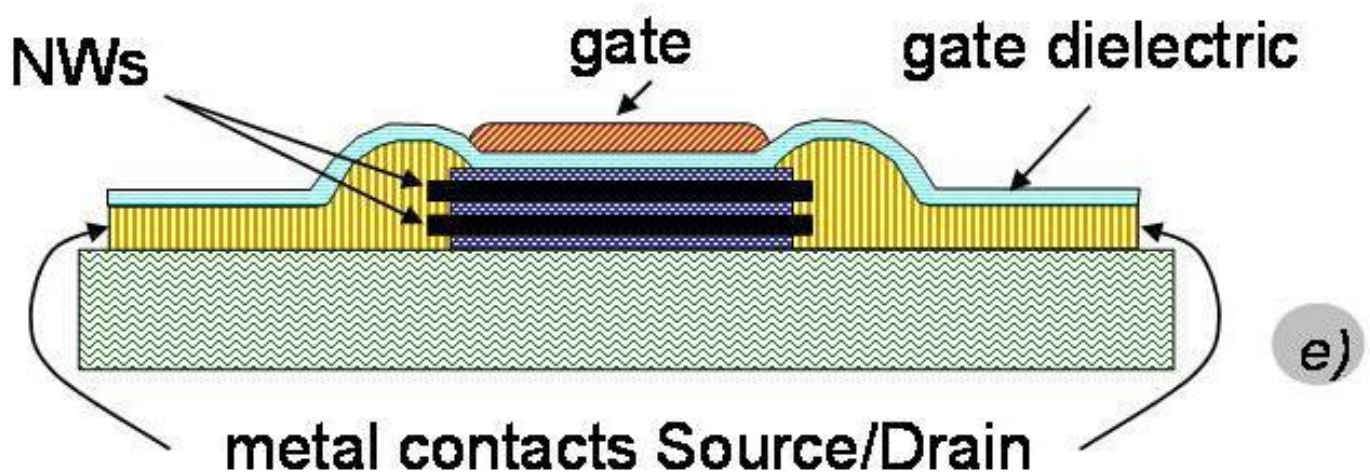
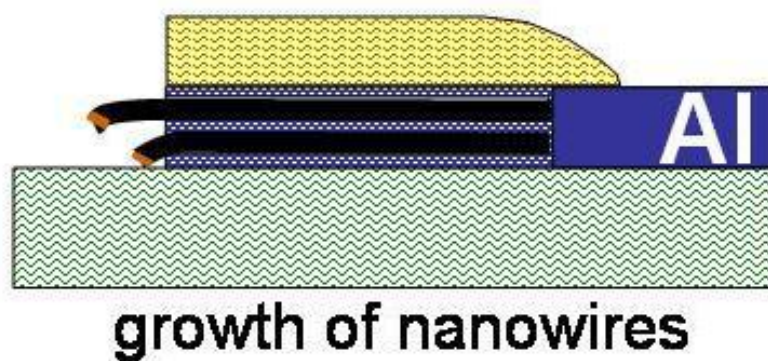
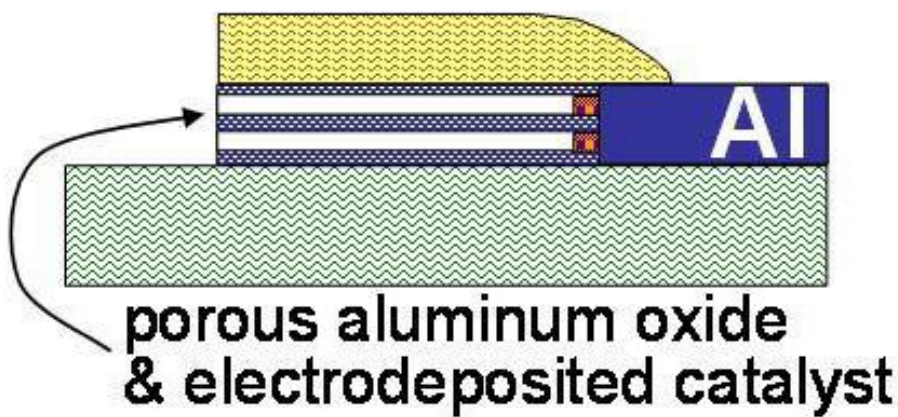
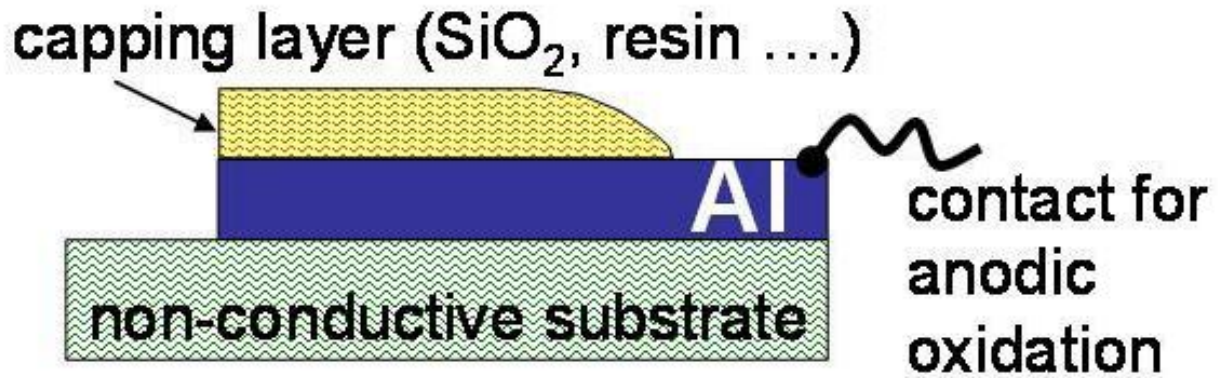
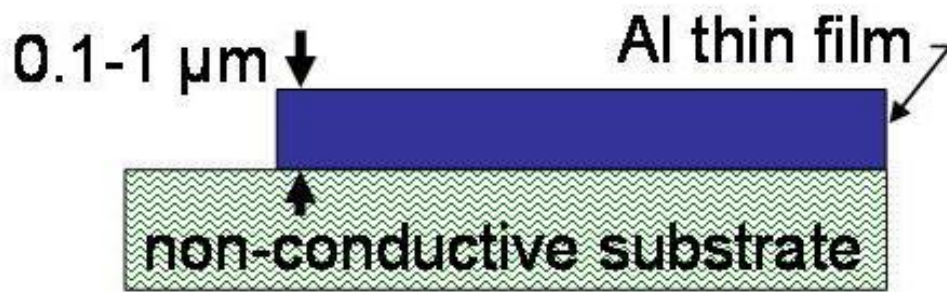
Thickness / density control on the substrate

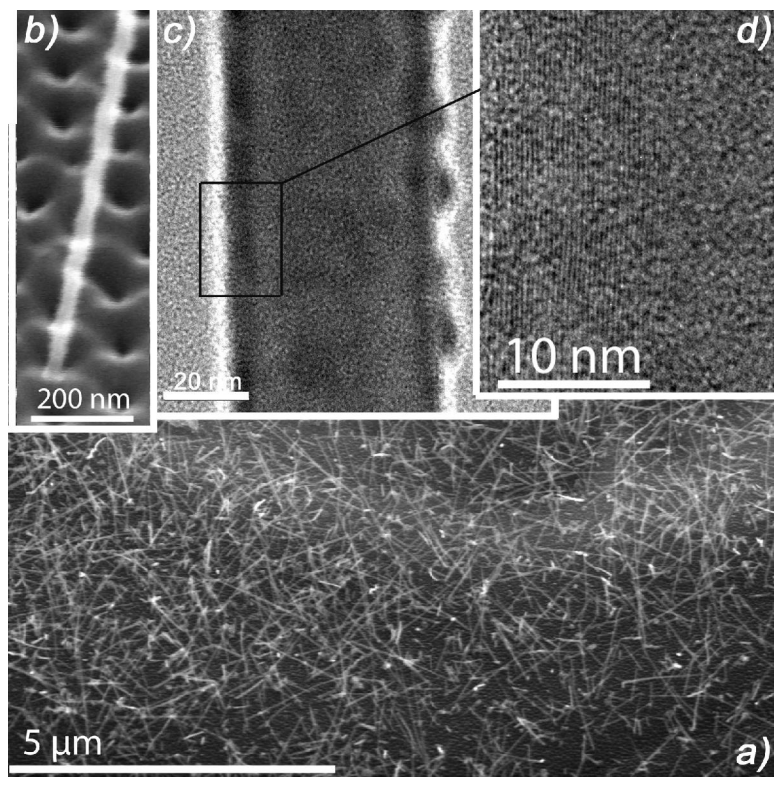


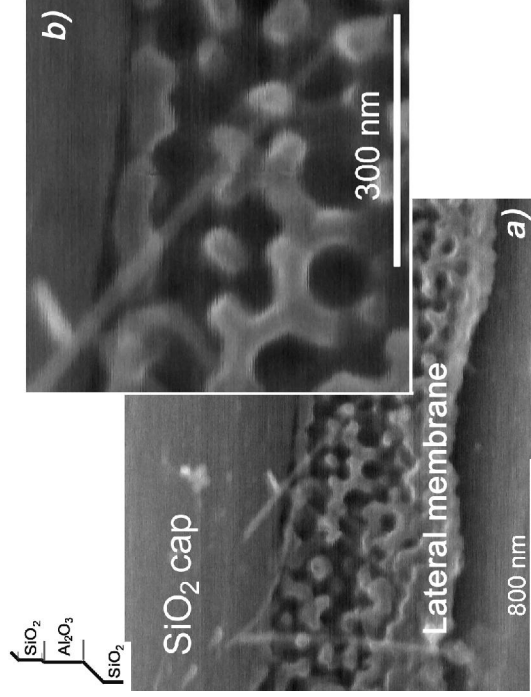


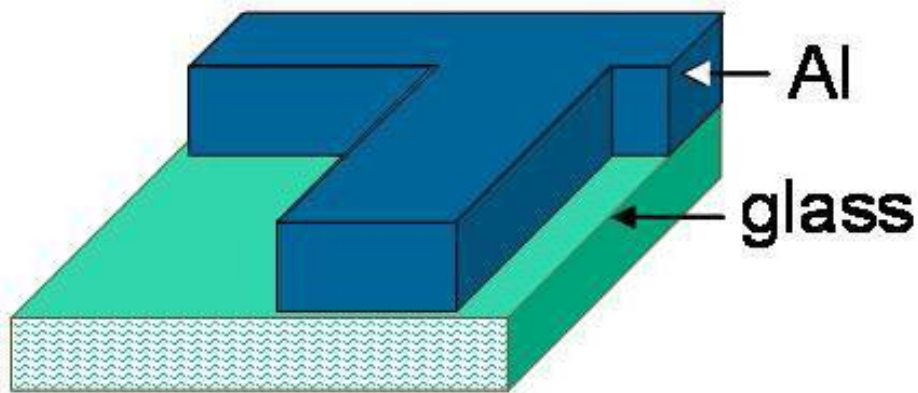






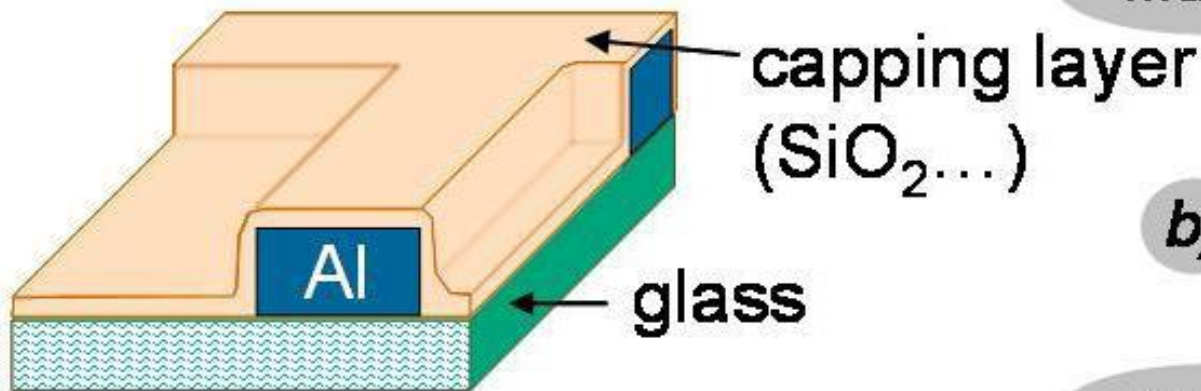






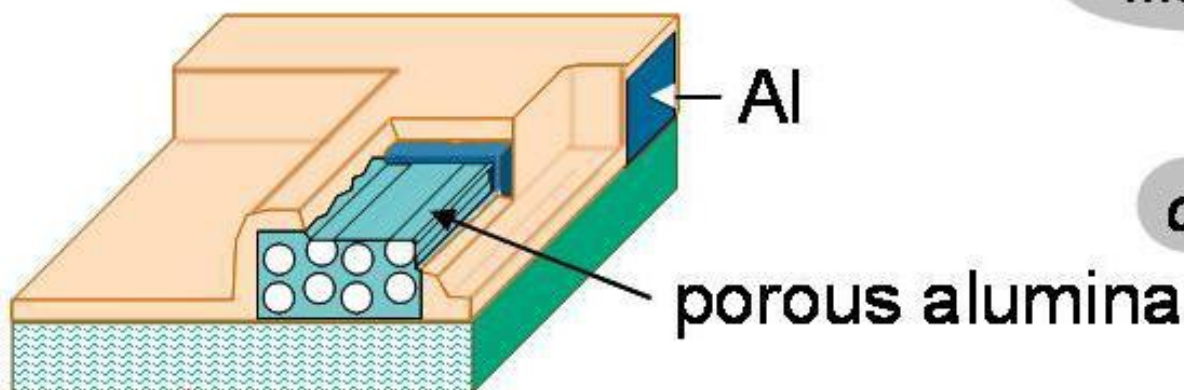
a)

mask 1

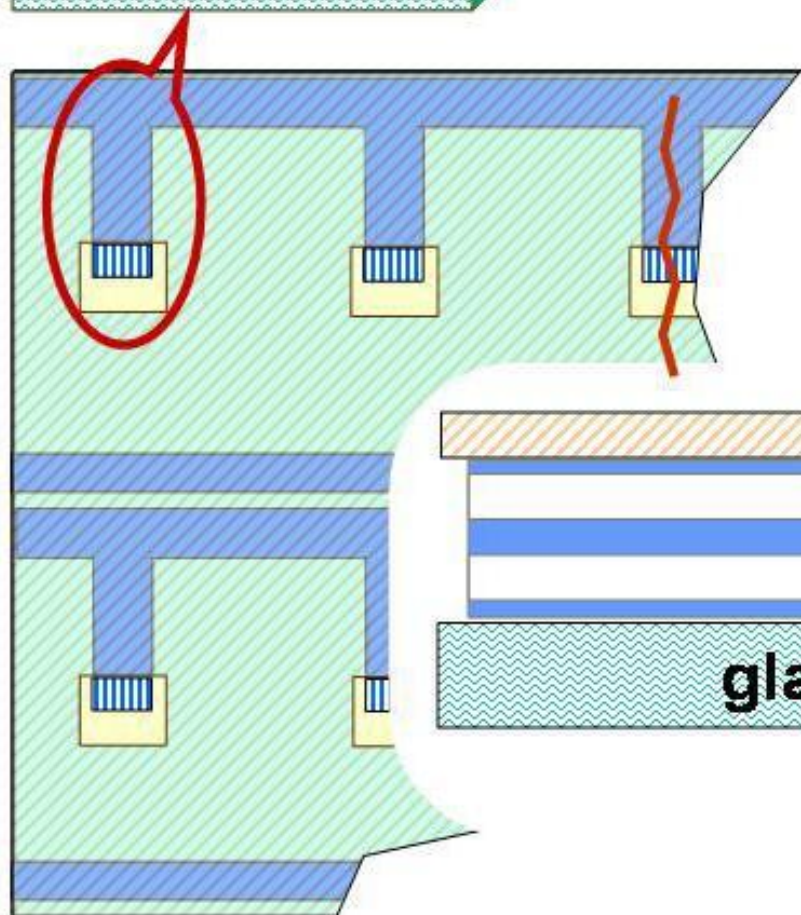


b)

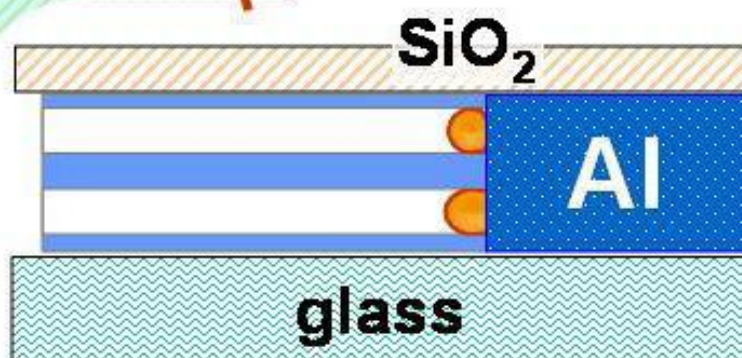
mask 2



c)



d)



e)

