Behavioural EMI Models of Complex Digital VLSI Circuits

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1. ABSTRACT

Increasing EMI potential of high-performance digital circuits like 32bit microcontrollers demand for switching current models and feasible ways to run netlist-based EMI simulations. A promising modelling approach for digital VLSI circuits is presented and a silicon test vehicle for correlation between models and measurements is described.

2. INTRODUCTION

Electromagnetic interference of complex digital circuits like high-performance 32bit microcontrollers cannot be neglected. Especially the automotive industry demands for EMC-improved systems on silicon. Numerous elements and circuits for noise emission reduction have been invented and implemented in microcontrollers. In most cases, this leads to an EMI reduction, but some questions remain open:

- Has the minimum possible EMI been achieved?
- Is this the optimum circuit solution e.g. regarding chip size to reduce EMI?

Since normally no experiments are allowed on product chips, EMI optimization is often a trial and error procedure causing cost which could have been avoided if EMI models and simulation tools had been available during the chip design phase.

This paper describes a modelling approach which is worked on within the European funding project MESDIE in the MEDEA+ frame [10]. It is targeting the generation of simulation models for switching current profiles and realistic power supply system impedance of complex ICs.

The ongoing work towards generation of EMI simulation models on chip level consists of 3 parallel approaches [9]:

- behavioural models of switching currents caused by synchronously clocked gate arrays in digital modules, based on BSIM transistor models,
- backannotation of RLC parasitics of the noise propagation paths, i.e. power supply system,
- proof of correlation between behavioural/RLC models and measurements performed on a test chip.

Figure 1 shows these 3 parallel approaches with:
A = functional modules described by behavioural models of their dynamic current profiles,
B = physical structure of power supply system (noise propagation paths) described by RLC parasitics,
C = test chip for correlation measurements to improve the quality of models A and B.

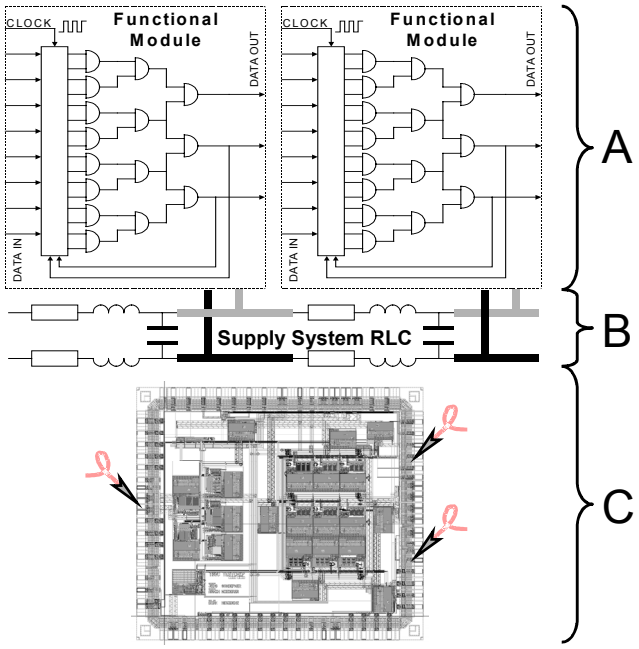

Figure 1: 3-level modelling and measurement approach

Whereas current profiles and power supply models are two desired outcomes of the work, the test chip is required for

ongoing correlation with and quality improvement of the behavioural and RLC models. The test chip "TASC" offers numerous configurable test structures for the on-silicon measurement of switching currents.
The following chapters describe:
3.1) behavioural modelling approach for current profiles,
3.2) parasitic models of power supply structures,
3.3) TASC test chip.

3. EMI MODELLING APPROACH

3.1. Behavioural modelling approach for current profiles

In the world of digital CMOS VLSIs, structures on silicon mean very complex functional modules, which cannot be modelled on transistor level in terms of EMC simulation. Thus behavioural EMC models must be developed which are able to describe the EMI behaviour of CMOS sub-systems or a complete VLSI IC.

To perform a current analysis of a specific CMOS design an extraction of the complete netlist has to be done. Such a "top-down"-approach is voluminous and only be possible if design-data were existing. Behavioural switching current models of single units, or as well as of complex systems, open the possibility to avoid this huge amount of investigations.
In this paper we present a modelling methodology based on an analytical description of the switching current of simple units, having regard to parameters which depend on technology processes. The simplest way to take those parameters into account is the usage of existing transistor models (e.g. BSIM3 or others). The analytic formulation enabled us to have a convenient parameterization of models and therewith an expansion to more complex units or systems.

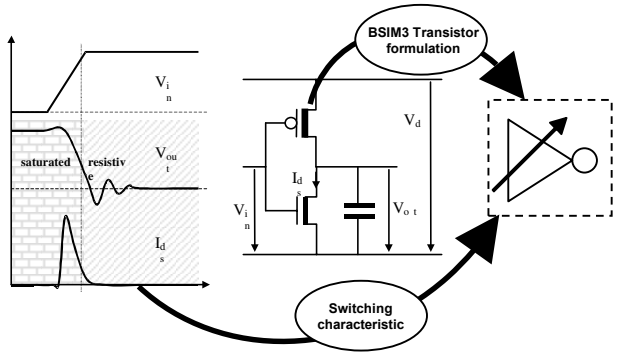

Figure 2: *Modelling of dynamic switching behaviour*

For modelling the switching characteristic of single gates, simple expressions for the transistor currents have been taken into account. The advantage of this procedure is an analytic description of the switching current characteristic. With regard to a simple inverter, both transistors pass through different operation ranges (saturation, resistive and cut off) during one switching phase [1]. As illustrated in figure 3, the overall functional behaviour of an inverter can be separated into five distinct operation areas. The transitions between those ranges are indicated by time crossover points t1 to t4. The transistor operating ranges and therefore the time crossover points are depending on input characteristics and transistor technology.

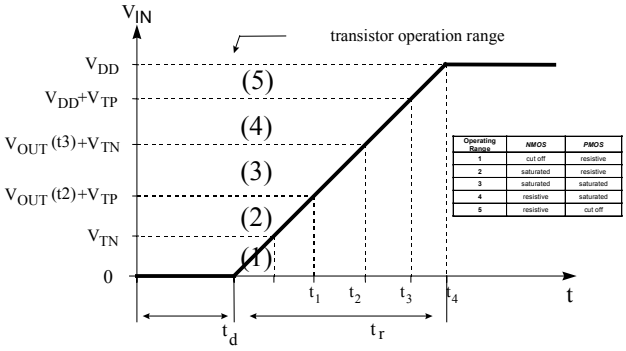

Figure 3: *Transistor operation ranges during one switching phase*

After the calculation of crossover points the related differential equations (DGLs) can be formulated for every range with the help of current balance equations. The validity of each equation is given in each section. The results of these DGLs are not always definite, hence further simplifications have to be made. The complete process of these simplifications cannot be described in this paper.
Fundamentally, the operation ranges are indicated by the crossing of each transistor from one operation range to the next. For example, at t2 the NMOS transistor changes with increasing input voltage (low to high) from saturation to triode area. The analytical relations of transistor currents are summarized:

Saturated: $$I_D = \frac{K}{2} \cdot (V_{GS} - V_{Th})^2$$

Resistive: $$I_D = K \cdot \left[(V_{GS} - V_{Th}) \cdot V_{DS} - \frac{V_{DS}}{2} \right]$$

V_{GS} is the voltage between the gate and the source, which is equal to the input voltage V_{in} , V_{Th} is the threshold voltage, whereas the gain of the transistor is dedicated by $K = \mu_n \cdot C_{ox} \cdot W/L$. The threshold voltage V_{Th} cannot be taken as constant for short channel devices and is rather influenced by effects like the vertical non-uniform doping effect, the lateral vertical non-uniform doping effect or short and narrow channel effects. A detailed description and consideration of these effects on operating current and charge carrier can be found in the BSIM3 models [2]. The equation of the behavioural model can be modified, if these effects are taken into consideration. The main advantage of using the BSIM3-modeling description is, for one, that

technology-related parameters are regarded. Furthermore, a close relation to the simulation of circuits is given, which enables a better integration into the design flow.

The following diagrams depict comparisons between results of numerical simulations of an output driver circuit and the analytical model description of switching current as well as time-related derivation of current (di/dt). A good correspondence is given in both cases.

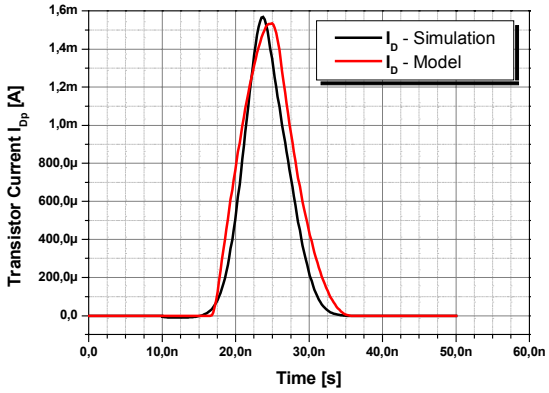

Figure 4: *Model validation for the switching characteristics of an output driver circuit*

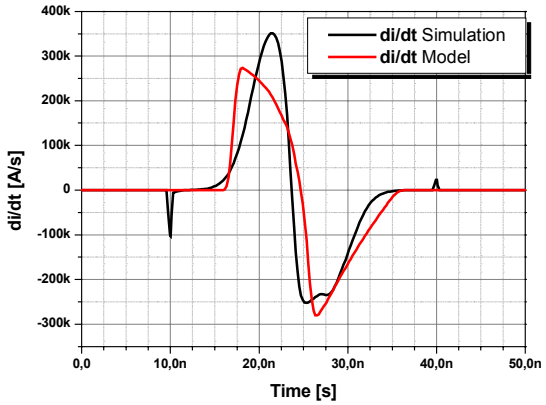

Figure 5: *Model validation for the time-related derivation of current di/dt*

Complex digital modules will be transformed with emphasis on the logical depth topology. The combined gates of one logic depth will be replaced by a parameterized inverter. All these inverters are configured by switching time and fan out load, and can then be simulated by behavioural current-based switching models, as shown in figure 6.
During the project, the mathematical switching description has to be refined by continuous correlation of test chip evaluation results, netlist simulation and behavioural simulation.

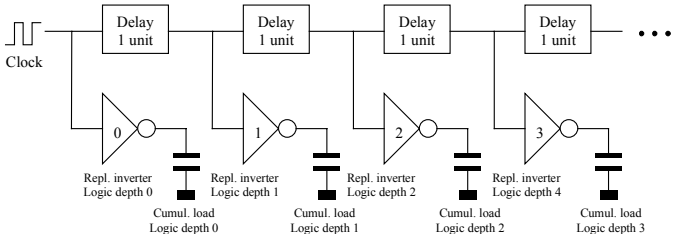

Figure 6: *Modelling methodology for expansion of behavioural models to complex systems*

Since the test chip contains not only complex structures, but also systematic primitive gate arrays, the refinement will start with the primitive arrays until a specific accuracy is achieved. It can then be extended to more complex structures. In a next step, the supply system will be considered by RLC parasitic extraction in the behavioural models as well. Finally the structures will become too complex to be simulated on transistor netlist base. For complete digital CMOS VLSI chips, we must rely on the quality of the behavioural models.

3.2 Parasitic models of power supply structures

For predicting the EMI behavior of an integrated circuit it is necessary to perform an di/dt-analysis. For carrying out such a dynamic current analysis of a specific CMOS design it is absolutely necessary to do at first an extraction of the parasitic elements of the power supply lines.
The parasitic elements in combination with the supply currents cause voltage drops on the supply lines. The static currents cause so called IR-drops at the resistors and the dynamic currents cause voltage drops

$$V = L \cdot \frac{di}{dt} \qquad (1)$$

at the inductors.
This could be validated by performing a circuit simulation of a CMOS gate which is connected to V_{DD} via a supply line (see figure 7). The values for the inverter as well as for the line were taken from a 0.13µm technology process.

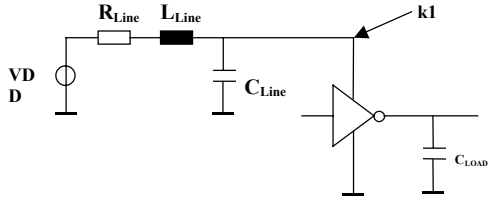

Figure 7: *Simulation model for an CMOS gate connected to a power supply line*

The line length was chosen to be 1mm while the width and height were 1µm and 0.29µm, respectively. This leads to extracted values of R=75ohms, C=81fF and L=1nH. The results in figure 8 show the voltage breakdown at node k1 which was caused by a voltage drop at the line due to the switching current of the inverter.

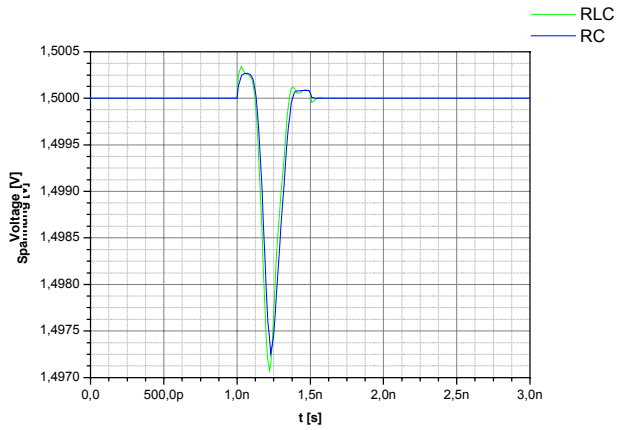

Figure 8: *Voltage drop at node k1 for switching gate from figure 7*

The influence of the parasitic inductance of the supply line could also be seen from the simulation results in figure 8. The simulations were done with (RLC) and without inductance (RC). While

$$\omega L << R \qquad (2)$$

an IC line could be seen as an RC line and the inductance could be neglected. Simulations have shown that rise times of 500ps at a 0.13µm gate cause currents at the supply line with frequency rates up to 2GHz. This brings up the values for ωL of lines as used in current copper based IC technologies in the same range as their resistance R.

The above described results and the fact that the inductance of the line is in the same range as the inductance of bonding wires shows that it is important not only to extract parasitic resistance and capacitance of IC supply lines, but also the parasitic inductance.

For the calculation of the inductance of lines over a lossy substrate at higher frequencies the different occurring propagation modes have to be taken into account. Depending on frequency and substrate resistivity there are three modes of propagation. These modes are slow wave mode, quasi TEM mode and skin effect mode [5]. The slow wave mode occurs at low frequencies and moderate substrate resistivities. It behaves mainly as a shunt resistive element in the transmission line. In the quasi TEM mode the substrate behaves essentially as a dielectric. In the skin effect mode the substrate acts as a lossy conductor with a skin-depth region just below the Si-SiO_2 interface. The three modes of propagation and the transitions between them can be mapped in a frequency-resistivity field as shown in figure 9 (after [5]), where b1 is the thickness of the oxide and b2 represents the thickness of the substrate.
For the automatic extraction of the parasitic resistors and capacitors from the layout data several tools [3], [4] are available at the market.

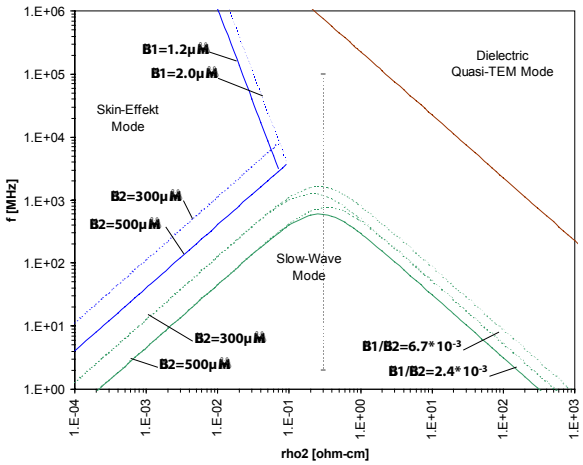

Figure 9: *Representation of the three propagation modes in the frequency-resistivity domain*

For the inductance calculation there are currently no tools available which do an automatic extraction from layout data in a satisfying way.
Within the EMC/EMI modeling approach which is described in this paper, investigations concerning an inductance extraction have been made. Good results have been achieved by using the PEEC method based tool Fast Henry [7]. It leads to sufficient results for lower frequencies where substrate effects don't have to be taken into account.
To take into account the substrate effects, a model is under development which uses substrate current loops to describe the behaviour of the lossy substrate. It is based on a similar model which is described in [6].
A step towards an automation of the extraction process has been done by creating a GDS to Fast Henry interface. This was accomplished by using and adapting the tool Electric. This freeware tool is a VLSI design tool which allows to import GDS-II data and to export Fast Henry simulation decks.

3.3. TASC test chip

3.3.1. Module overview

TASC, the "Test chip for Analysis of Switching Currents", is fabricated in a 130nm CMOS technology and provides numerous test structures for the systematic analysis of on-silicon switching noise generated by synchronously clocked digital logic and propagated through the supply system topology to the supply pads.
Consequently, TASC contains basically 3 test modules, which are located on the test chip according figure 10:

1) EMI Modelling Unit (EMU) with regular and irregular standard cell arrays,
2) Power Routing Unit (PRU) with various local and global supply topologies,
3) Port Switching Unit (PSU) with 16 pad output drivers.

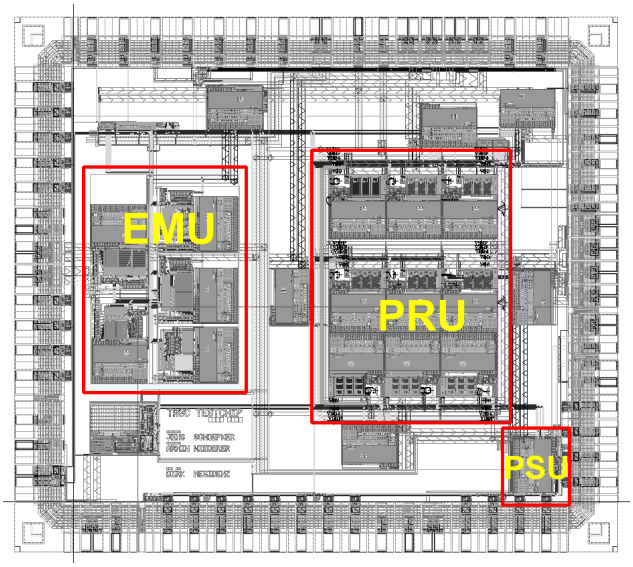

Figure 10: *TASC test chip layout*

The EMU module is intended to verify the behavioural switching current simulation models described in part 3.1. Therefore the module contains similar types of regular and irregular standard gate logic. The standard cell blocks are configurable by number and driver strength of switching gates, logic depth and clock skew. The smallest selectable switching logic consists of only one single gate. To enable on-chip current measurement of only a few switching gates, a high-sensitive current probe was realized on silicon which is described in chapter 3.3.2.
The PRU module is the biggest one since it contains 9 standard cell blocks similar to those in the EMU. The aim of this module is to provide similar logical modules with different power supply concepts. Either single cell blocks can be compared for their different local power supply concepts or one or more cell blocks can be operated simultaneously and compared for different global power supply concepts. Supply systems differ by topology and RC filter devices. The results of the PRU evaluation will be used to correlate the power supply RLC simulation models described in part 3.2 with the measurement results.
The PSU controls up to 16 output pad drivers which can be loaded with additional capacitors off-chip. The pad drivers are configurable by means of driver strength and slew rate control, data output skew and selection of power supply pins. On-chip current sensors sample the dynamic switching currents which can then be compared to the currents measured off-chip. Thus the package influence can be calculated.

Additional functional blocks on the test chip are:
- Clock Generation Unit (CGU) to provide clocks for conducted and radiated emission tests,
- Calibration and Inductance Test Line (CIT) for measurement sensor calibration and on-chip line inductance evaluation,
- Sampling Control Unit (SCU) to control the on-chip voltage and current sampling procedure,
- Test Control Unit (TCU) to set the desired test modes and probing points by the control software running on a PC.

3.3.2. On-chip probing technique

Overall goal of the TASC test chip is to provide accurate time domain measurements of the switching currents in power supply traces for blocks consisting of many digital standard cells. Since the development of behavioural models is based on the BSIM model of single transistors (see chapter 3.1), the logic under test is configurable from only one single switching gate up to several hundred simultaneously switching gates.

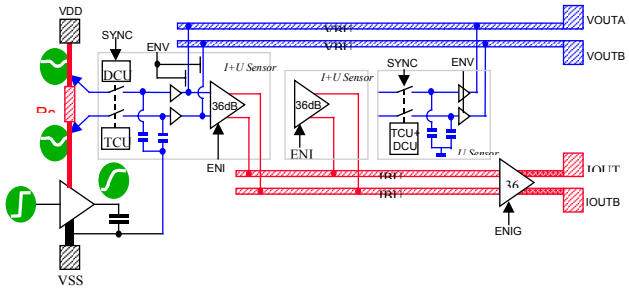

Figure 11: *On-chip current and voltage sensors*

Thus the on-chip current sensor has been designed to provide a sensitivity range from 500µA/V up to 500mA /V. It is built as a differential high gain amplifier configurable from 12dB to 72dB.

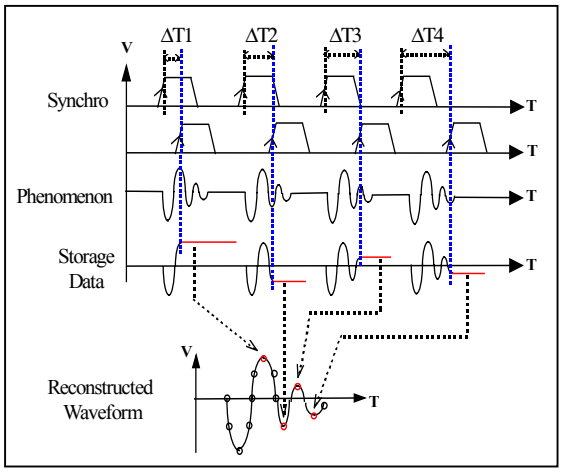

Figure 12: *Phenomenon sampling and waveform reconstruction*

The current is calculated from the voltage drop over small shunt resistors chained into the power supply traces. In addition to the current sensors, also voltage sensors have been located on the test chip to control switching edges and clock skews. Figure 11 shows a schematic diagram of the on-chip sensor circuits.

All on-chip signals are measured by a sampling technique shown in figure 12 [8].
A periodically recurring trigger signal forces the logic to switch, and the resulting switching edge or switching current is sampled on slightly increased time delays. Finally, all gained voltage and current values are combined to recreate the original waveform. Time step resolutions are in the range of single picoseconds, the bandwidth is in the range of several GHz. The complete measurement cycle and waveform reconstruction is controlled by the user interface running on a PC.
While editing this paper, the test chip is processed in the fab. Evaluation is expected to be started in November 2002.

3.3.3. Evaluation setup

The test setup for evaluation consists of:
- the control software running on a PC,
- an interface card providing digital and analog control voltages and receiving analog measurement data,
- the TASC test board,
- the TASC test chip mounted on the test board.

The sampling rate is in the 10kHz range, thus no high-frequent signals need to be transferred between PC and test board. Nevertheless, all analog signals are propagated over 50ohm connectors and coaxial cables.

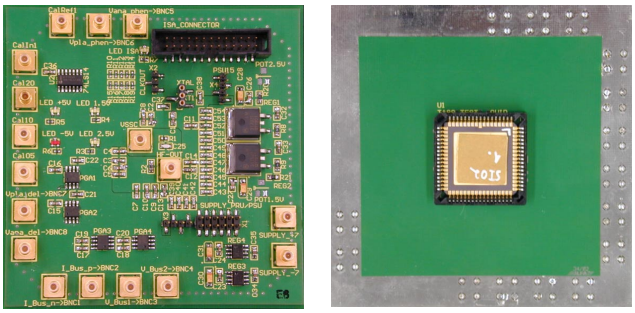

Figure 13: *Top (left) and bottom (right) side of the TASC test board*

The test board is designed to be operated also in frequency domain tests, i.e. for conducted emission (according IEC 61967.4) and radiated emission (according IEC 61967.2). Therefore its border size is fixed to 103mm, and the test chip is mounted on the bottom side of the 4 layer board, shielded by a ground plane from all outside components when facing inside the TEM cell. Top and bottom views of the test board are shown in figure 13.

4. SUMMARY

The digital functional modules of complex chips are reduced to simple "replacement gates" which have similar switching current behaviour as the original full module. In that step some assumptions have to be made, e.g. about the activity level. However, since those current models are mainly to be used for comparison of several power routing schemes, absolutely realistic numbers are not required, e.g. worst case or nominal assumptions can be made.

The RLC parameters of the IC's power routing are back-annotated from the layout and added to the previously derived behavioural models. This new net list can be simulated e.g. with Spice. It is important to include inductances of supply traces in the simulation net list since their physical influence cannot be neglected.

Both behavioural and RLC models have to be correlated with the physical reality. The test chip "TASC" offers regular modules which can be configured in a wide range. Current and voltage sensors are integrated on silicon. Test modes and measurement sequences are controlled by a comfortable software running on a PC. In addition to on-chip measurements in time domain, the conducted and radiated RF noise emission can be measured in frequency domain based on the IEC 61967 standard.

Behavioural models and RLC extractions have already been prepared. The test chip is in fabrication. By end of the year 2002 we will start the test chip analysis and continuously improve the models.
This work is supported by the European joint research project MEDEA+ A509 "MESDIE" [10], which deals with analysis and optimization of electromagnetic compatibility aspects on high-speed and high-density silicon and package designs. In that frame one work package aims at the on-chip EMI modelling. One approach was presented in this paper.

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