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Compact Modeling of Symmetrical Double-Gate MOSFETs Including Carrier Confinement and Short-Channel Effects

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ABSTRACT

A compact model for the drain current and node charges in symmetrical Double-Gate MOSFET, including short-channel and carrier confinement effects is developed. The model is particularly well-adapted to ultra-scaled devices, with short channel lengths and ultra-thin silicon films. An extensive comparison step with 2D quantum numerical simulation fully validates the model. The model is also shown to reproduce with an excellent accuracy experimental drain current measured in Double-Gate devices fabricated with SON process. Finally, the DG model has been successfully implemented in Eldo IC analog simulator, demonstrating the application of the model to circuit simulation.

Keywords: compact modeling, Double-Gate MOSFET, quantum effects, short-channel effects

1. Introduction

Double-Gate (DG) structure has been in the last years the object of intensive research and an impressing number of studies have confirmed its enormous potentiality to push back the integration limits to which conventional devices are subjected [1-4]. The main advantage of this architecture is to offer a reinforced electrostatic coupling between the conduction channel and the gate electrode. In other terms, a double-gate structure can efficiently sandwich (and thus very well control, electrostatically speaking) the semiconductor element playing the role of the transistor channel, which can be a Silicon thin layer or nanowire, a Carbon nanotube, a molecule or an atomic linear chain. The MOSFET operation of such ultimate DG devices with a single quantum conduction channel has been theoretically demonstrated in recent works [5-6].

Although the operation of DG transistor is similar to the conventional MOSFET, the physics of DG MOSFET is more complicated. Moreover, physical phenomena such as 2D electrostatics or carrier quantization have to be considered, since DG structure will be precisely used to design very integrated devices (with short channel and extremely thin films). Therefore, new compact models, dedicated the circuit simulation, have to be developed for DG MOSFET [4]. Several interesting models have been proposed for the classical (i.e. without quantum effects) drain current in long channels DG [3-4, 7-9] or for short channel DG operating in the subthreshold regime [10]. Carrier quantization effects have been considered for the first time in [11]. In this work, we propose a compact model which combines short-channel with quantum-mechanical effects and applies to all operation regimes. In addition the model is continuous over all gate and drain bias range, which makes it very suitable for implementation in circuit simulators. The development is based on the calculation of the 2D potential distribution in the device taking into account the quantum-evaluated inversion charge. A full 2-D quantum mechanical numerical simulation code [12] is used for completely validating the model.

The drain current as predicted by the model is compared with experimental data measured on scaled DG devices fabricated using the SON (Silicon-on-Nothing) process [13-14]. Finally, the drain current model is supplemented by a node charge model and further, the entire DG model is successfully implemented in Eldo IC analog simulator.

2. Drain current modeling

The schematic of a symmetric DG structure and its parameters are shown in Figure 1a. Figure 1b illustrates the band diagrams in an horizontal cross-section together with the first energy subbands. The drain current modelling starts with the calculation of the 2D potential distribution in the DG transistor. For this purpose several methods have been proposed, the most complete being the evanescent-mode analysis, where the potential is divided into two different parts $\Psi(x,y) = \Psi_L(y) + \Psi^*(x,y)$ [15]. The first term represents the long channel solution and the second term takes into account short-channel behaviour. This last term is then approximated by retaining only the lowest-order mode from a Fourier expansion of modes. The method can be very powerful for taking into account short-channel effects in the evaluation of the threshold voltage [15], but the mathematical development is complicated. For simplifying the calculation, in this work we assume the following dependence for the potential:

$$\Psi(x,y) = \Psi_S(x) \times VE(x,y) \qquad (1)$$

where Ψ_S is the surface potential and VE(x,y) is the vertical distribution envelope function. The 2D potential distribution is thus obtained by modulating the surface potential by an envelope function containing the potential dependence in the vertical direction. VE(x,y) is then given by:

$$VE(x,y) = \frac{P(x,y)}{P(x,y=0)} \qquad (2)$$

where P(x,y) is calculated as in [16]:

$$P(x,y) = \psi_0 - \frac{2}{\beta}\ln\left\{\cos\left[\sqrt{\frac{q^2 n_i}{2kT\varepsilon_{Si}}}e^{\frac{\beta(\psi_0 - QFL(x))}{2}}(y - \frac{t_{Si}}{2})\right]\right\} \quad (3)$$

where β=q/kT, QFL(x) is the quasi-Fermi level and ψ_0 are calculated as shown in [16].

For calculating the vertical distribution envelope function VE(x,y), the expression of QFL(x) is needed. An analytical expression of QFL(x) has been proposed in [17] for bulk MOSFET, depending on the x position in the channel, on the channel length and on the drain voltage. However, our detailed investigation by numerical simulation showed that the quasi-Fermi level in DG MOSFET also depends on the gate voltage and on the film thickness. Therefore, we adopted here a quasi-empirical expression (equation 4) inspired from that proposed in [17] and extensively verified by numerical simulation:

$$QFL(x) = \frac{2kT}{q} m \ln\left[\left(\exp\left(-\frac{V_D/m}{kT/q}\right) - 1\right)\left(\frac{x}{L}\right)^{\frac{c}{V_G - V_{FB}}} + 1\right]^{-1} \times (at_{Si})^{\frac{V_D}{3c}} \quad (4)$$

where $m = 2 + b(V_G - V_{FB})$, $a = 0.2nm^{-1}$, $b = 7.5V^{-1}$ and $c = 1V$.

The last term to be calculated for obtaining the 2D potential distribution is the surface potential $\Psi_S(x)$. As presented in [18], for obtaining the expression of $\Psi_S(x)$ the Gauss's law is applied to the particular closed surface shown in Figure 1a:

$$-E(x)\frac{t_{Si}}{2} + E(x+dx)\frac{t_{Si}}{2} - E_S(x)dx = -\frac{qN_A t_{Si}dx}{2\varepsilon_{Si}} - \frac{Q_i(x)dx}{2\varepsilon_{Si}} \quad (5)$$

where E(x) is the electric field, $E_S(x)$ is the surface electric field at the Si/SiO_2 interface and N_A is the channel doping. $Q_i(x)$ is the inversion charge density in the x point of the channel, calculated by the integration of the electron charge over the Si film thickness. In the right hand side of equation (5), the first term corresponds to the depletion charge and the second term corresponds to the mobile inversion charge.

In has been shown in reference [13] that for very thin films (<15nm), the electric field E(x) in equation (5) can be approximated as:

$$E(x) \approx -\frac{d\Psi_s(x)}{dx} \tag{6}$$

The following equation can also be written for the electric field:

$$\frac{-E(x)+E(x+dx)}{dx} = \frac{dE(x)}{dx} \tag{7}$$

In equation (10), the surface electric field at the interface Si/SiO_2, $E_S(x)$, is obtained from the boundary conditions at the interface:

$$V_G - V_{FB} = \frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox} E_s + \Psi_s + \phi_F \tag{8}$$

where V_{FB} is the flat-band voltage and ϕ_F is the Fermi potential. Replacing (6) in (7) and then in (5) and using (8), we obtain the following differential equation for the surface potential Ψ_S:

$$\frac{d^2\Psi_s}{dx^2} - \frac{2C_{ox}}{\varepsilon_{Si} t_{Si}} \Psi_s = \frac{1}{\varepsilon_{Si} t_{Si}} \left[qN_A t_{Si} - 2C_{ox}(V_G - V_{FB} - \phi_F) + Q_i \right] \tag{9}$$

An approximative analytical solution of equation (9) is given by:

$$\Psi_s(x) = C_1 \exp(m_1 x) + C_2 \exp(-m_1 x) - \frac{R(x)}{m_1^2} \tag{10}$$

with C_1, C_2, m_1 and R(x) calculated for filling the boundary conditions $\Psi_S(x=0)=\phi_S$ and $\Psi_S(x=L)=\phi_S+V_D$:

$$C_{1,2} = \pm \frac{\phi_S[1-\exp(\mp m_1 L)] + V_D + R(0)\dfrac{1-\exp(\mp m_1 L)}{m_1^2}}{2\sinh(m_1 L)} \tag{11}$$

$$R(x) = \frac{qN_A t_{Si} - 2C_{ox}(V_G - V_{FB} - \phi_F) + Q_i(x)}{\varepsilon_{Si} t_{Si}} \tag{12}$$

$$m_1 = \sqrt{2C_{ox}/(\varepsilon_{Si} t_{Si})} \tag{13}$$

$$\phi_S = (kT/q)\ln\left(N_A N_{SD}/n_i^2\right) \tag{14}$$

The evaluation of R(x) requires to know the value of the inversion charge density $Q_i(x)$, which can be calculated in two different cases: (a) the "classical" case, i. e. without quantum confinement effects and (b) the quantum case. In the classical case, the inversion charge is given by the following equation, assuming a Boltzmann distribution for the carriers in the channel:

$$Q_i(x) = \int_0^{t_{Si}} q\, ni\, e^{\frac{q}{kT}[(\Psi(x,y)-QFL(x))]} dy \qquad (15)$$

In the quantum case, the inversion charge $Q_i(x)$ is given by:

$$Q_i(x) = \frac{qkT}{\pi\hbar^2} \sum_{l,t} \sum_{i} m_{2D}^{t,l} g_{t,l} \times \ln\left[1 + \exp\left(-\beta\left(\xi_{l,t}^{i} + \frac{E_g}{2} - \Psi_S(x) + QFL(x)\right)\right)\right] \qquad (16)$$

where $m_t^*=0.19\times m_0$, $m_l^*=0.98\times m_0$, $g_l=2$, $g_t=4$, $\beta=q/kT$, $m_{2D}^{l} = m_t^*$, $m_{2D}^{t} = \sqrt{m_l^* m_t^*}$. In equation (16) $\xi_{l,t}^{i}$ are the energy levels calculated using a standard method for first-order perturbation applied to the energy levels of an infinite rectangular well (as shown in [13]):

$$\xi_{l,t}^{i} = (\xi r)_{l,t}^{i} + \Delta\xi^{i} \qquad (17)$$

where $(\xi r)_{l,t}^{i}$ are the energy levels of an infinite rectangular well. $(\xi r)_{l,t}^{i}$ is given by the well-known equation:

$$(\xi r)_{l,t}^{i} = \frac{\hbar^2 \pi^2 i^2}{2q m_{l,t}^* t_{Si}^2} \qquad (18)$$

and

$$\Delta\xi^{i} = \left\langle \varphi^{i} \middle| H \middle| \varphi^{i} \right\rangle \qquad (19)$$

where H is the Hamiltonian of the perturbation and ϕ^i are the electron wave functions associated to energy levels $\xi_{l,t}^{i}$. In equation (11), R(0) is calculated considering $Q_i(0)$ given by equation (15) or (16) with $\Psi_S(0)=\phi_S$.

Since $\Psi_S(x)$ given by equation (10) depends on $Q_i(x)$, replacing (10) and (17) in (16) leads to an implicit equation on $Q_i(x)$, which is solved numerically for obtaining $Q_i(x)$. Finally, for calculating the drain current in DG MOSFET we express the current density (including both the drift and the diffusion components) as:

$$J = -q\mu n(x,y)\frac{dQFL(x)}{dx} \tag{20}$$

which is then integrated in y and z directions:

$$I_d(x) = \mu W Q_i(x)\frac{dQFL(x)}{dx} \tag{21}$$

Current continuity requires the drain current be independent of x and therefore, integrating equation (21) in x direction from x=0 to x=L gives the final expression of I_D:

$$I_D = \mu\frac{W}{L}\int_0^{V_D} Q_i(x)dQFL(x) \tag{22}$$

In the classical case and considering the Boltzmann distribution for the carriers, equation (21) becomes [10]:

$$I_D = \mu W\frac{kT}{q}\frac{1-\exp(-qV_D/kT)}{\int_0^L \frac{dy}{\int_0^{t_{Si}} qn_i e^{q\psi(x,y)/kT}dx}} \tag{23}$$

3. Model validation by numerical simulation: short-channel, quantum effects and volume inversion

The model was validated by an extensive comparison with quantum numerical simulation using a full 2-D Poisson-Schrödinger code [12]. In a first step, the potential distribution as given by equation (1) has been extensively validated for various structure parameters and biases. An example is shown in Figures 2a, where the surface potential as given by the model for L=50nm and L=10nm is compared with numerical simulation. In Figure 2b, the potential distribution in a vertical cut-line perpendicular to the Si film (in the middle of the channel, y direction) is illustrated. A good agreement is obtained

between the model and the numerical simulation. The variation of the quasi-Fermi level (equation 4) was also validated as presented in Figure 3. Equation (3) has been derived under classical assumptions, but we verified by quantum numerical simulation that this equation still applies in the quantum case.

In a second step, the drain current expression has been completely validated by numerical simulation, for channel lengths varying between 30nm and 200nm and film thicknesses from t_{Si}=15nm down to t_{Si}=2nm. Figure 4 shows an example of this validation step DG MOSFET with different channel lenghts (a constant mobility is considered in equation (22)). Short channel behaviour of the quantum drain current is also checked in Figure 4: the model reproduces very well the simulation (even for L=30nm), in both weak and strong inversion regimes. The extensive investigation of additional $I_D(V_D)$ curves has shown that the model is completely valid in both linear and saturation regimes.

The validation procedure was continued by an in-depth investigation of the model capability to take into account carrier quantization effects. For this purpose the inversion charge density $Q_i(x)$ (in both classical and quantum case) in long and short channels has been compared to numerical results and very good agreement has been found (Figure 5). Further the classical and quantum drain current were calculated as a function of the channel thickness t_{Si}. Figure 6 shows that the quantum model perfectly reproduces two essential phenomena:

(1) the impact of quantum effects quantum effects, increasingly significant when t_{Si} is scaled down. The shift between classical and quantum $I_D(V_G)$ curves increases for thinner Si channels. In the same way, the shift between the classical and the quantum threshold voltage is clearly higher for t_{Si}=2nm than that for t_{Si}=10nm.

(2) the drain current dependence on the channel thickness in the subthreshold region, as a manifestation of the volume inversion, which is a key phenomenon in symmetrical

DG transistors. Above threshold the drain current does not depend much on the Si channel thickness [7].

4. Compact model versus experimental data

Finally, the model was used to fit drain current measured [13-14] on DG devices (Figure 7). The match between experiment and model is very good, especially in the subthreshold regime. Above threshold the model slightly overestimates the current due to the use of a constant mobility and no series resistances. For improving the model accuracy the next step will be to consider a realistic mobility model [19] and to include the effect of series resistances.

The proposed compact model can easily be used to obtain all main performance indicators of DG MOSFET, such as the threshold voltage V_T, the subthreshold swing S, the DIBL (Drain-Induced-Barrier-Lowering) effect on the threshold voltage, the threshold voltage roll-off, I_{on} and I_{off} currents and the CV/I metric. In addition, the model can be directly implemented in circuit simulation software and used for the simulation of DG MOSFET based-circuits, as will be shown in following paragraphe.

5. Model implementation in Eldo™ IC analog simulator

The drain current model presented previously has been implemented in a circuit simulator in order to evaluate the performances of simple DG MOSFET-based circuits. For this purpose, the model was firstly supplemented by a charge model including the expressions of charges on the device terminals. The schematic description of the entire model is given in Figure 8a as well as the symbol of a DG transitor with n-channel. In this figure Q_G is the total charge on the two gates, Q_D is the charge on the drain terminal and Q_S is the charge on the source terminal.

The starting point for calculating the gate charge is the neutrality condition which requires that the total charge in the device be always zero:

$$Q_G + Q_I = 0 \tag{24}$$

In (24) Q_I is the total inversion charge obtained by the integration of relation (16) from 0 to L:

$$Q_I = \int_0^L Q_i(x)dx \tag{25}$$

The gate charge Q_G is then obtained from equation (24). Under normal bias conditions, the inversion charge is not uniformly distributed along the channel except for V_D=V_S. Because of this bias dependence, $Q_i(x)$ contributes differently to the source and drain charges. Various approaches have been proposed for sharing the inversion charge between the source and drain nodes [20-22]. **In our development we have adopted the approach given in [22] and also presented in [18].** At low drain voltage, the inversion charge is equally shared between the source and drain. When the drain voltage increases, the drain charge is strongly reduced and the source charge becomes close to the inversion charge Q_I.

It is important to note that our compact model is completely continuous over all operation regimes and the drain current and node charges equations are derivable and their derivatives are also continuous over all bias regimes. We have also verified that the source and the drain electrodes can be permuted.

The compact model described previously for the n-channel DG transistor (NMOS) has been implemented in Eldo IC simulator. A similar model has been considered for the DG MOSFET with p-channel (PMOS). The model has been used further to simulate DC and transient response of a three-stage inverter chain containing DG MOSFETs (the schematic of this circuit is shown in Figure 8b). The Figure 8c shows the time response of the two outputs voltages (the output voltage of the second and of the third stages) to a

rectangular input voltage. This results demonstrates that the model can be perfectly used to the simulation of small circuit based on DG MOSFETs.

6. Conclusion

In this paper we developped a compact model for the drain current and node charges in symmetrical Double-Gate transistors, including short channel and carrier quantization effects. The model is particularly dedicated to ultra-scaled devices expected at the end-of-the-roadmap. The starting point of the model was the development of an analytical expression for the 2D distribution of the potential considering the quantum inversion charge. An extensive comparison with 2D Poisson-Schrödinger simulation data was conducted in order to fully validate the model. We have shown that the proposed model reproduces with an excellent accuracy the impact on the drain current of short channel effects, volume inversion phenomenon and carrier quantum confinement. A very good agreement was also obtained with experimental data measured on very integrated devices. Finally, the model was implemented in Eldo IC analog simulator and the transient simulation of simple DG CMOS-based circuits has been performed.

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References

[1]. Hisamoto D, Short course IEDM Tech Dig 2003 and references therein.

[2]. D.J. Frank *et al.*, "Monte Carlo simulation of a 30nm dual-gate MOSFET: How short can Si go?", In Proceedings IEDM Tech Dig 1992, p. 553.

[3]. Y. Taur, "Analytic Solutions of Charge and Capacitance in Symmetric and Asymmetric Double-Gate MOSFETs", IEEE Transactions on Electron Devices, **48**(12), p. 2861-2869 (2001).

[4]. M. Chan *et al.*, "Quasi-2D Compact Modeling for Double-Gate MOSFET", in Proceedings MSM 2004, p. 108-13.

[5]. M. Bescond *et al.*, "Atomic-scale Modeling of Source-to-Drain Tunneling in Ultimate Schottky Barrier Double-Gate MOSFET's", in Proceedings ESSDERC, p. 395 (2003).

[6]. M. Bescond *et al.*, "Atomic-scale modeling of Double-Gate MOSFETs using a tight-binding Green's function formalism", Solid-State Electronics **48**, p. 567 (2004).

[7]. Y. Taur *et al.*, "A Continuous, Analytic Drain-Current Model for DG MOSFETs", IEEE Electron Device Letters, **25**(2), p. 107-109 (2004).

[8]. D. Jiménez *et al.*, "Continuous Analytic I–V Model for Surrounding-Gate MOSFETs", IEEE Electron Device Letters, **25**(8), p. 571-573 (2004).

[9]. A. Ortiz-Conde *et al.*, "Rigorous analytic solution for the drain current of undoped symmetric dual-gate MOSFETs", Solid State Electronics, **49**, p. 640-649 (2005).

[10]. X. Liang and Y. Taur, "A 2-D Analytical Solution for SCEs in DG MOSFETs", IEEE Transactions on Electron Devices, **51**(8), p. 1385-1391 (2004).

[11]. G. Baccarani and S. Reggiani, "A Compact Double-Gate MOSFET Model Comprising Quantum-Mechanical and Nonstatic Effects", IEEE Transactions on Electron Devices, **46**(8), p. 1656-1666 (1999).

[12]. D. Munteanu and J.L. Autran, "Two-dimensional Modeling of Quantum Ballistic Transport in Ultimate Double-Gate SOI Devices", Solid State Electronics, **47**, p. 1219-1225 (2003).

[13]. S. Harrison *et al.*, "Electrical characterization and modeling of high-performance SON DG MOSFETs", in Proceedings ESSDERC 2004, p. 373-376.

[14]. R. Cerutti *et al.*, "New Design Adapted Planar Double Gate Process for Performant Low Standby Power Application", in Proceedings Silicon Nanoworkshop 2005.

[15]. S-H. Oh *et al.*, "Analytic Description of Short-Channel Effects in Fully-Depleted Double-Gate and Cylindrical, Surrounding-Gate MOSFETs", IEEE Electron Device Letters, **21**(9), p. 445-447 (2000).

[16]. A. Ortiz-Conde *et al.*, "Analytic Solution of the Channel Potential in Undoped Symmetric Dual-Gate MOSFETs", IEEE Transactions on Electron Devices, **52**(7), p. 1669-1672 (2005).

[17]. R.J. Van Overstraeten *et al.*, "Theory of the MOS transistor in weak inversion-new method to determine the number of surface states", IEEE Transactions on Electron Devices, **22**(5), p. 282-288 (1975).

[18]. X. Loussier *et al.*, "Compact model of drain-current in Double-Gate MOSFETs including carrier quantization and short-channel effects", in Proceeding MSM 2006.

[19]. M. Alessandrini *et al.*, "Development of an analytical mobility model for the simulation of ultra-thin single- and double-gate SOI MOSFETs", Solid-State Electronics, **48**, p. 589-595 (2004).

[20]. J.A. Robinson *et al.*, "A general four-terminal charging-current model for the insulated-gate field-effect transistor—I", Solid-State Electronics, **23**, p. 405-410 (1980).

[21]. C. Turchetti *et al.*, "On the small-signal behaviour of the MOS transistor in quasistatic operation", Solid-State Electronics, **26**, p. 941-948 (1983).

[22]. Y.P. Tsividis, Operation and modeling of the MOS transistor. 2nd ed. Boston: McGraw-Hill, 1999.

Figure captions

Figure 1. (a) Schematic of symmetrical DG MOSFET structure and its electrical and geometrical parameters considered in this work; the dashed area shows the closed surface for the application of the Gauss's law; (b) Band diagram in a vertical cross-section in the channel and definition of the different parameters used in the model development.

Figure 2. (a) Surface potential variation along the channel from source to drain for L=50nm and L=100nm (t_{Si}=5nm, V_D=0.4V). (b) Potential variation the y direction for differents channel doping levels (t_{Si}=10nm, V_G=0.6V). Comparison between compact model and numerical simulation.

Figure 3. Variation with x of the normalized quasi-Fermi level QFL/V_D for L=200nm **(intrinsic channel)** at low and high drain voltage.

Figure 4. Drain current in long and short channel DG transistors as calculated by model in the quatum case and validation by numerical simulation (t_{Si}=10nm, t_{ox}=1nm, midgap gates, **intrinsic channel**, V_D=0.1V).

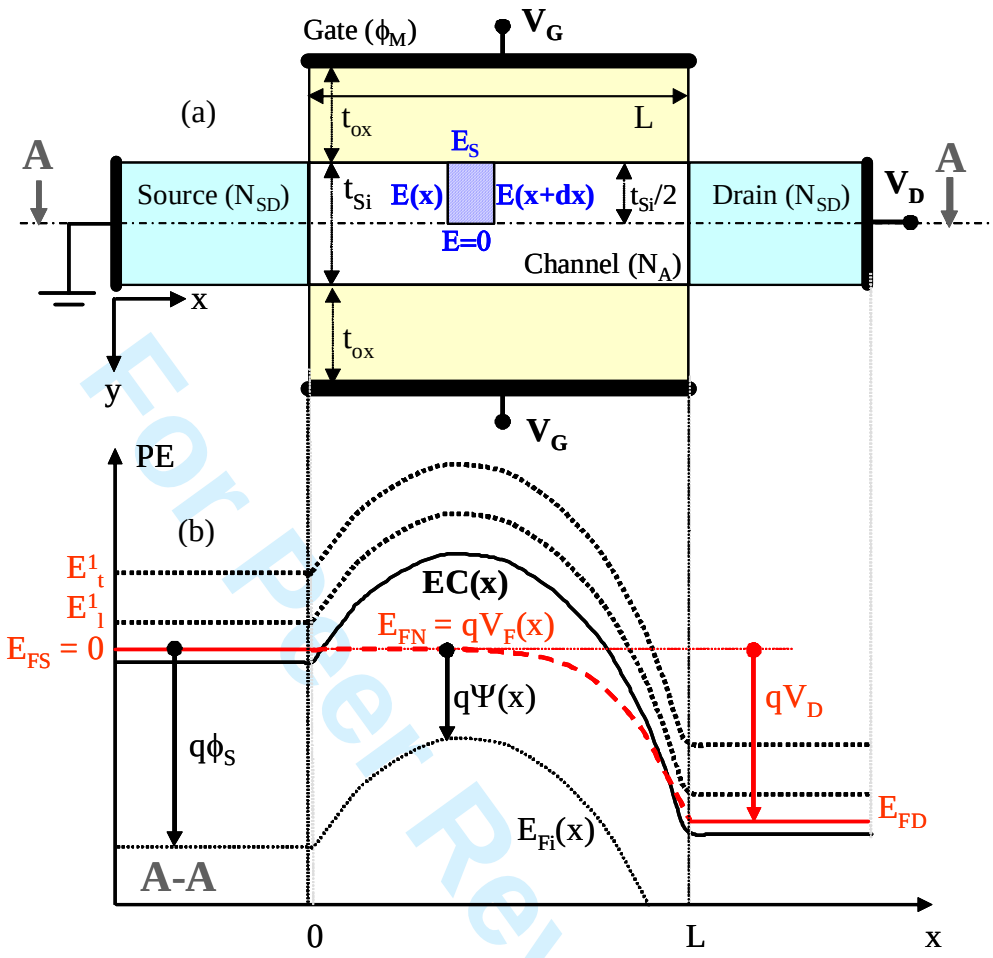
Figure 5. Variation of the inversion charge density $Q_i(x)$ along the channel from source to drain in the classical and quantum mechanical cases: (a) L=200nm; (b) L=50nm. Other parameters are: t_{Si}=5nm, V_G=1V, V_D=0.4V, **intrinsic channel**.

Figure 6. Impact of film thickness on the subthreshold operation of L=50nm DG transistor: the model perfectly reproduces quantum effects and volume inversion

(t_{ox}=1nm, midgap gates, **intrinsic channel**). The drain current calculated in the classical case is also shown.

Figure 7. Compact model versus experimental data measured on DG transistors fabricated with the GAA/SON process described in references [13-14].

Figure 8. (a) Schematic description of the DG model implemented in Eldo IC analog simulator and definition of the node charges. The symbol of a DG MOSFET with n-channel is also represented. (b) Schematic of a three-stage inverter chain containing DG MOSFETs with n- and p-channels. (c) Transient analysis of the three-stages inverter chain shown in figure (b) and simulated using the model: response to a rectangular input voltage V_{IN}. The parameters of DG transistors are: L=50nm, t_{Si}=10nm, t_{ox}=1.5nm, intrinsic channel and midgap gates.



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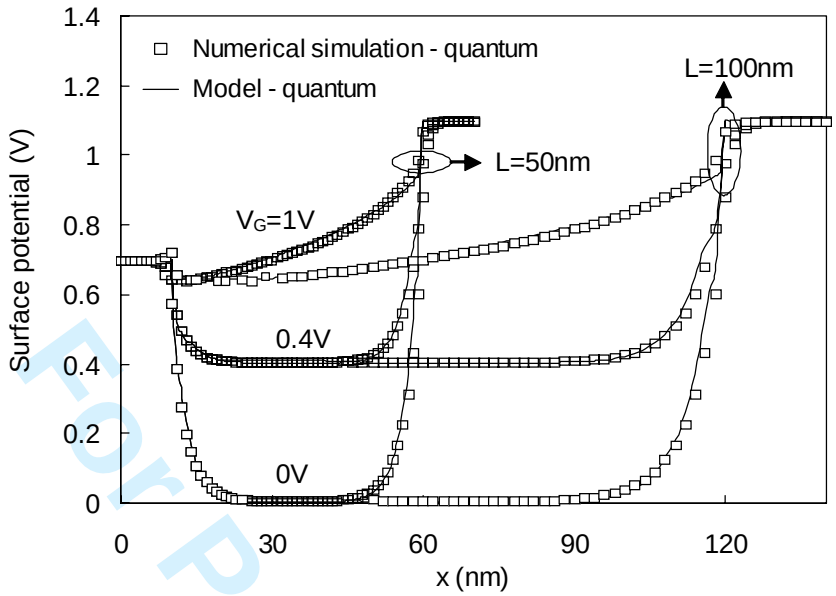

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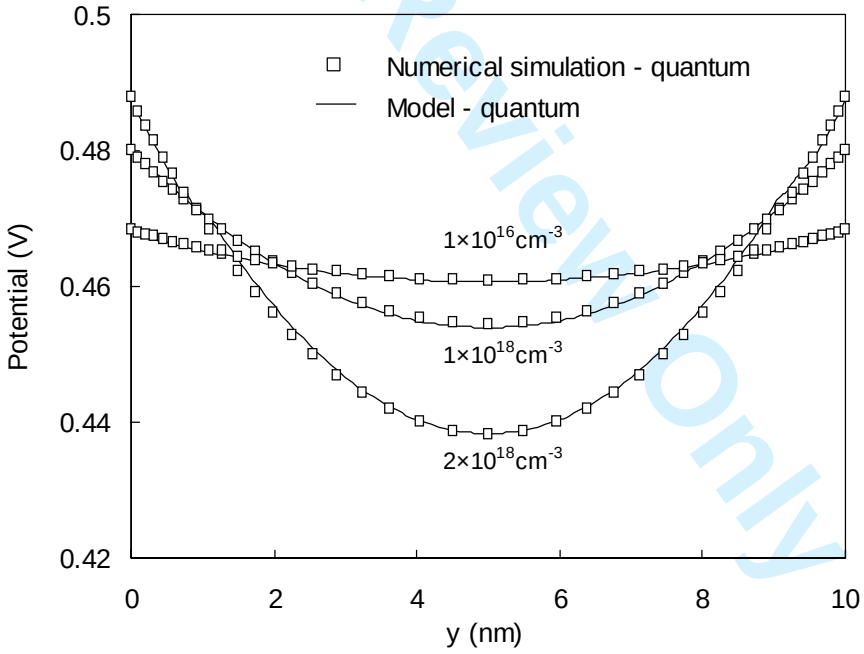

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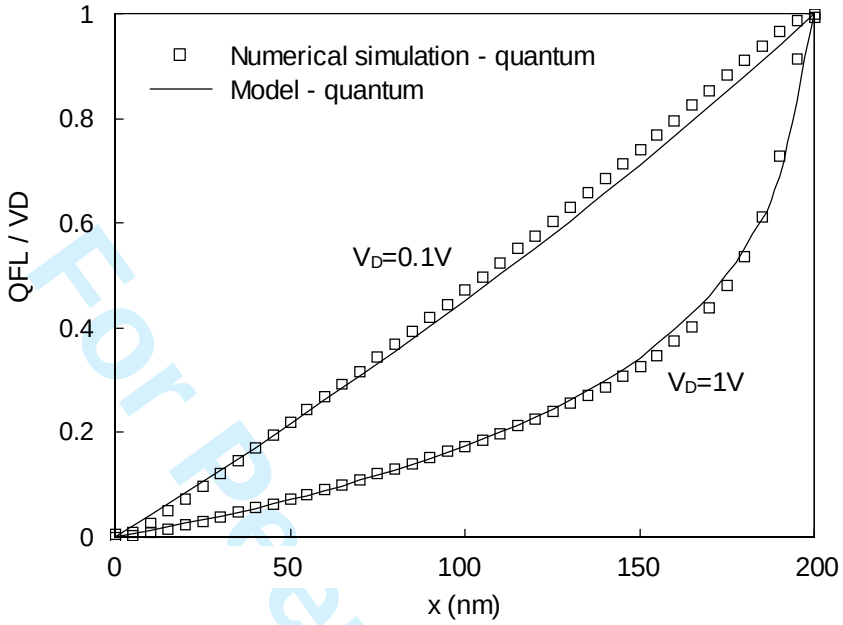

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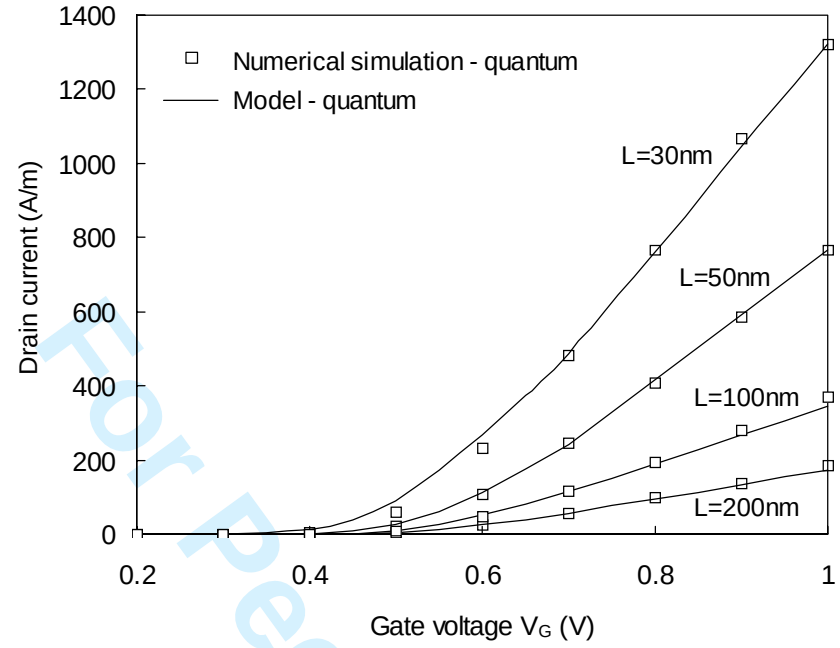

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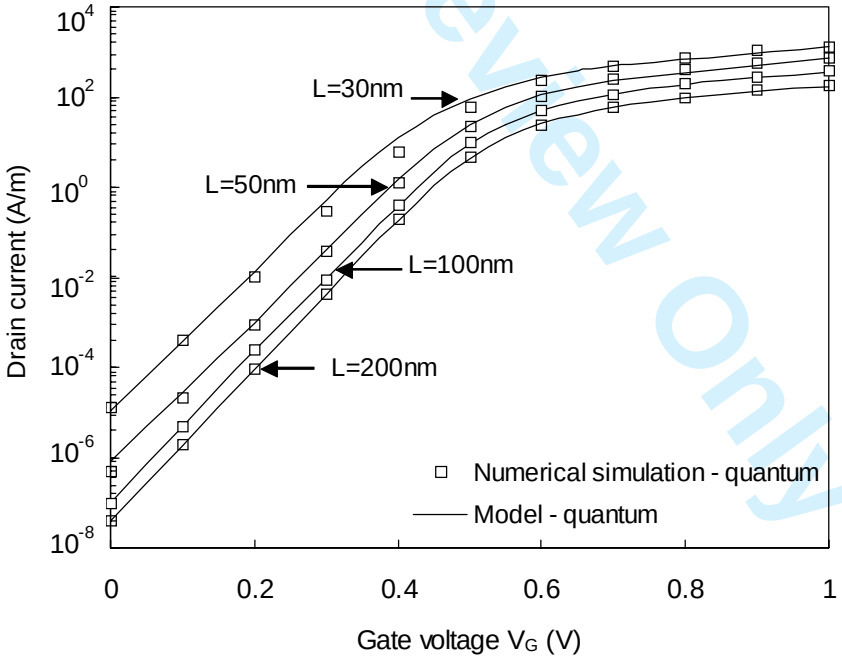

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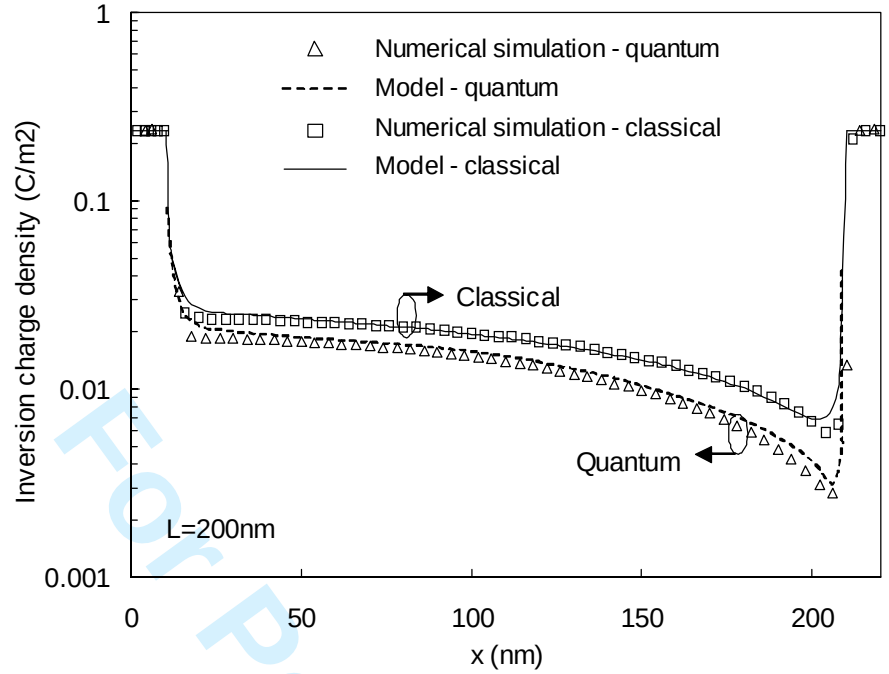
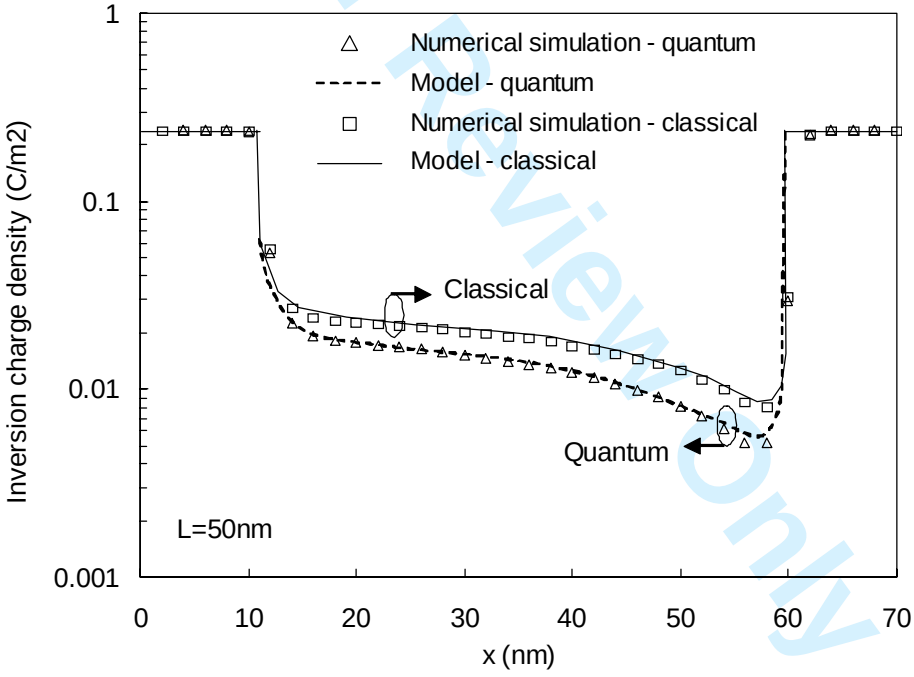
Figure 4. Munteanu et al.



(a)



(b)

Figure 5. Munteanu et al.

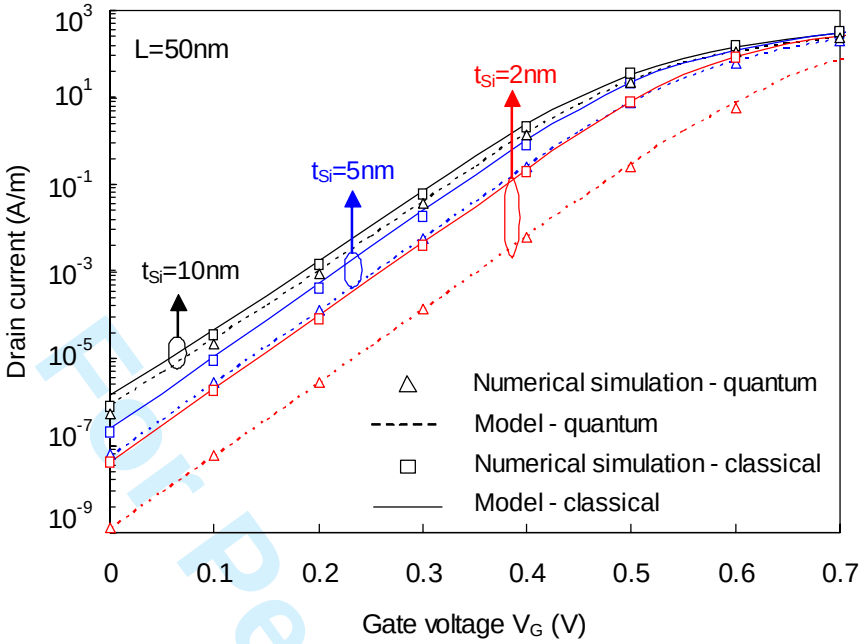


Figure 6. Munteanu et al.

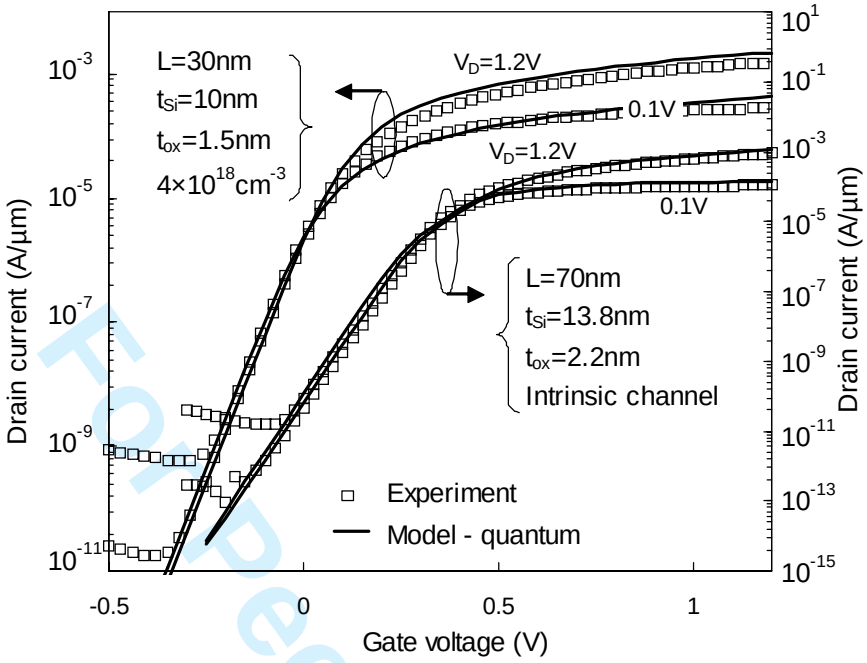
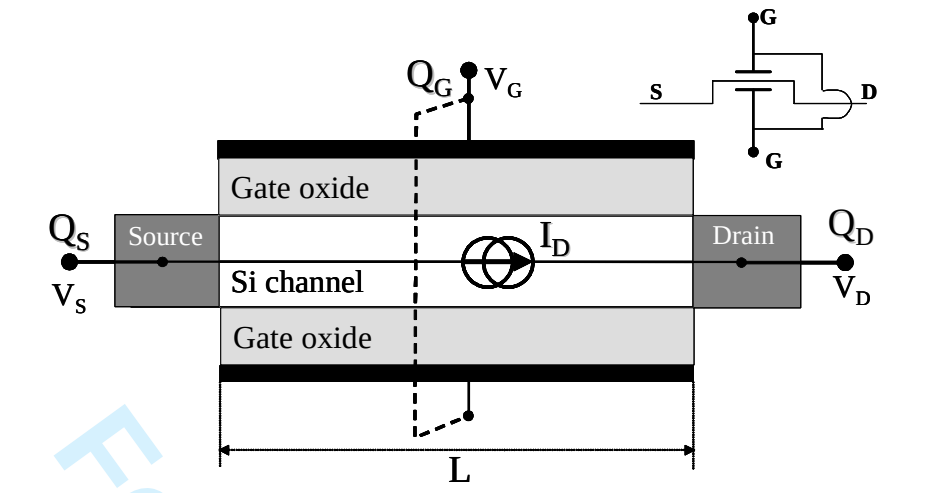
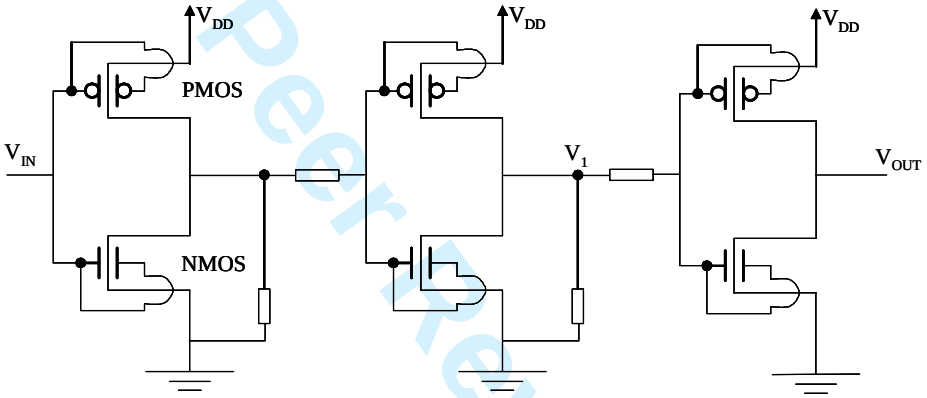


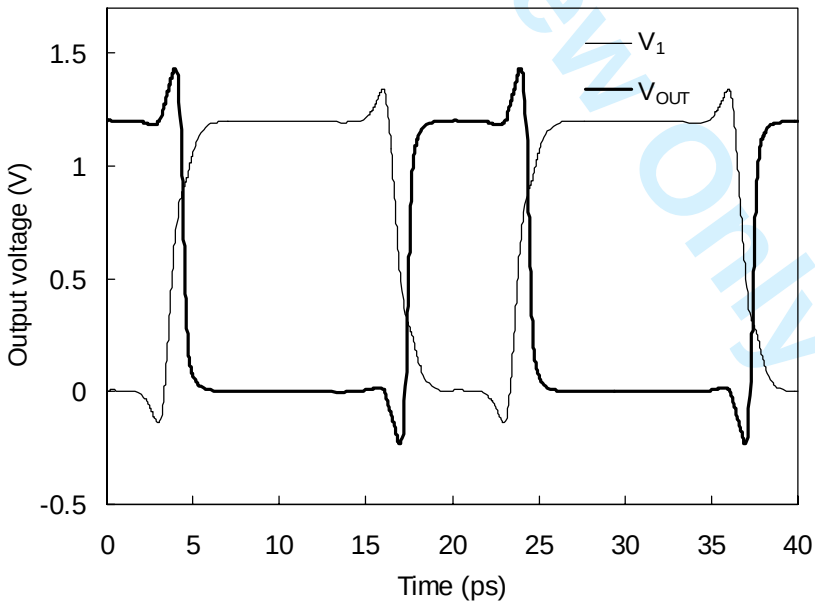
Figure 7. Munteanu et al.



(a)



(b)



(c)

Figure 8. Munteanu et al.