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BiCMOS Implementation of a Full-digital Linearized System for Complex Modulation Transmitter

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Abstract— This paper presents an original way to implement a wide band, low power, full-digital, linearized system for complex modulation transmitter. The circuit is devoted to all applications that require efficient amplification. It has been implemented in a 0.13 μm BiCMOS9 process, so simulation and experimental results are presented to validate the principle of the system.

I. INTRODUCTION

In the context of the proliferation of various standards in 3G or more, the evolution of transmitters leads to multi-standard operation. In the perspective of a flexible transmitter, the digital approach offers several advantages compared with analog implementations. Indeed, added to less consumption and size reduction, it allows an easier reconfigurable system.

Concerning the modulation, the increasing demand of services leads to the use of more and more complex schemes with non constant envelope signal (like CDMA or OFDM systems). So, the transmitter must include a system to linearize the amplification for any signals and optimize the efficiency at the same time.

A transmitter has been proposed [1] to overcome all these constraints. This proposed architecture (Fig.1) is based on the use of a homodyne IQ transmitter, the EER (Envelope Elimination and Restoration) method [2] and sampling techniques [3] for the linearization. The main characteristic of the architecture, Fig.1, is to generate an RF phase-modulated with constant envelope signal before the amplifier. A 1bit- $\Sigma\Delta$ coder is used to convert the envelope signal in a constant envelope one; this signal is, at the same time, combined with both quadrature phase signals and transposed to the carrier frequency thanks to three-inputs mixers. Therefore, this constant envelope signal can be amplified by any kind of non linear high efficient PA. The envelope information is restored by band-pass filtering. This architecture does not suffer from phase/amplitude delay mismatch and bandwidth limitation introduced by the DC/DC converter used in classical EER architecture.

In the perspective of a universal transmitter, the architecture is attended to meet modern communications systems requirements (e.g. CDMA, CDMA2000, WCDMA, UMTS) such as signal bandwidth, noise floor, dynamic range (nearly 80dB).

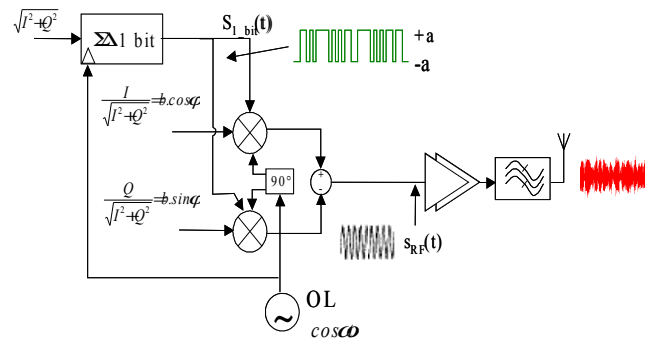


Fig. 1 Transmitter Architecture

In this work, we focus on the implementation of the linearization system, that is digital up to the amplifier. In a previous paper [4], the design, the implementation and the measured characteristics of a high-speed, 45 dB power controlled, 9-bit (necessary to respect the requirements for new standards) RF DAC (Digital to Analog Converter) is demonstrated.

In this paper, we focus on an original way to implement a digital quadrature modulator and the combiner to make the architecture digital boundary as far as possible in the transmitter chain.

II. A DIGITAL QUADRATURE MODULATOR

A. Toward the digital quadrature modulator

As it is shown in Fig.1, the quadrature modulator mixes the interpolated 1-bit $\Sigma\Delta$ envelope signal with the normalized phase signals ($I_n=I/\sqrt{I^2+Q^2}$ and $Q_n=Q/\sqrt{I^2+Q^2}$) and the local oscillators.

The immediate and classical solution would be to implement an analog modulator with three-inputs mixers.

In the perspective of a flexible transmitter, we wanted a solution to push away the limit of the digital part. A simple digital multiplication of the phase signals (I_n and Q_n) with the two-levels $\Sigma\Delta$ signal could have been a solution, but, at high frequencies, it suffers from long time delay and high power consumption. We implemented an alternative solution, based on simple gates, presented in the next section.

B. New digital quadrature modulator

Since the output of the $\Sigma\Delta$ and the LOs signals have only ± 1 values, the multiplication of the three signals depends only on the sign of the product of $\Sigma\Delta$ and the LOs signals:

- if both signals have the same value, then the output is equal to I_n (or Q_n);
- if both signals have complementary values, then the output is equal to $-I_n$ (or $-Q_n$).

This corresponds to the truth table of a logic exclusive OR function. So the command signal (CMD), that determines whether the phase signals have to be inverted or not, is simply the XOR of the envelope (output of $\Sigma\Delta$) and LO signals.

$$CMD_I = E_{\Sigma\Delta} \oplus LO$$

$$CMD_Q = E_{\Sigma\Delta} \oplus LO_{90}$$

Therefore the result of the multiplication of the three signals can be written as:

$$I_{LO} = (I_n \cdot \overline{CMD_I}) + (-I_n \cdot CMD_I)$$

$$Q_{LO} = (Q_n \cdot \overline{CMD_Q}) + (-Q_n \cdot CMD_Q)$$

The implemented IQ modulator using only multiplexors, XOR and NOR gates is plotted in Fig.2.

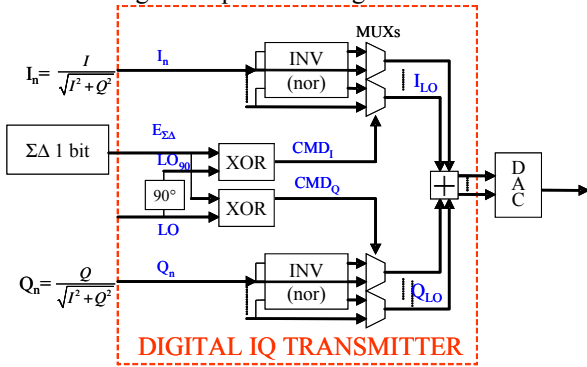


Fig. 2 Digital Quadrature Modulator

By choosing a simple selection of $\pm I_n$ and $\pm Q_n$, a straightforward full-digital and wideband quadrature modulator can be implemented. The power consumption is reduced compare to analog solutions.

In addition, the system gain in precision as the quadrature LOs signals can be digitally generated leading to a phase-error less than 1° , and then to a minimisation of the image frequency.

The two digital signals, I_{LO} and Q_{LO} , have then to be added through an output combiner presented in the following section.

III. OUTPUT COMBINER

A. Choice of architecture

The sum of the two 9-bit high frequency signals I_{LO} and Q_{LO} has to be realised at the output of the modulator. So a 10 bit adder has to be designed in order to prevent overflow (Fig.3).

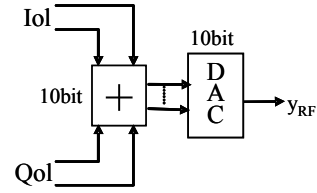


Fig. 3 10-bit Digital Adder with DAC

But one must take care about two characteristics for the design of the adder [5]: the propagation delay and the power consumption. They depend on the frequency, the supply voltage, and the topology of the circuit. With actual technology, the reachable performances are not sufficient for high frequencies and low power applications.

The idea proposed in this work is to replace the 10-bit digital adder and the 10-bit DAC by two 9-bit DACs combined by addition of their output current in a load (Fig.4).

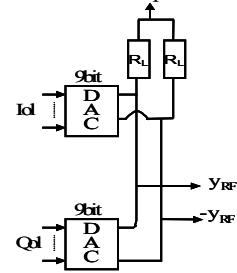


Fig. 4 Proposed Combiner

This structure is differential and wideband, that avoids the use of a band-limited single-to-differential circuit at the input of the power amplifier. The power dissipation of the two 9-bit DACs is the same as in the case of a single 10-bit DAC since for a given output power, each DAC delivers half of the output power.

B. Power-controlled DAC

In order to meet the new standards gain control requirements for radiocommunication systems, we need to achieve 80 dB dynamic gain control. The power amplifier may have about 35dB of dynamic, so the output combiner, thanks to the DAC, must provide approximately 45dB of gain control necessary to adjust the transmitter power (Fig.5).

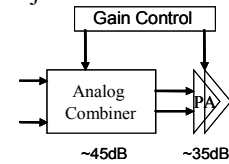


Fig. 5 System gain control

In [4] we have described a way to design the 9bits, 45dB gain controlled DAC. To optimize its implementation, we have proposed to split the basic structure in two DACs with smaller sizes.

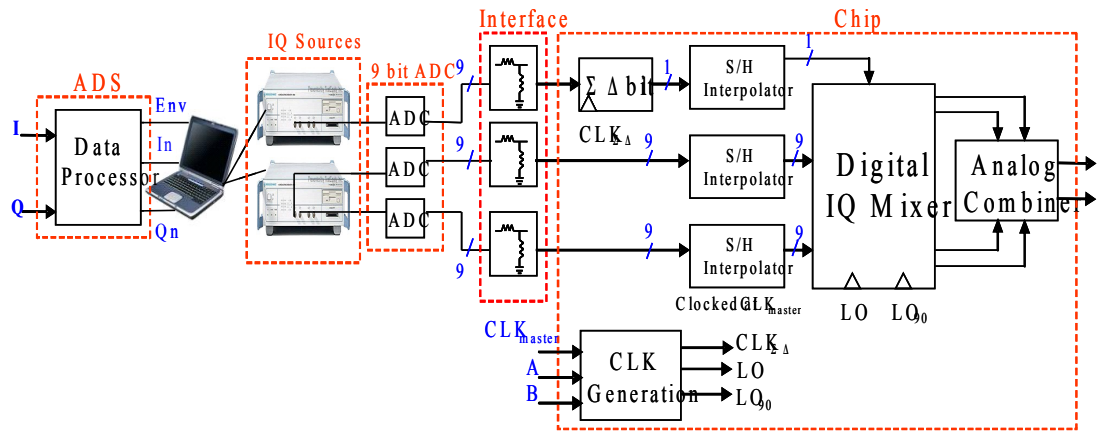


Fig. 6 Block diagram of the chip and test set-up

IV. IMPLEMENTATION AND MEASUREMENTS

A. Test set-up

The linearization system, including the digital quadrature modulator and the analog combiner, has been designed with $0.13\mu\text{m}$ BiCMOS from STMicroelectronics. Fig.7 shows the layout of the circuit including the $\Sigma\Delta$ coder, interpolation filters, signal buffers, digital up-converters and analog combiner. Attention has been paid in the layout to separate the low frequency digital circuit and power supplies from the RF signals.

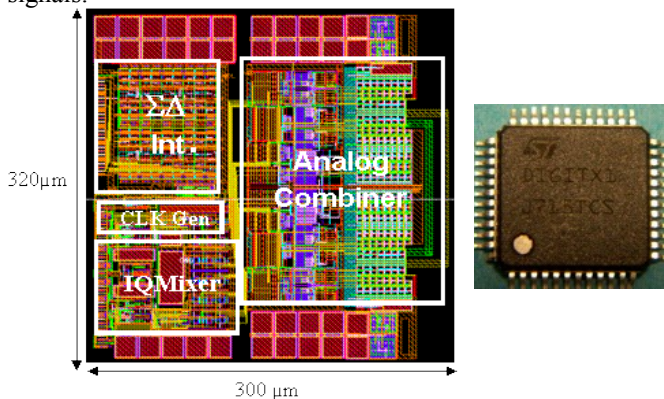


Fig. 7 Layout of the linearized system

A block diagram of the test set-up is shown on Fig.6.

The band-base processing consists in creating IQ datas that permit the generation of the analog signals. Three external 9bits ADC are used to convert analog IQ sources signals into digital domain. 9 bits represent the minimum resolution needed to fulfill the new standards EVM requirements. The interface block transforms the 3V output external DAC level into the 1.2V input circuit level. A “clock generation” circuit has been designed on the chip to generate the different clock signals, derived from an external clock master frequency. Two control signals (A and B) allow the $\Sigma\Delta$ modulator frequency control.

B. Simulated and experimental results

A test chip with only the 9bits DAC has been implemented in a first step to demonstrate its performance [4]. DAC circuit is $160*160\mu\text{m}^2$ size. The chip consumes less than 3.5mW at 1.4GHz (limitation due to the signal generation). Simulation results predict less than 48mW at 4GHz. The targeted 45dB dynamic has been proved experimentally.

Concerning the test of the whole implemented system (chip of Fig.7), Fig.8 and Fig.9 show the output spectrum respectively for simulation results and measurements in the case of an envelope frequency of 3MHz, for a DAC control current of $20\mu\text{A}$, with a RF frequency of 900MHz (sampling frequency limited experimentally to 1.8GHz). As expected, and it allows to validate the principle of the linearized system, the output of the transmitter is composed of a two-tone signal with a bandwidth of 6MHz.

The image rejection has been measured at -16dBc (Fig.9), compared to -26dBc (Fig.8) in the simulation. One of the principal reasons of this increase is attributed to the degradation introduced by out-of-chip components (9bits ADC for example) and to the imperfections of the layout.

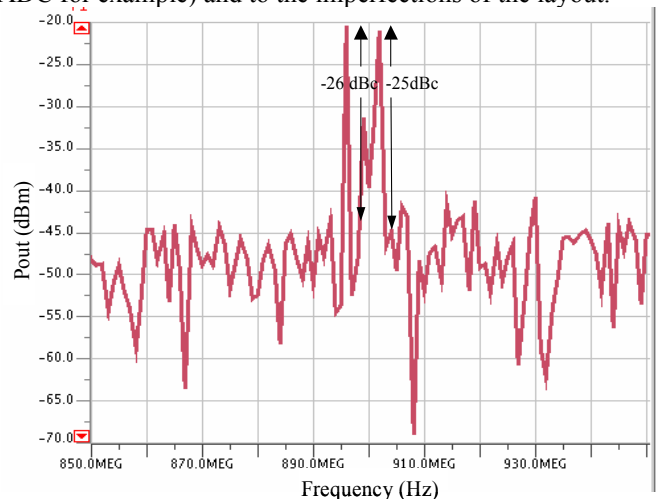


Fig. 8 In-band spectrum for $I_{ref}=20\mu\text{A}$ at 900 MHz (extracted layout simulation)

V. CONCLUSIONS

This paper presents the implementation of a fully digital linearized transmitter architecture dedicated to radiocommunication standards. An original way to implement an IQ modulator, fully-digital and wide band, has been proposed. It takes advantage of the ± 1 signal at the output of the 1-bit $\Sigma\Delta$ modulator and very simple implementation with CMOS logic gates and multiplexors, instead of high consuming digital multipliers.

A chip has been realized in the $0.13\mu\text{m}$ BiCMOS process of STMicroelectronics; it has been optimized in the sense of the consumption reduction. Its performances can be improved thanks to an optimization of the layout and an integration of the external blocks (for example, IQ sources); nevertheless the measurements results allow to confirm the efficiency of this digital approach, especially of the digital IQ modulator.

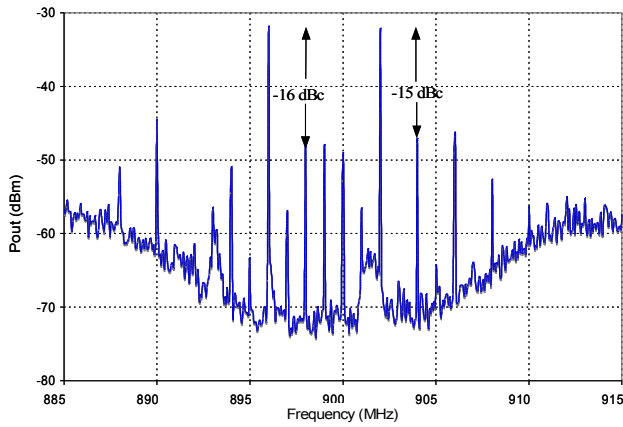


Fig. 9 In-band spectrum for $I_{ref}=20\mu\text{A}$ at 900MHz (measured)

Finally, Fig.10 presents the dissipated power of the whole system for LO frequency of 900MHz. It shows the increase with the DAC current I_{ref} , and an upper value of 35mW.

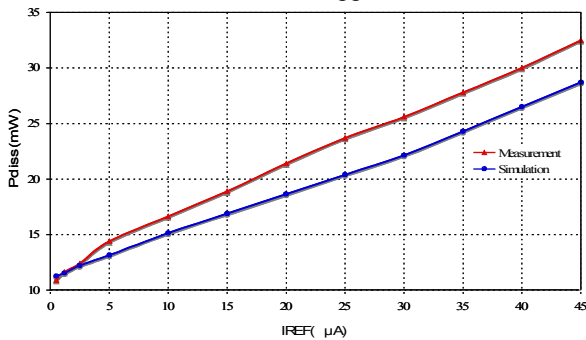


Fig. 10 Dissipated power of the transmitter with LO frequency of 900 MHz

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