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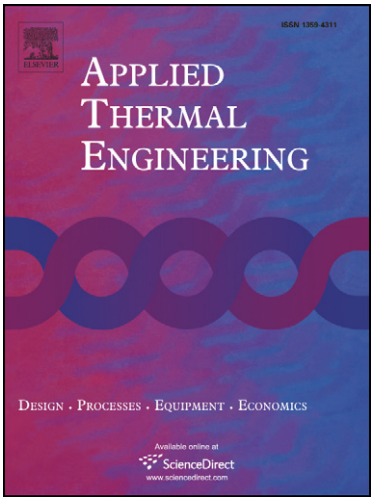

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Architectural **optimisation** for microelectronic packaging

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Abstract

The aim of this paper is to provide a methodical approach for architectural optimization of power microelectronic devices. Because critical parameters of electronic devices are linked with reliability, architectural optimisation, selection of the geometrical parameters of device and optimization of these parameters by iteration method associated by numerical analysis of reliability have to be achieved. In this way, this paper discusses about a methodical and numerical approach for the optimization of reliability in electronic devices, in particular the influence of geometrical parameters on the device reliability.

1) Introduction

In these last decades, the development of power electronic packaging has lead to important evolution about integration and architectural design of microelectronic device. This evolution answers to the increasing miniaturization, high density of components with a high reliability of devices. For this latter, the reliability prediction of device can been calculated via the semi-empirical relation ships, such as Coffin-Manson rule [1,2] and its variants in conjunction with complex non-linear finite element analysis which are used at the present time to determinate the fatigue life of solder joints or the failure of substrate.
In this way, the improvement of microelectronic device reliability is linked to the thermo-mechanical stresses in solder joint, thermal properties of heat sink and the geometrical parameter in device architecture [3,4]. **Numerical approach allows determining** the thermo mechanical stresses and life prediction of device. Also, this approach gives better understanding about the influence of design parameters on microelectronic devices reliability [5].
The aim of this paper is to show how numerical approach can integrate the optimization of geometrical parameters, such as the thickness of different layers of microelectronic device. Some industrial constraints are added to the optimization problem. Results are analysed in terms of mechanical and thermal influences.

2) Construction principle of microelectronic device and thermo-mechanical considerations

2.1) Microelectronic device description

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In modern electronic devices, the packaged structures consist of a variety of metallic, ceramic, plastic or composite layers [6]. The large difference of coefficient of thermal expansion (CTE) between ceramic substrates, such as Al_2O_3 and AlN, heat dissipation materials, such as Cu and Al, and semiconductors **such** as Si and GaAs, induces thermal stresses resulting in failures at the interfaces between the different layers of the devices. In high power dissipation packages, thermal management is an important issue to prevent thermal damage of sensitive components on the silicon ship, particularly for high-density electronic packaging. Thermal management is thus one critical aspect in the design of multichip modules to ensure reliability of electronic devices with high packing and power densities. In this context, the thermo-mechanical stresses depend on the differences of CTE of the materials, the geometry and the temperature gradient in device.

As it can be seen in figure 1, the CTE of the used materials are quite different. Therefore, device reliability is mainly linked with the difference of 1) **the CTE of the copper base plate (17 10^{-6} °C^{-1}), 2)** the DBC substrate CTE (6.5 10^{-6} °C^{-1}) and with the large area solder connection between DBC and base plate. This joint is most critical at passive thermal cycling. The failure mechanism is solder fatigue which provokes an increase of the thermal resistance and an early module failure [7]. The improvement of this reliability is commune for heavy-duty traction modules where copper base plate is replaced with AlSiC or Cu/W composite base plate. Indeed, it matches the CTE of DBC substrates and therefore reduces the stress on the large area solder joint.

2.2) Failure origin of microelectronic devices

The solder connection between silicon chip and DBC substrate is less critical to thermal cycling because of their relative small CTE mismatch. This joint is common for any module design, and the high active power cycling stress can be cause failures and a careful selection of DBC material and silicon chip size is important in order to keep the mechanical stress low.

The modelling of creep rate by common Coffin-Manson rules applied on the solder joint between DBC and base plate has been performed. Figure 2 shows clearly a peak stress in the extremity of the solder joint. This peak stress is owing to the load transfer which occurs from the substrate to the DBC (see figure 2). It is due to the difference of CTE between the different materials layers in electronic architecture which leads to important differences of thermal strain and thermo-mechanical stresses. This load transfer involves a longitudinal stress in the DBC equal to zero at the free edge which converges to a limit stress far away [8]. The weakness rigidity of the solder joint comparing to the other materials enables the load transfer from the substrate to the DBC. It brings about also a peak stress in the solder joint near the free edge and provokes the fatigue failure of the device. **More details are available in [6].**

2.3) Geometrical and physical parameters of a standard microelectronic device

The heat source is assumed to be an electronic chip in contact with joint solder on the top of DBC substrate which is a thin alumina film coated on both sides with thin copper film. Each silicon chip generates a background power close to 15 Watts (or 3 10^9 $W.m^{-3}$) which is dissipated in cross the multilayer electronic device, i.e. DBC substrate and **copper base plate**. The convective heat transfer coefficient between the bottom copper base plate and the cooling water is equal to h=20000 $W.m^{-2}.K^{-1}$ with the temperature of cooling water (T_{ext}) equal to 20°C.

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The geometrical parameters of device are directly been measured on micrographs from optical microscope observations. This observations have been performed on a polished cross section of standard microelectronic device, see figure 3. These measures have allowed **defining** the device geometry for a numerical model. Quadratic elements have been used to the meshing of electronic devices. The meshing has been studied in terms of stress concentrations. It has lead to some refined meshing near the free edges of each layer.

For heating circuits in general, the rate of failure is often determined by failure of the alumina plate **and/or** of the joint solder between copper plate and DBC substrate. This is caused by excessive thermally induced interfacial stresses. In this way, it is also important to study the interfacial tension due to the different CTE of the different layers in electronic device as well as the differences in terms of temperature. The architecture and the properties of packaging materials are the key parameters **to improve** the reliability of electronic device.

Some geometrical and physical parameters of electronic device can be easily modified in an industrial process; we have selected in particular the following parameters (Table 1).

This study will determine the influence of these parameters on the reliability of device and therefore describes the methodical and numerical approach for the optimisation of these parameters which can be easily modified in industrial application.

3) Module optimization problem

In this section, general optimisation problem is presented in an electronic context. Design variables are presented.

3.1. Optimization problem

The generalized architecture optimization problem writes as follows:

(1) $$\text{Minimize } f(V)$$
(2) $$\text{subject to } gi < 0;\ i = 1;\ ng$$
(3) $$Lj < vj < Uj;\ i = 1;\ nv$$

where V is the vector of design variables. $f(V)$ is the objective function to be minimized, gi are the constraints of the architecture optimization problem, ng is the number of constraints, Lj and Uj are respectively the lower and the upper limits of variables vj, with nv number of variables.

In this present problem, the design variables are the layer thicknesses and the material properties of the heat sink. Thicknesses are defined as continuous variables. Material variables are defined as discrete variables. Note that in the current approach, no constraint function gi is imposed, but lower and upper limits are used for variables vj in order to avoid negative thickness or too large dimensions.

3.2. Variable choices

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Electronic packages are composed of different plates and materials. One of the actual key-issue is to find the best composition of modules in terms of materials and plate thickness. In this approach, three layers are optimised with two different materials:

- Layer variables: one of the key-issue of the reliability of electronic packaging is the solder joint between the heat sink and the copper plate. In this approach, three layers closed to this joint are optimised. The first **one** is the heat sink thickness. This variable enables to decrease or to increase the static moment which brings about some stress in the joint [9]. The copper **base** plate thickness near the joint is optimised too. This layer can provokes some stress concentration due to the load transfer from the heat sink. The last optimised layer is the alumina layer. For some thermal considerations, it is important to have an optimal thickness with out decreasing mechanical performances.

- Material variables: the heat sink material enables to control temperature dissipation in the electronic package. Some precedent works have shown this influence [9]. In the current approach, two materials are optimised: AlSiC and Cu. This material optimization consists in having a good compromise between mechanical properties and thermal properties.

For some industrial constraints, some lower and upper limits are imposed for these variables. Continuous variables are used for the thickness and discrete variables are used for the material choice. Table 2 presents the variables and their limits.

3.3 Objective function

The objective function is very important for the optimisation problem. Indeed, results depend directly on this objective function. In our problem, a viscoplastic strain is chosen as objective function. It is based on the Darveaux's model and is defined as follow: Expressed in tensor form, as used in the modelling, the Darveaux constitutive model for the steady state creep is given in equation below [10] [11].

(4) $$\frac{\partial \varepsilon^{cr}}{\partial t} = A\left[\sinh(B\sigma_{mises})\right]^n \exp\left(\frac{-Q}{RT}\right)$$

$\frac{\partial \varepsilon^{cr}}{\partial t}$ is creep strain rate
σ_{mises} is Von Mises effective stress
R is gas constant
Q is activation energy
T is absolute temperature
A is pre-exponential factor
B and n are materials dependent constant
sinh is hyperbolic sinus function

Materials property values used in the Darveaux constitutive model are given in the table 3. These representative typical values of SnAgCu solder joint.

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The explicit treatment for the discretization in time is employed. This requires a small time step to be taken, in order to limit the plastic strain correction in each time step to a fraction of the plastic strain correction in each time step to a fraction of the elastic. A procedure has been implemented to fully automate the time step size variation throughout the cycles. **COMSOL software** is used to calculate this objective function. The finite element model is not recalled here. Details of the numerical model are available in [9]. To resume, the objective function *Fi* of the solution *i* can be write as follow:

(5) $$Fi=\frac{\partial \varepsilon_i^{cr}}{\partial t}$$

ε_i^{cr} corresponds to the strain defined in equation (4).

3.4 Optimisation procedure

Matlab software is used here. The *fmincon* function enables us to find minimum of constrained nonlinear multivariable function. This algorithm is a subspace trust region method and is based on the interior-reflective Newton method described in [12] and [13]. Each iteration involves the approximate solution of a large linear system using the method of preconditioned conjugate gradients (PCG). The main difficulty is to avoid local optima. In order to verify the stability of the algorithm, different starting points have been used. In all studied cases, results are the same for different starting points.
A coupling between COMSOL and Matlab has been carried out. For this purpose, a script of the numerical model has been implemented using the design variables. Figure 4 represents the flow chart of the optimization program.

3.5 Conclusion

The optimisation of electronic packages has been presented **in this study.** Design variables have been chosen: three layer thickness and two materials. This optimisation procedure is now applied to the electronic package presented in section 2.

4. Applications

The archistructural problem is now applied on the electronic module presented in section 2. Two heat sink materials are optimized: copper and AlSiC **base** plates.

4.1 Results

The heat sink is here composed of copper material or AlSiC material. In order to verify the stability of the solution, different starting points have been used. Each solution *i* is rated with a ratio *ri* defined by:

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(5) $$ri=\frac{Fi}{Fref}\times 100$$

where *Fref* corresponds to the Darveaux's criterion defined in Eq (4). The computation time is about one hour with a 3.06 GHz Pentium IV computer. The algorithm has converged to *ri*= 93% which corresponds to a decrease equal to 7% for the AlSiC material. In this case, the optimized variables vector *V* is equal to:

(6) $$V=\begin{pmatrix} v1=2mm \\ v2=0.27mm \\ v3=1mm \\ v4=AlSiC \end{pmatrix}$$

The optimized variables are a good compromise between the thermal and the mechanical responses.

4.2 Discussions

Following comments can be addressed:

- **Effect of the heat sink dimension**: the algorithm decreases the thickness of the heat sink. It enables to diminish the static moment of the packaging. **Indeed, this static moment is due to the geometrical and material properties of the heat sink.** It involves a lowest moment which decreases the effect of the load transfer from the substrate to the copper plate. One consequence is the fact that the shear stress in the solder joint is less important which brings about a creep strain lower than the reference packaging;

- **Effect of the copper layer dimension**: the decreasing or the increasing of the thickness of the copper plate has not an important influence. **Furthermore, the algorithm decreases its thickness.** Indeed, the rigidity is less important and the stress generated by the transfer is decreased. The solder joint ensures the link for this load transfer and is less stressed with this diminution of the thickness;

- **Effect of the alumina (DBC) substrate:** alumina substrate allows us to obtain good properties in terms of thermal behavior. **The algorithm leads to a more important thickness. Indeed, i**t isolates the bottom of the module and decrease thermal effects. It brings about a decrease of stresses due to the difference of CTE between the different layer;

- **Effect of the nature of the material heat sink:** the best material is AlSiC. Indeed, thermomechanical properties of the AlSiC material induce a best response of the module due to its CTE, conductivity and rigidity. It offers the best compromise for electronic packaging.

It is interesting to calculate the normalized sensitivities of the objective function. It shows that the normalized sensitivities of the copper layer can be neglected in comparison with the others materials. In the next section, a sensitive analysis has been done on the thicknesses of the alumina and the AlSiC layers.

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4.3 Influence of the alumina and the AlSiC thicknesses

As the copper layer influence can be neglected due to its normalized sensitivity, the analysis is carried out on the alumina and the AlSiC. Figure 5 presents the creep strain following the AlSiC and the alumina layer thicknesses.

This figure shows an important non-linearity of the response. A good compromise must be chosen for both thicknesses. The AlSiC must be important because it decreases the creep strain. But the alumina thickness presents a maximum nearly 0.28 mm where the creep strain is maximum. The alumina thickness must be inferior to 0.26 mm **or** superior to 0.285 mm in order to have a small value of the creep strain.

4.4 Conclusion

The optimization procedure has been applied to a typical electronic module. It enables us to optimize the thickness of layer with the material of the heat sink in the same time (see Figure 6). The main conclusion is that optimized modules present a good compromise in terms of thermal and mechanical response. It enables us to understand mechanisms in the design of electronic module.

5 Conclusion

This study has allowed to determinate the optimal architecture of microelectronic device in according to the reliability criterion. A particular attention concerns the description of thermo-mechanical and reliability problem, and thus this present study suggests a numerical optimisation approach by finite elements and an iterative method.
Finally, this study shows the interest of numerical analysis in many technology and scientific problems. This approach offers also the news possibilities for the optimization of complex device.

6. Acknowledgements
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List of tables

Table 1 : Identification of main geometrical and physical parameters in according to the optimization of device reliability.

Table 2 : Design variables

Table 3: Specific constants of solder joint material in Darveaux's model.

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Geometrical parameters	**Actual Values in standard industrial device**
Thickness of the base plate	3 mm
Thickness of the copper layer in DBC substrate	0.3 mm
Thickness of alumina in DBC substrate	0.6 mm

Physical parameters	**Actual Values in standard industrial device**
CTE of base plate	8 10^{-6} °C^{-1} (AlSiC) or 17 10^{-6} °C^{-1} (Copper)
Thermal conductivity of base plate	160 $W.m^{-1}.K^{-1}$ AlSiC) or 400 $W.m^{-1}.K^{-1}$ (Copper)

Table 1 : Identification of main geometrical and physical parameters in according to the optimization of device reliability.

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Variables	Lower limit	Upper limit
Thickness of the base plate	1 mm	4 mm
Thickness of copper layer in DBC substrate	0.125 mm	1 mm
Thickness of the alumina in DBC substrate	0.125 mm	1 mm
Material of the base plate (discrete variable)	Copper	AlSiC

Table 2 : Design variables

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A (s-1)	B (Pa-1)	n	Q/R (K-1)
9.62 e+4	9.25 e-8	15.631	8.6 e+3

Table 3: Specific constants of solder joint material in Darveaux's model.

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List of figures

Figure 1: Electronic device architecture

Figure 2 : In case of plate base copper, load transfer from the substrate to the DBC.

Figure 3 : Real and model geometry of standard microelectronic device

Figure 4: flow chart of the optimization program

Figure 5: creep strain following the AlSiC and the alumina thicknesses.

Figure 6: Actual and optimized geometries

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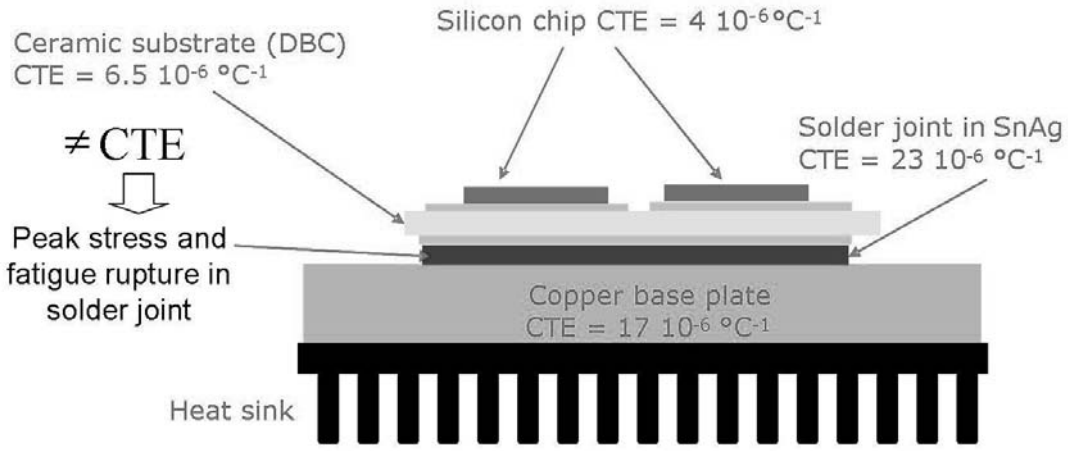

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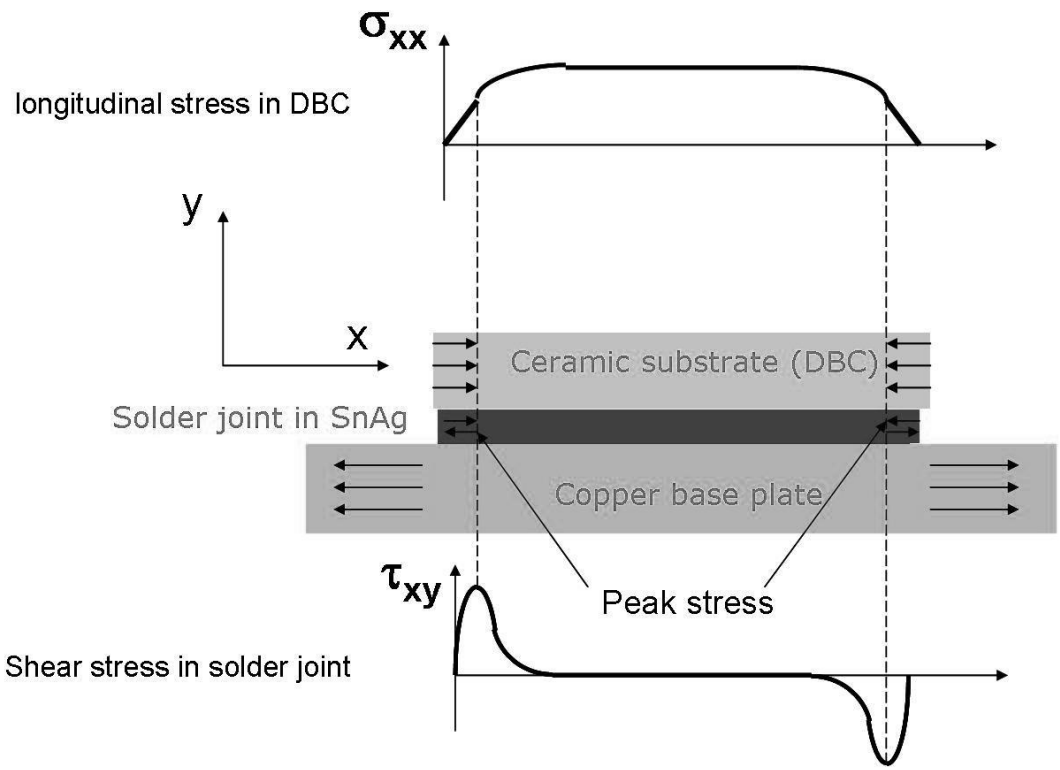

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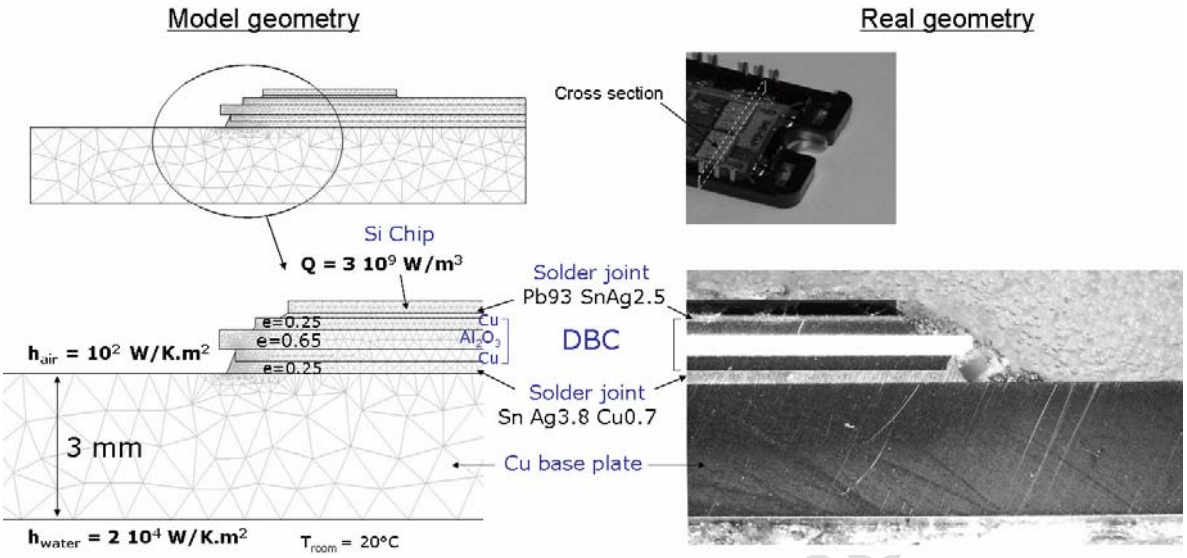

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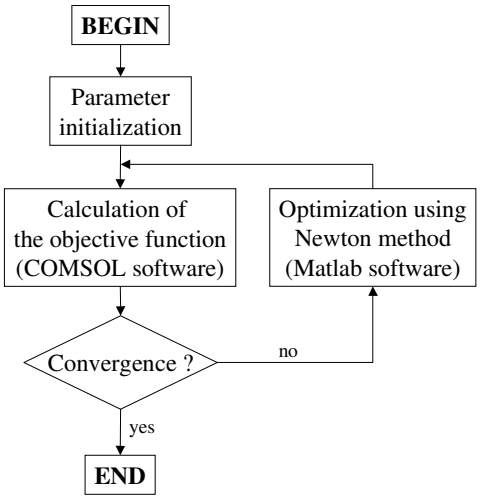

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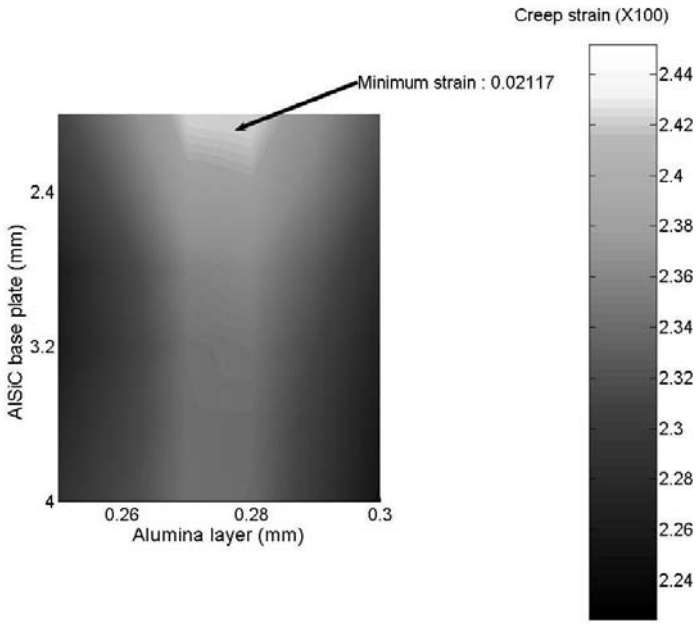

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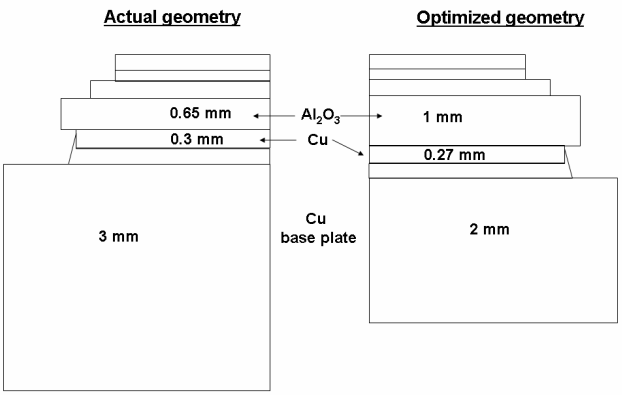

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