



HAL
open science

Single die multiple 600V power diodes with vertical voltage terminations and isolation

Kremena Vladimirova, Jean-Christophe Crébier, Yvan Avenas, Christian Schaeffer, Timothé Simonot

► **To cite this version:**

Kremena Vladimirova, Jean-Christophe Crébier, Yvan Avenas, Christian Schaeffer, Timothé Simonot. Single die multiple 600V power diodes with vertical voltage terminations and isolation. ECCE (Energy Conversion Conference and Exposition) IEEE, Sep 2010, Atlanta, United States. hal-00520089

HAL Id: hal-00520089

<https://hal.science/hal-00520089>

Submitted on 22 Sep 2010

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Single die multiple 600V power diodes with vertical voltage terminations and isolation

K. Vladimirova, J.-C. Cr ebier, Y. Avenas, C. Schaeffer, T. Simonot

Grenoble Electrical Engineering Lab (G2Elab)
961 Houille Blanche Street, 38402 St Martin d'H eres, France
e-mails: vladimirova@g2elab.grenoble-inp.fr, crebier@g2elab.grenoble-inp.fr

Abstract – Integrating multiple power devices in the same die makes their implementation more simple and reliable. In this paper, a new concept for low cost and high efficiency monolithic integration of 600V vertical power diodes is proposed and experimentally validated. The concept relies on the creation of vertical voltage terminations on the periphery of the devices, thus allowing to terminate and to isolate each one of the integrated power devices. Simulation results show that the stress of the electric field can be minimized by introducing an angle on the vertical termination walls. The fabricated prototypes fulfill the initial design electrical specifications with excellent dynamic and operational behavior.

I. INTRODUCTION

Recently, the interest in power conversion systems such as interleaved converters or multiphase structures with intercell coupling device has grown up [1]. These structures offer the advantage to increase the apparent switching frequency of the converter and to improve the dynamic response and performance of the system while drastically reducing the sizes of the passive components. In order to do so, many inverter legs and interconnections are needed, thus leading to complex implementation and reliability problems. A possible solution of those problems is the monolithic integration of the active devices, of their drivers and associated functions [2]. This leads to a reduced amount of power dies and interconnections and simplifies their implementation. But the cohabitation of multiple vertical diodes or transistors in the same die requires isolation techniques to limit the electrical interactions such as the leakage currents among the power devices [3]. To separate active regions of vertical power devices integrated in a common die, a trench termination technique can be used [4]. Originally appeared in the scientific papers as a technique that allows to terminate each device by reducing the surface electric field so that the breakdown voltage is near ideal [5,6], this technique can also be used to isolate each drift region of the monolithically integrated multiple power devices. As a result, it becomes possible to integrate several power devices in a single die, all sharing the same backside contact (drain, cathode or collector).

This paper presents the monolithic integration of multiple 600V vertical power diodes. The idea is to use a deep trench vertical termination, filled with dielectric material, to terminate and to isolate each device from its neighbor while maximizing their voltage handling capability using the same termination. The paper focuses on the special

care taken to minimize the stress of the electric field on the periphery of the device, acting on the angle of the termination walls. Power diodes in the range of 600V are fabricated and experimentally tested. The obtained results proved the initial design specifications.

II. DESIGN AND REALIZATION

A. Concept

The concept of the vertical voltage termination technique is to create a deep trench termination on the periphery of the device. Using a deep reactive ion etching (DRIE) technological step to obtain the desired depth and wall angle of the termination, multiple devices can be integrated in a single power die. Figure 1 shows a schematic view of the principle using power diodes as example.

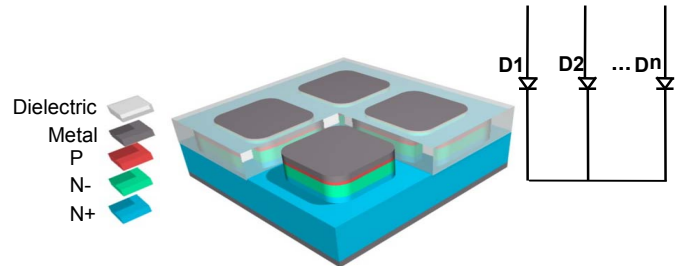


Fig. 1. Schematic view of multiple power diodes integrated in a common die using the vertical voltage termination technique

As figure 1 indicates, the vertical voltage termination technique allows the parallel implementation of multiple ‘island’ power devices on common degenerated semiconductive layer – the semiconductor substrate itself - or the metal layer.

A key benefit of the vertical voltage termination is the possibility to electrically isolate the different power devices who share the same backside (cathode) electrode. This authorizes the connection of the anodes of all the devices at different potentials at the same time and with no electrical interaction among them.

The technique is also advantageous because of the opportunity to distinguish the different patterns by the etching step. In this way, assembly of several power devices can be achieved at wafer level with minimum back end additional process steps. At the same time, it simplifies the assembly and the package of multiple dies and reduces the final cost of the power module.

The technique was developed on an epitaxial wafer but is easily transferable on homogenous substrates.

With such surface treatment and edge termination, power devices could also benefit of 3D interconnections replacing the wire bonds by massive copper connections. Figure 2 presents the possible evolutions of the package for multiphase bridges assembled in a 3D Power Chip on Chip configuration [7].

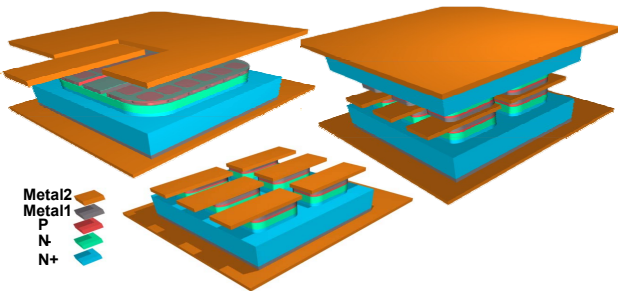


Fig. 2. Schematic view of the package using the vertical voltage termination technique. Example of a power transistor, six diodes with common cathode and a six legs polyphase rectifier

B. Theoretical results

In order to evaluate the effectiveness of the vertical voltage terminations, a detailed analysis with 2D finite elements simulations (SILVACO) has been carried out. In figure 3 is depicted the electric field distribution and the iso-potential contours at the reverse voltage of 800V for a vertical PIN diode having the following characteristics – 110 μ m thickness of the Si substrate where 0-3 μ m is the depth of the P region with 3.10e17/cm3 concentration, 3-50 μ m is the drift N region with 2.10e14/cm3 concentration and 50-110 μ m N region with 1.10e19/cm3 concentration.

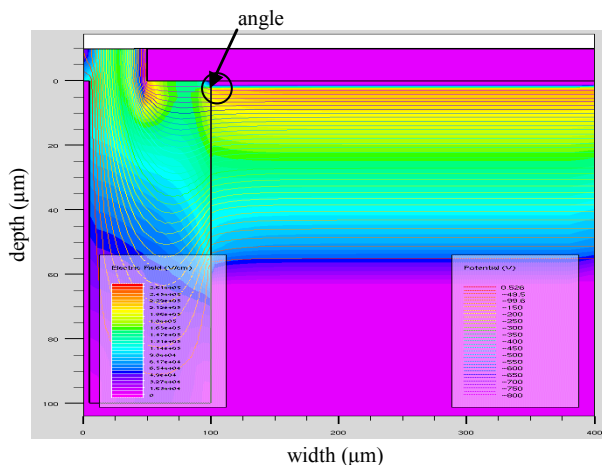


Fig. 3. Electric field distribution contours and potential lines at reverse voltage of 800V and vertical voltage termination of 100 μ m depth, 100 μ m width and 90°angle

In order to evaluate the possible effects due to the proximity of the neighbor device the left simulation plan

represents the most critical case of the increase of the backside potential. The simulated structure has a right angle vertical voltage termination of 100 μ m depth and 100 μ m width. The termination trench is filled with a dielectric material (with dielectric constant 3 which is the case of silicone gel) and completed with 10 μ m metal field plate on the surface.

The results show that the stress of the electric field on the periphery of the device, at the interface with the dielectric material can be significantly reduced using the “mesa like” vertical termination technique in addition with the field plate. The idea is that the trench termination will sustain most of the electric field allowing a better redistribution of the iso-potentials at the interface and at the periphery of the device.

Figure 4 represents the blocking capability of the simulated structure. It can be seen that the diode with vertical voltage termination achieves the required voltage rating of 800V which is the ideal breakdown voltage for devices with the same physical parameters having no cylindrical or spherical junctions.

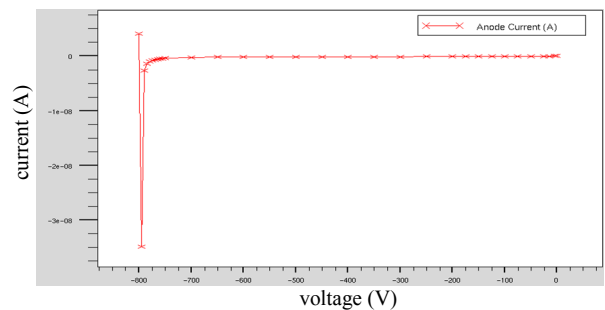


Fig. 4. Current-voltage reverse biased characteristic of the simulated structure

Figure 6 summarizes the possible effects of the addition of an angle on the wall termination as a result of the reduction of the section of the device from the P region to the N region (fig. 5). Figure 5 shows that the result of non vertical walls of the termination is a curvature to the bottom of the potential lines, witch is advantageous for the voltage handling capability of the device but also for the dielectric material. As it can be seen in figure 6, the lower the angle the lower the surface electric field. However, very low angles (below 45°) are not commonly used because they require very high consumption of silicon.

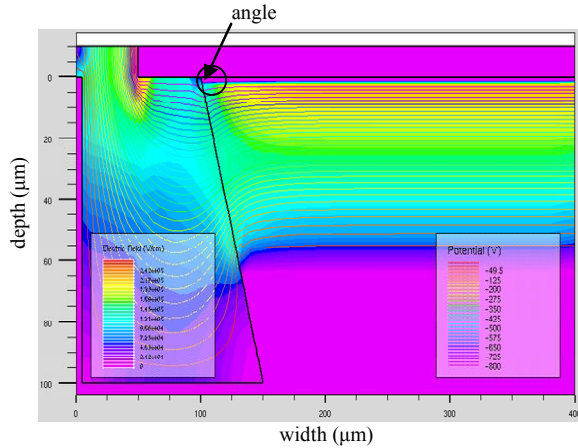


Fig. 5. Electric field distribution contours and potential lines for a diode with a vertical voltage termination of 100 μ m depth, 100 μ m width at 60° angle

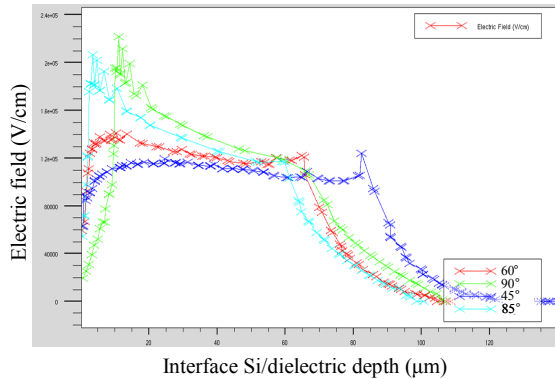


Fig. 6. Comparison of the cross-sectional views of the electric field at the interface Si/dielectric for different angles of the wall terminations

We have also analyzed the optimum trench depth. The results showed that the vertical voltage termination is functional to terminate and to isolate the active regions of the devices from each other only if its depth exceeds the drift and lightly doped N region depth of the substrate. In our case the drift region has a depth of 50 μ m coming from an epitaxy on a heavily doped substrate of 500 μ m and the surface electric field was found to be significantly reduced when the trench depth is greater than 50 μ m. Table 1 summarizes the results for the simulations of a structure with deep trench termination with 45° angle of the wall and completed with a field plate on the surface.

TABLE I

| Trench depth (μ m) | Maximum electric field (kV/cm) |
|-------------------------|--------------------------------|
| 100 | 120 |
| 60 | 120 |
| 50 | 280 |
| 40 | 350 |

C. Realization

Figure 7 presents SEM pictures of the realized vertical voltage termination diodes. In our case 500 μ m N type (100) substrate plus 55 μ m lightly doped (20 Ω cm) epitaxial layer was used for the fabrication of the prototypes.

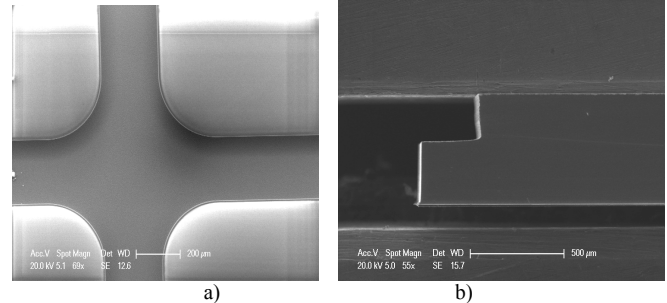


Fig. 7. SEM photographs of the silicon vertical voltage terminations of four power diodes integrated in the same die: a) view of the top of the surface, b) cross-sectional view of the periphery of one of the devices

All process steps except for the trenches realization – wet etching of the metal on the surface and deep reactive ion etching (DRIE) for the terminations - were performed without the need of any photolithography steps. No post processes for surface or wall treatment were performed after the silicon etching step. We obtained silicon etch rate of about 11 μ m/min using SF₆, C₄F₈ and He gases. We used a resist layer as masking material. The selectivity of silicon to the resist is almost 160:1. After the DRIE step the obtained depth of the vertical termination is about 100 μ m with 300 μ m width and an angle of the termination wall of almost 87° (fig. 8).

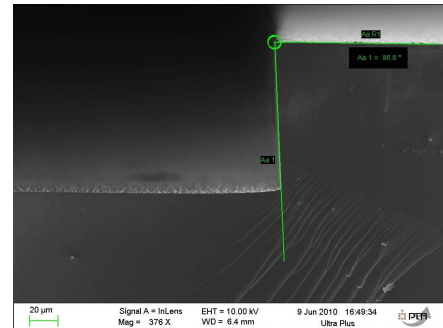


Fig. 8. SEM photograph of the angle of the termination wall

The vertical voltage termination technique can easily be applied on homogenous substrates too. In that case silicon etching should be performed until the common metal contact layer is reached. The mechanical support for the multiple ‘island’ power devices must then be assured by the metal layer. In order to do so, it is required that the metal layer should be significantly thicker. A possible technique that can be considered is the wafer bonding of silicon and a thick metal plate (copper or molybdenum). Figure 9 shows a schematic view of the concept.

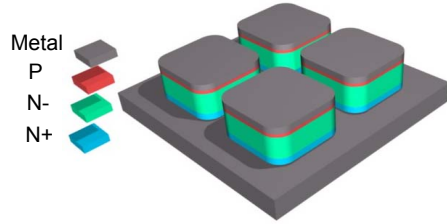


Fig. 9. Schematic view of the vertical voltage technique in the case of homogenous substrates

III. EXPERIMENTAL RESULTS AND DISCUSSION

For the experimental validation, the fabricated power diodes (600V, 10A) were packaged and passivated with silicone gel to protect the trench terminations and the whole power die. A metallic isolated substrate for improved thermal management was used to access the devices electrodes. The common cathode was soldered while the ‘multitude’ of anodes were wire bonded (the dies are 8x8mm²). Figure 10 shows the realized packages for 4 and 9 vertical 600V PIN diodes with common heavily doped Si layer as common cathode electrode.

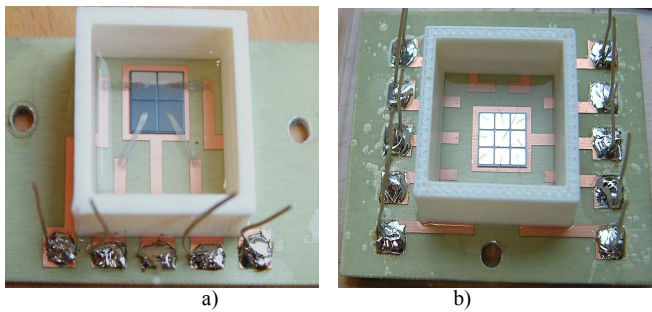


Fig. 10. Photographs of the packaged multiple power devices: a) four, b) nine power diodes

A. Static characterization

The packaged prototypes were experimentally tested in a first time with a static characteristic power curve tracer HP 371A. Figure 11 shows the reverse characteristics of each power device in the case of testing the monolithic integration of 4 diodes (prototype figure 10a). The four curves correspond to the four power diodes integrated in the same die. All four devices fulfill the initial design specifications considering the breakdown voltage rating of 600V.

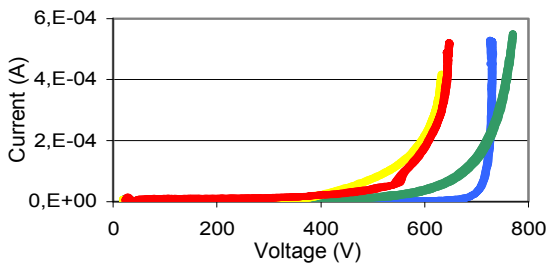


Fig. 11. Static characteristics of the reverse biased power diodes

The results show clearly that all four diodes have different voltage handling capabilities. It can be noticed in

fig.10 that one of the diodes has a leakage current of 10 μ A while the others have leakage currents in the range of 200 μ A. It has been demonstrated in previous studies [8] that the possible reason for large leakage currents is the imperfect sidewall treatments exposed the metallurgical junctions. However, in this case passivation of the power die and the termination walls was performed in a non protected atmosphere and the probable reason of the different blocking capability of the devices is a possible dust coming after dicing and before passivation of the walls.

Figure 12 represents the direct characteristic of the same four diodes.

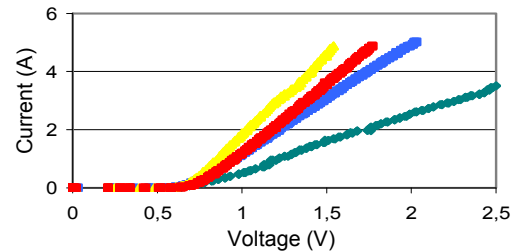


Fig. 12. Static characteristics of the direct biased power diodes

A non perfect ohmic contact between the semiconductor and the metal or a poor front side bonding quality might be the reason for the difference of their characteristics. Indeed, the current rating of the diodes is almost one decade below our expectations with static resistance of the four diodes in the range from 0.17 Ω to 0.6 Ω . This highly resistive behavior of the diodes should be the purpose of future additional experimental measurements.

B. Dynamic characterization

To experimentally validate the blocking capability of the diodes with vertical voltage terminations, one of the characterization tests included their implementation in a Buck power converter. The diode was not implemented as an operational switch but as a device under test to be exited by the high dv/dt created by the commutation cell of the converter. The experimental setup is shown in figure 13.

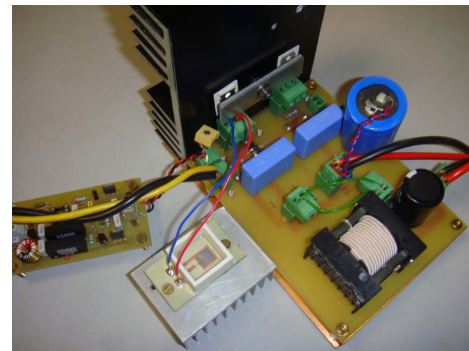


Fig. 13. Diode with vertical voltage terminations implemented in a Buck converter

The diode was connected in antiparallel with the main switch (a MOSFET transistor) and the tested diode was

excited with the same voltage as the transistor. No load current was allowed to flow through the device under test, and only HF currents created by the dynamic behavior were observable. The aim of this test was to evaluate if the diode was able to sustain the dynamics of the commutation and to maintain the voltage handling capability of the power MOSFET.

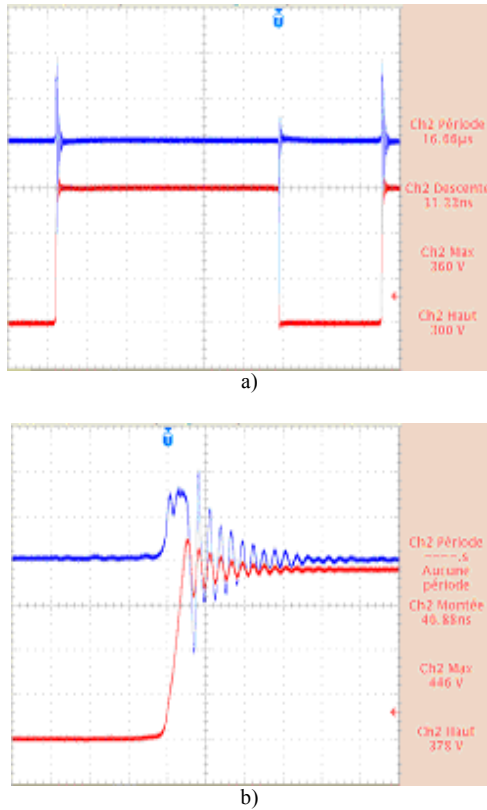


Fig. 14. Dynamic characteristics of the fabricated power diode a) current and voltage at the switching periods of the MOSFET, b) zoom at the off state with $dV/dt=450V/50ns=9kV/\mu s$

In figure 14 are depicted the obtained results with corresponding switching voltage waveforms (red curve) and dynamic current through the diode under investigation (blue curve). The diode demonstrated an excellent functional behavior of $9kV/\mu s$ (dV/dt).

C. Implementation of the multidiode device into an interleaved converter

In order to validate the approach, the implementation into an interleaved converter has been carried out. This validation is only partial since the converter was initially designed for 200V devices. Nevertheless, it gives an idea of the operation of several power devices sharing the same substrate and being islanded by the technique and the approach we have presented in this paper. The topology considered is a boost chopper with three commutation cells and three inductors, the diodes in the commutation cells are all sharing the same cathode electrode. The topology is depicted on figure 15a).

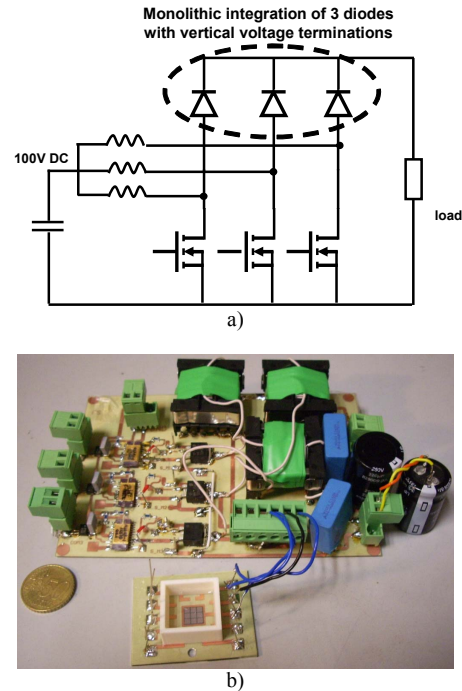


Fig. 15. Multidiode chip implemented in an interleaved Boost converter a) schematic view, b) picture of the experimental setup

Figure 15b) presents a picture of the converter where its boost diodes have been replaced by our multidiode chip. Figure 16 and 17 present practical results where it is possible to observe one transistor VDS voltage (dark blue curve on fig.16 and fig.17) and several current waveforms in the diodes (black curve on fig.16, black, grey and clear blue curves on fig.17) and current in one of the inductors (clear blue curve on fig.16). The waveforms exhibit high frequency oscillations at numerous time locations during the switching period because the interconnections have poor quality and the duty cycles have been phase shifted at 120° in order to take advantage of the structure from a filtering point of view.

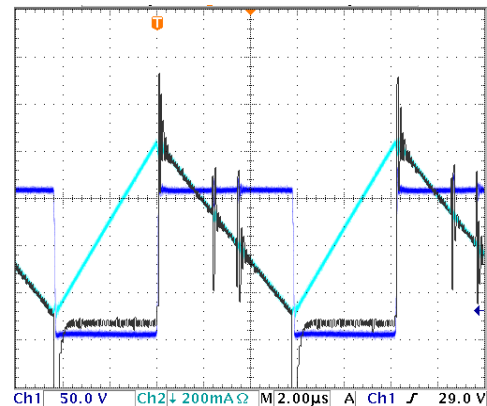


Fig. 16. Experimental results for one commutation cell -VDS voltage waveforms for the transistor, current through the diode and current through the inductor

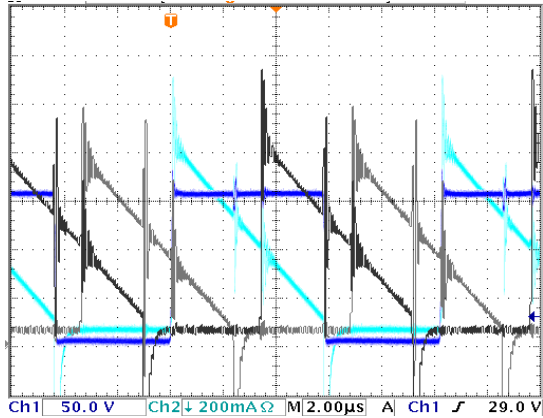


Fig. 17. VDS voltage waveforms for one of the transistors and current trough the tree diodes of the multidiode chip

The results correspond to what could be expected from the converter. The correct sharing among the boost legs indicates that they are very comparable since no feedback was implemented to equally split the load current among the three boost converters.

IV. CONCLUSION

The integration of multiple power diodes into a single die was presented. It is based on vertical voltage termination and isolation technique. The proposed technique contributes considerably to integrate the active parts of the complex converter by reducing the interconnections among the power devices.

The fabricated prototypes proved that the vertical voltage termination improves the electrical performance of the devices in terms of breakdown voltage while completely isolating their active regions – there is no electrical interaction between the different power devices other than the common backside potential.

The proposed technique simplifies the packaging. Using a deep reactive ion etching process step as a final processing step allows distinguishing the different patterns while maintaining simple the fabrication of the devices. The cost trade – off between packaging saving and wafer process additions should be further investigated.

The thermal coupling of the devices and the effects on trench isolation on the reverse biased leakage current and its temperature behaviors should be the purpose of future research studies.

ACKNOWLEDGMENT

The authors would like to thank CIME-nanotech (Grenoble), and RTB centers PTA (Grenoble) and FEMTO-ST (Besancon) for their technical support.

The authors acknowledge also the French Research National Agency (ANR) for its founding and support for the realization of the power devices (projects MOBIDIC and ECLIPSE).

REFERENCES

- [1] F. Forest, E. Laboure, T. Meynard, and J.-J. Huselstein, "Multicell interleaved flyback using intercell transformers," **Power Electronics, IEEE Transactions on**, vol. 22, no. 5, pp. 1662–1671, Sept. 2007.
- [2] Rouger, N.; Crebier, J.-C., "Toward Generic Fully Integrated Gate Driver Power Supplies," **Power Electronics, IEEE Transactions on** vol.23, no.4, pp.2106-2114, July 2008
- [3] US Patent 5,496,760: Method for Manufacturing Dielectrics Dividing with Isolated Regions, Fuji, 1996
- [4] Igic, P.; Holland, P.; Batcup, S.; Lerner, R.; Menz, A, "Technology for power integrated circuits with multiple vertical power devices", **Power Semiconductor Devices and IC's, 2006. ISPSD 2006. IEEE International Symposium on**, 4-8 June 2006 Page(s):1 – 4
- [5] Chanh Park; Jinmyung Kim; Taehoon Kim; Kim, D.J," Deep trench terminations using ICP RIE for ideal breakdown voltages", **Power Semiconductor Devices and ICs, Proceedings. ISPSD '03. 2003 IEEE 15th International Symposium on *14-17 April 2003 Page(s):199 - 202*
- [6] Theulier, L.; Mahfoz-Kotb, H.; Isoird, K.; Morancho, F, "A new junction termination technique: The Deep Trench Termination (DT2)", **Power Semiconductor Devices & IC's, 2009. ISPSD 2009. 21st International Symposium on**, 14-18 June 2009 Page(s):176 – 179
- [7] Vagnon, E.; Crebier, J.C.; Avenas, Y.; Jeannin, P.O., "Study and realization of a low force 3D press-pack power module", *PESC 2008, IEEE Power Electronics Specialists Conference, 15-19 June 2008 Page(s):1048 – 1054*
- [8] Chanh Park; Hong, N.; Kim, D.J; Lee, K.," A new deep trench termination technique using ICP RIE for ideal breakdown voltages", **Power Semiconductor Devices and IC's, 2002. ISPSD 2002. IEEE International Symposium on**, Page(s):257 – 260