



HAL
open science

Design and characterization of an integrated CMOS gate driver for vertical power MOSFETs

Timothé Simonot, Nicolas Clément, Jean-Paul Rouger, Jean-Christophe Crébier

► **To cite this version:**

Timothé Simonot, Nicolas Clément, Jean-Paul Rouger, Jean-Christophe Crébier. Design and characterization of an integrated CMOS gate driver for vertical power MOSFETs. ECCE (Energy Conversion Conference and Exposition) IEEE, Sep 2010, Atlanta, United States. <hal-00520085>

HAL Id: hal-00520085

<https://hal.science/hal-00520085v1>

Submitted on 22 Sep 2010

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization

Design and characterization of an integrated CMOS gate driver for vertical power MOSFETs

SIMONOT Timothé, ROUGER Nicolas, CREBIER Jean-Christophe

Grenoble Electrical Engineering Lab – G2Elab, UMR 5269 CNRS/ Grenoble –INP / UJF,
St. Martin D'Hères, France
crebier@g2elab.grenoble-inp.fr

Abstract -- Currently, the trends in energy management are performance enhancement and increase in system reliability for the reduction of energy consumption. In this context, the integration of the gate driver within power transistors is particularly appropriate. This integration offers multiple advantages, from electrical and EMI performance improvement to power module size reduction, and reliability and functionality increase. This article presents a power MOSFET gate driver system developed with an approach which consists in including all the circuits required to drive a power switch on a single CMOS chip. The CMOS driver chip functionalities will be presented in this paper, and its design will be explained. Finally, experimental results of the fabricated chip used in a buck converter topology will be shown and discussed.

Index Terms-- power conversion, power MOSFET gate drive, integrated circuit design, hybrid integration

I. INTRODUCTION

Trends in power converters are to increase the switching frequencies in order to reduce the size of the passive components. MOSFETs are appropriate devices because they are superior to power BJTs and IGBTs in high frequency, low to medium voltage applications where the switching power losses can be dominant. Moreover, some devices are designed to be driven with a low voltage control. As it is shown in figure 1, several functions are required for a proper drive of power MOSFETs, such as a control signal insulation system, an amplification of the control signal, protection circuits and also a floating supply to deliver energy to these systems. Gate signal insulation systems in many power electronics circuits are classically achieved with a magnetic or piezoelectric transformer [1, 2], a level shifter [3], or can be integrated using an optical receiver [4, 5] or using a wireless HF transmitter [6]. Then, the amplification of the driving signal is needed as close as possible to the power transistor gate in order to minimize inductive effects and coupling resulting in increased commutation losses. The addition of protection circuits may prevent the component from its destruction in the event of an over voltage, a short circuit current or an operation over the temperature limit. At last and in order to supply these systems, an insulated low power floating supply is necessary.

With the help of VLSI (Very Large Scale Integration) complex functions can be integrated within a small silicon area, with specific insulation characteristics and separated

from the power device, allowing operations at high voltage levels (kV). This paper presents the design, the characterization and the implementation of a CMOS driver chip, which integrates all the required functions to drive a power MOSFET.

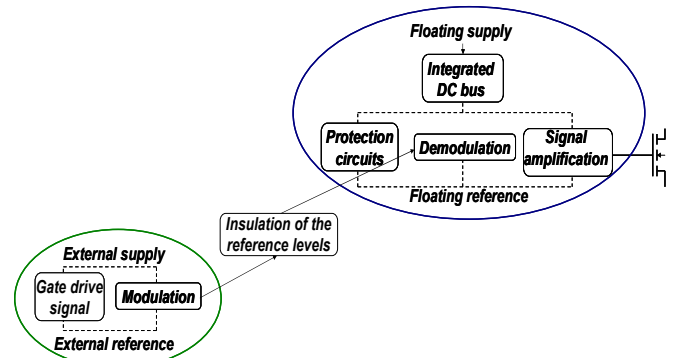


Fig. 1. Power MOSFET drive system

The integration of the supply of the whole system is usually a specific issue not often addressed in the integration process. To solve this concern, self supply systems have been developed along with different techniques like bootstrap [7], charge pump [8], or pulsed linear regulator [9] in a purpose of simplifying the implementation while increasing the reliability of the converter. These systems can be assembled in the power module or monolithically integrated inside the power device. These techniques have the advantage of offering good performance levels and a good reliability as interconnections are strongly reduced and simplified.

II. CMOS DRIVER CHIP DESIGN

The choice was made to include all the functions needed to drive a power MOSFET within a single and separate CMOS chip, sharing elements with the power device to drive. This is a good way to strongly reduce the interconnections among gate driver components, to simplify its implementation and increase its reliability. It allows eliminating most of the electrical connections (to the control, to the ground or external supplies), which drastically reduces the EMI coupling and parasitic propagation paths. As shown in figure 2, this CMOS device contains a remote control signal insulation system, a signal amplification circuit and a self

supply system. The external gate signal is modulated and sent from the converter control unit into the integrated coreless transformer and then demodulated. The purpose of this transformer is only to guarantee an electrical insulation level between the control unit and the integrated driver. This transformer does not deliver the energy required for the switching of the power transistor, this energy being provided through the integrated self supply circuit. This demodulated gate signal is then amplified and applied to the main switching transistor. The amplification circuit is supplied with the help of a linear pulsed regulator system which requires only an auxiliary transistor and a storage capacitor [9]. The self supply transistor can be monolithically integrated in the same power chip, and the driver chip and the storage capacitor can be flip chipped at the surface of the power transistor with the appropriate footprint and surface metallization [14]. This will further simplify the implementation of power transistors compared to state of the art commercially available gate drivers, while improving their reliability and increasing their functionalities.

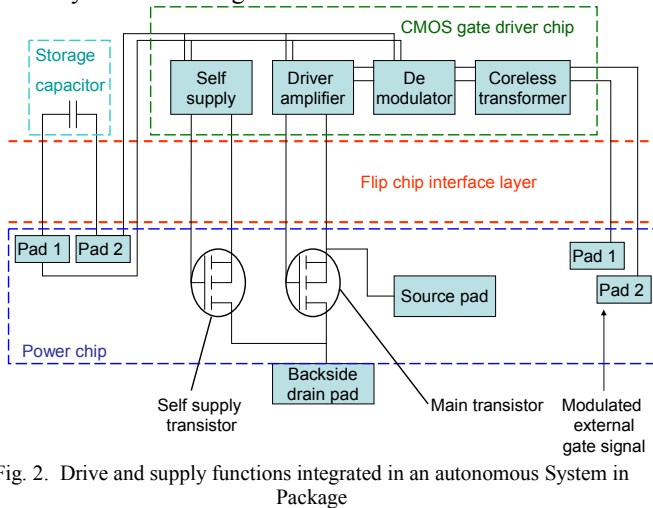


Fig. 2. Drive and supply functions integrated in an autonomous System in Package

A. Control signal insulation

The control signal insulation is carried out with a coreless transformer integrated onto the CMOS die (Figure 3). This is a planar stacked type transformer taking advantage of the four metal layers available with the selected technology (AMS 0.35 μ m). It exhibits a high coupling coefficient together with a low self resonant frequency and needs less silicon area compared to other types of integrated transformers [10]. The primary winding is made with the outer metal layers because the potential of this winding is tied to the supply of the converter control unit which can be very different from the reference potential of the CMOS chip. This happens in the case where its related power device is a high side transistor, for example in a full bridge topology. The secondary winding is on the inner metal layers. The dielectric oxide thickness between the two windings is 2.6 μ m, which offers an electrical insulation in the range of 1kV. The same electrical insulation is expected for the pads on the power

chip which are drawn to receive the wire bonds bringing the control signal from the converter control unit. For this, these pads are insulated from the active region of the power transistor with a thick silicon nitride layer deposited by PECVD. To reduce Eddy currents in the substrate, N tubs were added under the transformer windings.

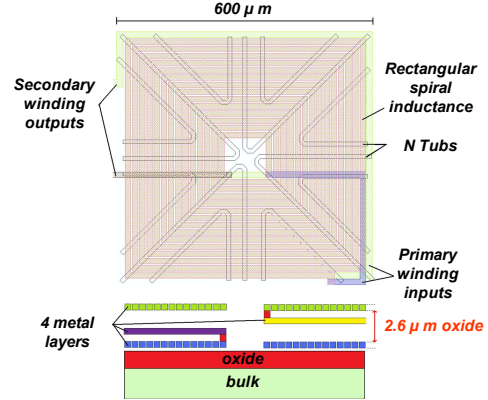


Fig. 3. Integrated transformer layout and cross sectional views

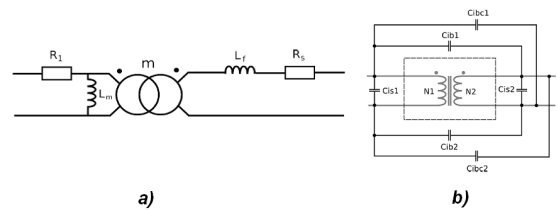


Fig. 4. a) Magnetic model of the integrated transformer b) Capacitive model

The electrical inductive and resistive model associated with this transformer is shown figure 4-a. The transformer is represented by the series resistance R_1 and the magnetizing inductance L_m on the primary side, and the series resistance R_s and the leakage inductance L_f on the secondary side. The coupling coefficient is m . The capacitive model shown in figure 4-b includes the inter-windings capacitances C_{ib1} , C_{ibc1} , C_{ib2} and C_{ibc2} and the windings capacitances C_{is1} and C_{is2} . The values of these components are determined with a series of test applied to a numerical modeling of the structure of the transformer. This has been carried out with software Flux 2D (from CedratTM) and the results are presented in table I.

TABLE I
VALUES OF THE MODEL ELEMENTS OF THE TRANSFORMER

R_1	L_m	m	L_f	R_s	
19,6 Ω	58 nH	0.9	10 nH	120 Ω	
C_{is1}	C_{is2}	C_{ib1}	C_{ib2}	C_{ibc1}	C_{ibc2}
- 100 fF	- 100 fF	260 fF	260 fF	130 fF	130 fF

Since the transformer does not have a magnetic core, the value of the magnetizing inductance is small and the signal sent into the transformer must be modulated at a high frequency. The chosen modulation technique is the Amplitude Modulation (AM) with a carrier frequency

between 90 and 250MHz and a square wave modulator. This was chosen to simplify the demodulation circuit. The signal at the output of the transformer is applied to the demodulation circuit in order to extract the low frequency gate signal waveform. A 10ns delay between the demodulated and the initial gate signals was observed in simulation, which is small compared to the 160ns delay introduced by classical optic couplers such as the HCPL 2200/2219 [11]

B. Self supply system

A new active control of the self supply voltage of the CMOS chip is implemented using the two functions integrated in both the CMOS die and the power device. Basically, the supply circuits derive the energy from the power transistor during its ON and OFF states. This is carried out with two different circuits, one operating during the ON state and one at the turn OFF switching transition of the power device to drive. The energy that is harvested is either regulated using a pulsed linear regulator [9] or converted using an integrated charge pump topology [12]. Besides their possible and easy integration, the combination of both supply techniques allows different type of operations from permanent switching to long term ON or OFF state. Moreover, only a small storage capacitor is needed next to the gate driver to filter the self supply voltage. The optimal size of the storage capacitor is calculated on the basis of the current consumption of the CMOS chip (10mA in average), the switching frequency of the power MOSFET, the tolerable voltage drop of the supply voltage (less than 1V), and the energy that can be gathered during the ON state. This leads practically to storage capacitors between 10nF and 100nF at 3.3V for switching operations from DC up to 500 kHz.

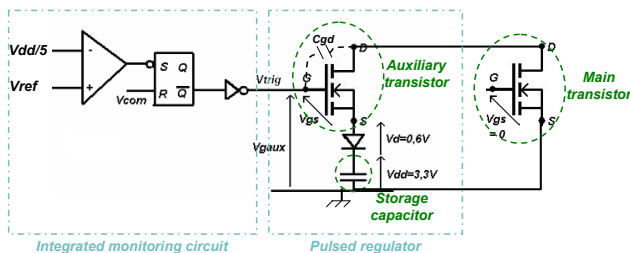


Fig. 5. Pulsed regulator and monitoring system

Figure 5 shows the pulsed regulator system together with the monitoring circuit which can be easily integrated in the CMOS chip. The pulsed regulator is active when the main transistor is switched off, as a voltage V_{gaux} appears at the gate of the auxiliary transistor via the capacitor C_{gd} . This is the consequence of a positive dv/dt appearing across the power device while it is turning off. When this voltage reaches the auxiliary transistor threshold voltage level, this transistor is switched on and part of the load current flowing in the power device is directed into the storage capacitor, therefore recharging it. The monitoring circuit is an improvement of the state of the art. It helps controlling this

recharge by comparing a fraction of the supply voltage with an internal reference voltage source. This gives the opportunity to enlarge the effective operating range of the self supply technique with respect to the power side operating conditions (V and I). When the capacitor voltage reaches the desired supply voltage level (3.3V), the state of the comparator changes and the auxiliary transistor is switched off, stopping the recharge. This is to mention that the gate voltage of the auxiliary switch cannot be switched ON but it can be shorted to interrupt the recharge sequence. As the main transistor switches ON, the RS latch is reset and the gate of the auxiliary transistor is left floating, thus allowing to be sensitive to the next recharge occurrence.

Nevertheless, this approach is known as being limited for operations at low frequencies or permanent ON state. Especially, the permanent ON state operation is not allowed as it would require an infinite storage capacitor. In order to widen operating conditions, permanent ON state self supply solutions were recently investigated [13], in which the main transistor is partially switched OFF, therefore generating a recharge sequence of the storage capacitor. The new solution proposed here is to add a new system completing the pulsed regulator supply. This system is composed of a boost type charge pump circuit, which is activated only during the ON state of the main transistor (figure 6). This circuit multiplies the low voltage available across the power switch while current is flowing through it (supposedly close to 1V) in order to obtain a sufficient voltage to supply the CMOS chip. The connection between the power switch and the input of the charge pump circuit is made through a second auxiliary switch. The topology of the charge pump is given figure 6. As it can be seen, C_{in} and the switched capacitors C_1 and C_2 are integrated in the CMOS chip while C_{out} is the external storage capacitor. An internal command circuit made of a ring oscillator and a clock generator creates the command signals of the charge pump switches. With a switching frequency of 60MHz and an input voltage of 1,2V, the output voltage and delivered power levels of the charge pump circuit were estimated by simulation as a function of the gate width of the CMOS switches and the value of the switched capacitors (figure 7). In the optimal case, an output power of 25mW was obtained, which is sufficient to supply the chip and consequently allowing a permanent ON state. Nevertheless, the output voltage of the charge pump is in the range of 2,5 to 3V, requiring to establish the nominal threshold voltage of the power device in comparable levels. This is addressed later in the paper. The efficiency of the charge pump circuit is about 50%, which is satisfactory since the energy is harvested from the conduction losses of the power device. Therefore, the overall efficiency of the converter is not deteriorated.

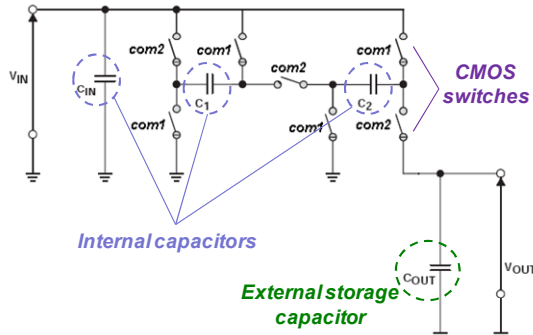


Fig. 6. Boost charge pump topology

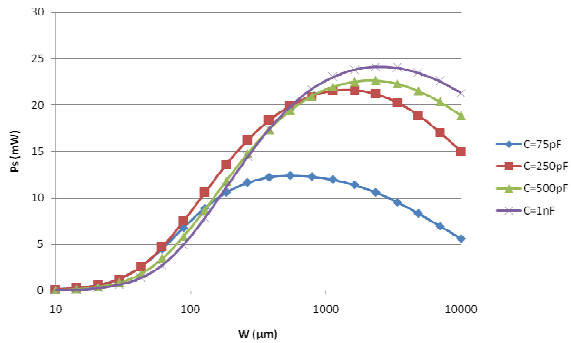


Fig. 7. Simulation of the output power of the charge pump as a function of the gate width of the CMOS switches and the switching capacitors value

The advantages of these self supply systems are a precise monitoring of the storage capacitor recharge sequence at main switch turn OFF and the possibility of a permanent ON state type of operation. This is a valuable extension of functionality compared to the state of the art. Moreover, it is important to point out that the energy used to supply the chip is harvested from both the conduction and commutation losses. As a result, in a mode of operation where the OFF state self supply does not increase the commutation losses, the efficiency of the converter stays the same and no external voltage source is needed to supply the chip, so the overall performance is increased.

C. Bipolar gate signal generation

Since this integrated driver supply can only be a positive voltage source, an integrated circuit based on a CMOS full bridge topology generates a three level signal to properly drive the gate of the power transistor. Each bridge arm is composed of several stages of CMOS inverters. The consecutive stages are of increasing size in order to amplify the gate signal as desired (figure 8) under very high dynamic conditions. The three levels signals are generated as follows: when the gate signal of the power transistor V_{com} is high (ON state), the gate is connected to the supply VDD and the source to the ground, so that $V_{gs}=+VDD$ (see qualitative waveforms on figure 8). When the gate signal goes low (OFF state), the gate is connected to the ground and the source must stay connected to the ground during the recharge sequence of the storage capacitor, then $V_{gs}=0$. This allows creating a path

for the load current to be derived from the main switch into the storage capacitor. When the storage capacitor's recharge is complete, the inverted comparator's output V_{trig} goes high (see figure 5), the auxiliary switch is turned OFF and then the source is connected to VDD so that $V_{gs}=+VDD$.

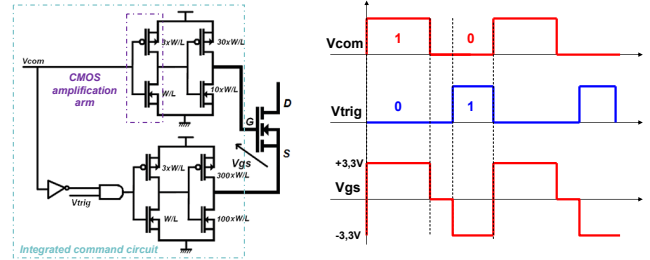


Fig. 8. Three level gate signal generation circuit and its operating waveforms

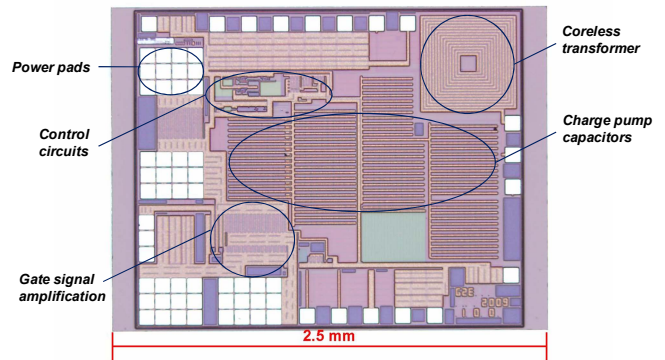


Fig. 9. Microscope photography of the CMOS chip

The design and layout of the CMOS chip were made with the microelectronic software Cadence, which offers high design reliability since accurate models for simulation are provided by the foundry (Austria MicroSystems), including temperature effects, worst case conditions and Monte Carlo analysis. These tools help the designer in circuit sizing and to anticipate on eventual failures due to environmental conditions. Figure 9 shows a microscope photography of the fabricated chip.

III. EXPERIMENTAL RESULTS

A. Integrated transformer characterization

1) Dielectric test

The insulation voltage of the integrated transformer was tested using a Tektronix 371A power curve tracer, which can deliver voltage pulses up to 3kV. To prevent floating pins, the two connections of the primary coil were short circuited. The secondary coil was also short circuited and a positive voltage has been applied between the primary and the secondary part of the transformer. A dielectric liquid has been deposited on the CMOS die in order to prevent the breakdown in air. The dielectric response of the transformer is shown on figure 10,

and it can be seen that a dielectric breakdown appears at approximately 1200V, which corresponds to the chosen insulation technique (see section II.A).

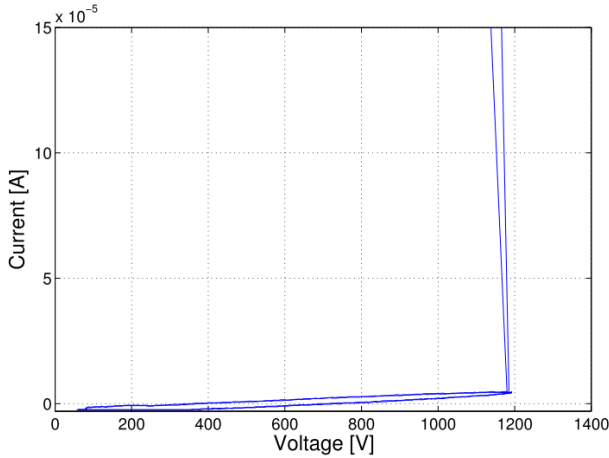


Fig. 10. Dielectric breakdown of the integrated transformer

2) Integrated transformer Scattering parameters measurement and comparison with the model

The S-parameters of the integrated transformer were plotted using a VNA (Vector Network Analyzer – Anritsu ME7808C, from 40MHz up to 110GHz) in a two orthogonal G-S port configuration. The measurements were conducted at IMEP in Grenoble, France. The S-parameters were also simulated using the software Agilent ADS (Advanced Design System) with the values of the model previously determined, the measurements were then compared to the model. Figure 11 shows the modulus of the measured S21 parameter corresponding to the transmission of the transformer from 40MHz to 40GHz, with a 50Ω impedance on both probes. It can be seen that two resonant frequencies appear at 490MHz and 890MHz, which can be interpreted as a better transmission of the transformer at these frequencies. From 5GHz to 40GHz, some other resonant frequencies appear, most likely due to the resonance of the inductances with small value capacitors. A similar behavior can be seen on figure 12, showing the measured and simulated Smith chart of the S11 parameter corresponding to the reflection at the primary winding. It can be seen on figure 13 that the model of the primary winding fits the measurements from 40MHz to 400MHz, but differ around the first resonant frequencies. The model must then be modified and a physical explanation of these resonances must be found. However, for a low frequency range (40MHz – 400MHz), the model is well suited and our design is validated. Those measurements are also helpful to determine resonant frequencies at which an optimal transmission of the transformer can be achieved.

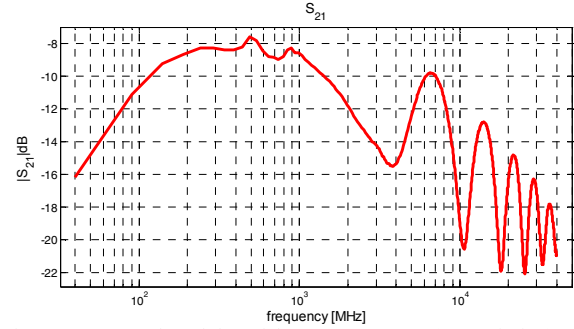


Fig. 11. Measured modulus of the S21-parameter (transmission) of the transformer

```

m1
freq=40.00GHz
S(1,1)=0.996 / 3.176
impedance = Z0 * (2.538 + j35.889)

m3
freq=40.00MHz
S(1,1)=0.438 / 140.596
impedance = Z0 * (0.433 + j0.298)

```

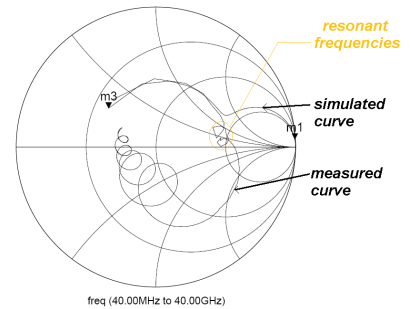


Fig. 12. Smith chart of the measured and simulated S11-parameter of the integrated transformer

3) Test of the demodulation circuit

A modulated sinusoidal signal using the modulation technique described in section II-A was applied to the primary side of the transformer as shown in figure 13 in order to validate the demodulation circuit and to measure its delay. The modulated signal was generated using a 100MHz signal generator. Figure 13 shows that at a 90MHz frequency of the sinusoidal signal, the amplitude at the primary side of the transformer must be around 15V in order to achieve a proper demodulation. Figure 14 gives an explanation of this requirement by showing the secondary side voltage of the transformer. As it can be seen, the signal losses in the transformer are considerable since the amplitude of the secondary side voltage is only 6V. This can be due to the frequency of the modulated signal, as it has been seen in the previous section that the first resonant frequency of the transformer is 490MHz. Another solution would be to improve the impedance matching between the modulator and the primary side, and also between the secondary side and the demodulation circuit. In order to decrease the losses in the signal transmission, a modulation circuit operating at the resonant frequency of the transformer must be designed, or the transformer must be redesigned in order to lower its resonant frequency and to adjust its input and output impedances matching. As a circuit which generates 3V amplitude at a 500MHz frequency is hard to achieve and would also increase the energy consumption of the system, the other solutions will be investigated in a future version of the CMOS chip. Nevertheless, figure 13 shows a proper operation of the demodulation circuit, and a 10ns delay between the modulated and demodulated signals observed in simulation is confirmed by this experiment.

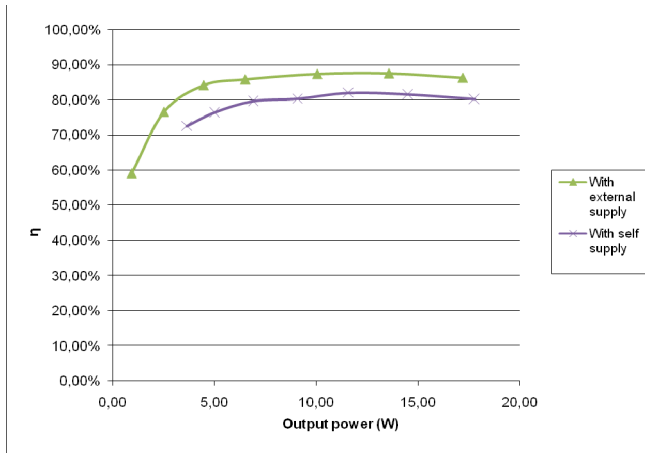


Fig 17. Efficiency of the buck converter with self supply and with an external voltage source

3) ON state self supply system

The command systems of the charge pump circuit were tested and observations showed a good operation of both the ring oscillator and the control circuit. As shown in figure 18, the ring oscillator is active only when the gate signal is high, thus the power switch being in the ON state. The output power of the charge pump circuit was estimated in the case of a permanent ON state mode of operation and compared to the simulation results. The measured current consumption of the command chip in this mode of operation was 9.1mA with a voltage of 3.3V, so a power consumption of 30mW. Figure 19 shows the measured output power of the charge pump circuit as a function of its input voltage. It can be seen that an input voltage of 2.4V is required to obtain an output power of 30mW, and thus to self supply the chip in a permanent ON state. However, a lower input voltage applied to self supply the chip in the case of a long or permanent ON state is possible as the consumption of the chip decreases when its supply voltage is lower. Thus, experiments have shown that a chip can be supplied with an input voltage of the charge pump circuit as low as 1,5V.

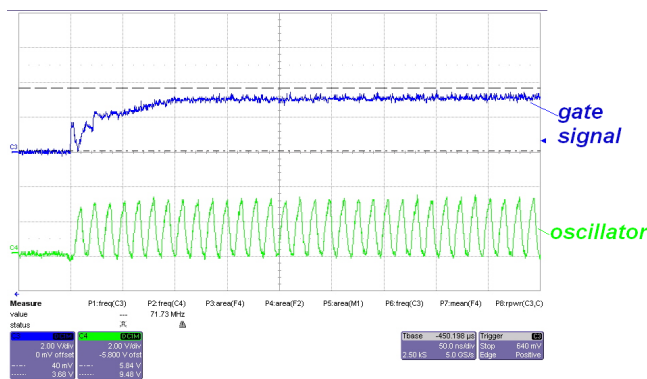


Fig 18. Ring oscillator waveform of the ON state self supply

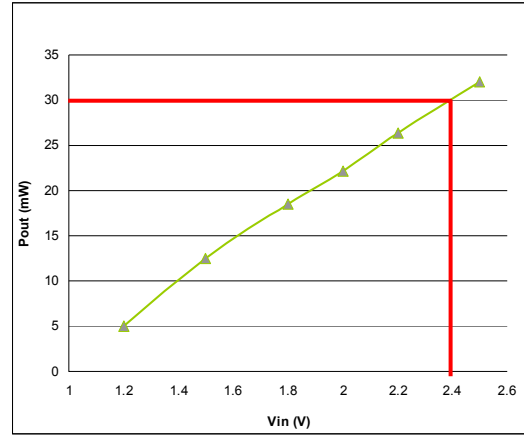


Fig 19. Output power of the charge pump circuit as a function of its input voltage

IV. SUMMARY

A gate drive circuit for power MOSFET transistors has been introduced in this paper. It includes the integration of the insulation of the remote control signal, two self supply systems, and several driving functions including bipolar gate source voltage generation. Experimental results of the fabricated CMOS chip have been shown and explained in order to illustrate and to validate some of the chosen approaches. The results show a good operation of the demodulation circuit of the gate signal, bipolar gate signal generation, and the control circuits of the OFF and ON state self supplies. Efficiency of the OFF state self supply must be observed at a higher load current in order to validate the hypothesis that the efficiency of the converter is not deteriorated compared to an external voltage source to supply the command. This will be possible with the fabrication of dedicated power components in a near future. These results are nonetheless encouraging, especially due to the full integration of all required gate driving systems. This integrated CMOS driver allows external supply, control, and driving systems to be no longer required. This will greatly simplify the implementation of the power devices in multiple transistor applications as described in [15] as well as improving the global reliability of the converter.

ACKNOWLEDGMENT

The authors gratefully acknowledge the contributions of J.D Arnould and N. Corrao from IMEP-LAHC (Grenoble - France) for the characterization of the coreless transformer. We would also like to thank O. Deleage for his contribution to the modeling of the coreless transformer.

The authors also acknowledge the French Research National Agency (ANR) for its founding and supports for the realization of the power devices (projects MOBIDIC and ECLIPSE) and the french RTB Centers PTA, LAAS, FEMTO-ST and CIME-Nanotech for their technological supports.

REFERENCES

- [1] Kliger, R., "Integrated transformer-coupled isolation," *Instrumentation & Measurement Magazine, IEEE*, vol.6, no.1, pp. 16-19, Mar 2003
- [2] Vasic, D. Costa, F. Sarraute, E. : "Piezoelectric transformer for integrated MOSFET and IGBT gate driver" in *Power Electronics, IEEE Transactions on*, Jan. 2006 Volume: 21, Issue: 1 On page(s): 56- 65
- [3] Wang, B.; Riva, M.; Bakos, J.; Monti, A., "Integrated circuit implementation for a GaN HFETs driver circuit," *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, vol., no., pp.901-906, 24-28 Feb. 2008
- [4] N. Rouger and J.-C. Crebier, "Integrated photoreceiver for an isolated control signal transfer in favour of power transistors," in *Power Semiconductor Devices and IC's, 2008. ISPSD '08. 20th International Symposium on*, May 2008, pp. 213–216.
- [5] Mazumder, S.K.; Sarkar, T : "Optically-activated gate control of power semiconductor device switching dynamics" in *Power Semiconductor Devices & ICapods, 2009. ISPSD 2009, 14-18 June 2009* Page(s):152 – 155
- [6] Brehaut, S. Costa, F : "Gate driving of high power IGBT by wireless transmission", *Power Electronics and Motion Control Conference, 2006. IPEMC 2006. CES/IEEE 5th International*
- [7] Ming Kong; Wei Yan; Wenhong Li, "Design of a synchronous-rectified buck bootstrap MOSFET driver for voltage regulator module," *ASIC, 2007. ASICON '07. 7th International Conference on*, vol., no., pp.974-977, 22-25 Oct. 2007
- [8] IR-IPS511, Datasheet Intelligent Power Switch 1 Channel High Side Driver in a TO-220FL Package, International Rectifier.
- [9] J.-C. Crebier and N. Rouger, "Loss free gate driver unipolar power supply for high side power transistors," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1565–1573, May 2008.
- [10] Sunderarajan S. Mohan, Maria del Mar Hershenson, Stephen P. Boyd, and Thomas H. Lee, "Bandwidth Extension in CMOS with Optimized On-Chip Inductors", *IEEE JOURNAL OF SOLID-STATE CIRCUITS*, VOL. 35, NO. 3, MARCH 2000
- [11] Datasheet HCPL2200/HCPL2219, Hewlett Packard.
- [12] Bhalerao, S.A.; Chaudhary, A.V.; Patrikar, R.M., "A CMOS Low Voltage Charge Pump," *VLSI Design, 2007. Held jointly with 6th International Conference on Embedded Systems., 20th International Conference on*, vol., no., pp.941-946, 6-10 Jan. 2007
- [13] Rouger, N.; Crebier, J.-C.; Aubard, L.; Schaeffer, C.; , "Toward Generic Fully Integrated Gate Driver Power Supplies," *IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on*, vol., no., pp.1866-1871, 6-10 Nov. 2006
- [14] T. Simonot, V. Gaude, J.-C. Crebier and N. Rouger, "3D hybrid integration and interconnection of a power transistor and its gate driver", *ECCE 2010*, paper accepted
- [15] F. Forest, E. Laboure, T. Meynard, and J.-J. Huselstein, "Multicell interleaved flyback using intercell transformers," *Power Electronics, IEEE Transactions on*, vol. 22, no. 5, pp. 1662–1671, Sept. 2007.