# Digital Sliding-Mode Controller For High-Frequency DC/DC SMPS

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# Letters

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***Abstract*—Digital control technique is becoming an attractive alternative for high-frequency switching mode power supply (SMPS). This paper introduces a fully synthesizable digital sliding-mode (SM) controller for high-frequency dc/dc SMPS. The proposed SM controller is associated with a digital pulsewidth modulation (DPWM) block to operate at constant and high switching frequency compared to already published approaches. The digital SM controller is experimentally validated by means of field-programmable gate array in a 4-MHz step-down converter with 10-bit analog-to-digital conversion (ADC) and 11-bit DPWM. Measured dynamic performances are superior to conventional digital controllers for dc/dc SMPS.**

***Index Terms*—Digital controller, field-programmable-gate-array (FPGA) implementation, high-frequency switching-mode power supply (SMPS), sliding-mode (SM) control.**

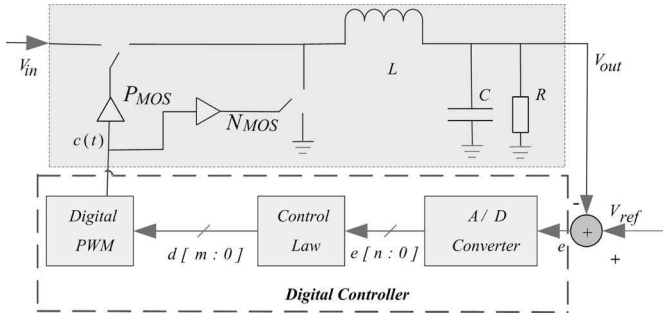


Fig. 1. Schematic of a digital controller for a step-down SMPS.

### I. Introduction

DIGITAL control technique has recently become an attractive candidate in the design of high-frequency dc/dc switching-mode-power-supply (SMPS) applications [1]–[3]. A schematic diagram of a digital controller for compact SMPS application is shown in Fig. 1 . The digital controller includes three functionality blocks: analog-to-digital conversion (ADC), control law, and digital pulsewidth modulation (DPWM). Due to emerging windows ADC techniques [1]–[3] and efficient DPWM methods [1]–[5], the issues of high-speed low-power dedicated ADC and DPWM for digital controller have become less important. However, due to the cost/complexity constraints existing in low-power dc–dc converters, few investigations concern the development of high-performance control algorithms. Most existing digital controller for high-frequency (in megahertz range) and low-power (several watts) SMPS converters are designed using linear PID control in field-programmable gate array (FPGA) and application specific integrated circuits (ASIC) implementations [1], [3], [4]. Nevertheless, because of the nonlinearity characteristics of SMPS in nature, it is difficult for a linear PID algorithm to offer high dynamic performances over wide operating conditions and parameter range [6], [7].

As SMPS represents a particular class of variable structure systems (VSSs), nonlinear control methods, especially a sliding-mode control (SMC) can enhance the dynamic performances of SMPS. Moreover, it is particularly suitable for high-frequency SMPS application as the control behavior approaches the ideal SMC with the increase in switching frequency [8]. To avoid the issue of variable switching frequency of the conventional hysteresis-modulation (HM) based SMC [9], recently an analog PWM-based SM controller has been proposed [10]. Unfortunately PWM-based analog SM controller shows limitations to control low-power high-frequency SMPS. Analog controllers are sensitive to analog component variations, and it is difficult to realize sophisticated control laws to improve the performances. By contrast, digital implementation overcomes the latter sensitiveness. Moreover, digital control enables to estimate signals in an indirect manner avoiding the use of critical sensors. Finally, advanced control laws may be implemented with a degree of reprogrammability. In [11], an FPGA implementation of a digital PWM-based SM controller is reported for a 23-kHz buck converter, where the DPWM adopts an 8-bit counter-comparator using a 6 MHz clock. With this design, a 1 GHz clock would be required for a converter operating at 4 MHz switching frequency, for example. The practical implementation for IC application with high switching frequency in megahertz range is then questionable. To our knowledge, the relevant experimental results of a SMPS with a digital SM controller operating at high-frequency ($>$1 MHz) have not yet been reported.

This paper proposes an original implementation of a PWM-based digital SM controller in FPGA for a step-down SMPS. The experimental validation comprises a discrete low-voltage

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buck converter operating at 4 MHz, a 10-bit discrete ADC and a 11-bit hybrid DPWM. An SM controller similar in complexity as a classical linear PID, but offering higher control performance, is presented in next section. The hybrid DPWM is presented in Section III.

## II. Proposed DPWM-Based SMC

The control objective of a SMPS is to keep the output voltage $V_o$ tracking the reference voltage $V_{\rm ref}$ with an acceptable ripple. Therefore, the sliding surface of the SM controller is chosen as [7]

$$S = K_1(V_{\rm ref} - V_o) + K_2\frac{d}{dt}(V_{\rm ref} - V_o) + K_3\int (V_{\rm ref} - V_o)dt \quad (1)$$

where $K_1$, $K_2$, and $K_3$ are control parameters of SMC. Considering the error-space phase plane $((V_{\rm ref} - V_o), \frac{d}{dt}(V_{\rm ref} - V_o))$, the system dynamics can be written as

$$\begin{cases} e_1 = V_{\rm ref} - V_o \\ \dot{e}_1 = e_2 \\ \dot{e}_2 = -\dfrac{1}{LC}e_1 - \dfrac{1}{RC}e_2 - \dfrac{V_{\rm in}}{LC}u + \dfrac{V_{\rm ref}}{LC} \end{cases} \quad (2)$$

with $R$ the load, $L$ the inductance, $C$ the capacitor, $u$ the control signal of switch, and $V_{\rm in}$ the input voltage.

With the equivalent control [12], the sliding-mode (SM) input $u$ can be determined using the invariance conditions by setting $S = 0$ and $\dot{S} = 0$ [8]

$$u = \frac{1}{V_{\rm in}}\left[V_{\rm ref} + LC\left(\frac{K_1}{K_2} - \frac{1}{RC}\right)e_2 + LC\left(\frac{K_3}{K_2} - \frac{1}{LC}\right)e_1\right]. \quad (3)$$

From (3), it can be seen that the SM controller involves the time differentiation of output voltage: $e_2 = -dV_o/dt = -i_C/C$, which results in the need of measurement for capacitor current $i_C$, and thus, increases the cost of the digital controller. Here, a simple numeric derivation is adopted to eliminate the need of hardware measurement

$$e_2 = -\frac{dV_o}{dt} = -\frac{V_o(n) - V_o(n-1)}{T_s} \quad (4)$$

where $V_o(n)$ and $V_o(n-1)$ are the output voltages in the $n$th and the $(n-1)$th cycle, respectively. Therefore, the proposed DPWM-based SM controller can be obtained as follows:

$$d = \frac{1}{V_{\rm in}}\left[V_{\rm ref} - LC\left(\frac{K_1}{K_2} - \frac{1}{RC}\right)\frac{V_o(n) - V_o(n-1)}{T_s}\right] + \frac{1}{V_{\rm in}}\left[LC\left(\frac{K_3}{K_2} - \frac{1}{LC}\right)(V_{\rm ref} - V_o)\right]. \quad (5)$$

This control algorithm is not more complex than a classical PID one and easy to implement in a FPGA or ASIC as it requires only few memories, multipliers, and adders.

To achieve the design specifications, the SMC must maintain the variable state trajectory on the sliding surface for all subsequent time. It is then necessary to ensure the existence conditions for a sliding surface. This task is performed using the Lyapunov's second method, where the Lyapunov's function is generally defined as $V = (1/2)S^2$. The following existence condition must be satisfied:

$$S\dot{S} < 0. \quad (6)$$

Rewriting (1) in Laplace form as

$$K_1 e_1(s) + K_2 s e_1(s) + K_3 e_1(s)\frac{1}{s} = 0 \quad (7)$$

the convergence dynamics can be chosen as a standard second-order system form to ensure the SMC system stability.

## III. 11-Bit Hybrid DPWM Design

The digital PWM-based SM controller requires a DPWM to do the digital-to-time conversion (DTC) to drive the transistors. This paper proposes an hybrid DPWM comprising a $\Delta$–$\Sigma$ block, a digital clock module phase-shift block (DCM) and a counter-comparator block. By comparison, Norris *et al.* [13] detail a pure $\Delta$–$\Sigma$ PWM (soft DPWM) and Batarseh *et al.* [5] describe a pure DCM (hardware) DPWM. The experimental testbench includes an 11-bit FPGA-based DPWM with a *5-bit* $\Delta$–$\Sigma$ block, a *4-bit segmented DCM phase-shift* block, and a *2-bit counter comparator* (see Fig. 2). Consequently, for operation at switching frequency $f_s$, the counter-comparator block only needs a $2^2 \cdot f_s$ clock. It dramatically alleviates the high clock-frequency requirement. For instance, when DPWM operates at $f_s = 4$ MHz, the proposed hybrid DPWM only needs a 16 MHz system clock. In contrast, the pure digital $\Delta$–$\Sigma$ DPWM in [13] needs a second-order loop filter, which is potentially less stable than the cascade of two first-order filters proposed here, and the segmented DCM phase shift in [5] would require a system clock of 1 GHz to achieve the 4 MHz switching frequency.

## IV. Experimental Results

The functionality of the proposed DPWM-based SMC is experimentally verified using a discrete buck converter with 3.0 V input and 1.5 V output voltage. A 10-bit discrete ADC (AD9203) is used in order to avoid limit-cycle oscillation [4]. The implementation of the proposed DPWM-based SM controller is performed on a Xilinx XC2VP30 FPGA with an external 16 MHz system clock. A very-high-speed-integrated-circuit Hardware Description Language (VHDL) design approach is used to synthetize the SM controller with Xilinx ISE development software. The test platform and its block diagram are shown in Figs. 3 and 4, respectively. The parameters of the SMPS are listed in Table I. The tests are currently performed up to 4 MHz due to frequency limits of the discrete SMPS.

The sliding-control parameters are determined by considering the second-order system stability condition and desired behavior. After simulation studies, the damming ratio $\zeta$ is set to 1 and undumped natural frequency is set to 1/15th of the switching frequency. A classical but optimal PID algorithm is considered for the sake of performance comparison with the proposed SM

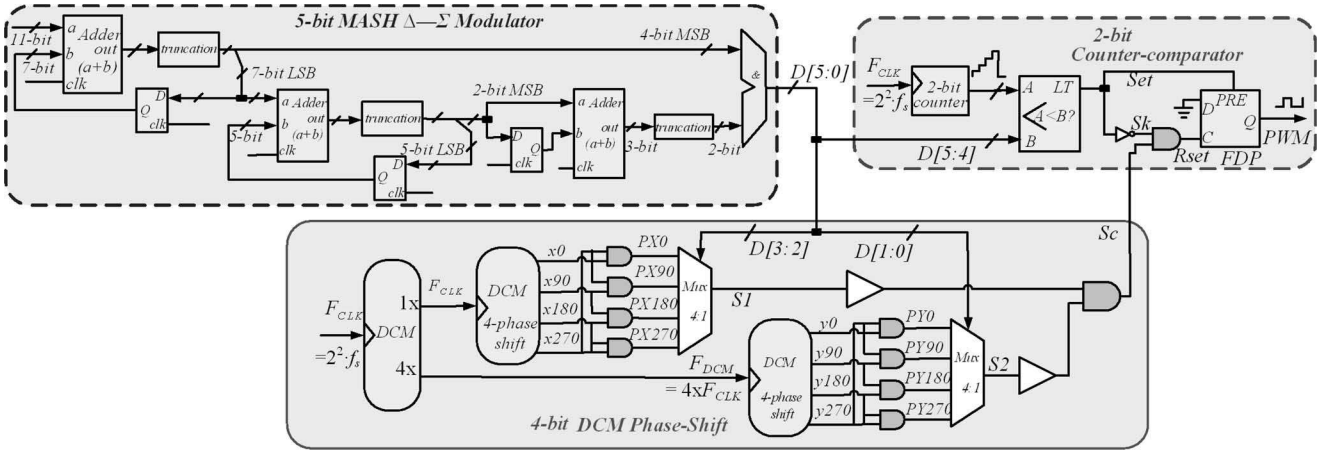



Fig. 2. Proposed 11-bit FPGA-based hybrid DPWM: 5-bit $\Delta$–$\Sigma$ modulator, 4-bit segmented DCM phase-shift and 2-bit counter comparator.

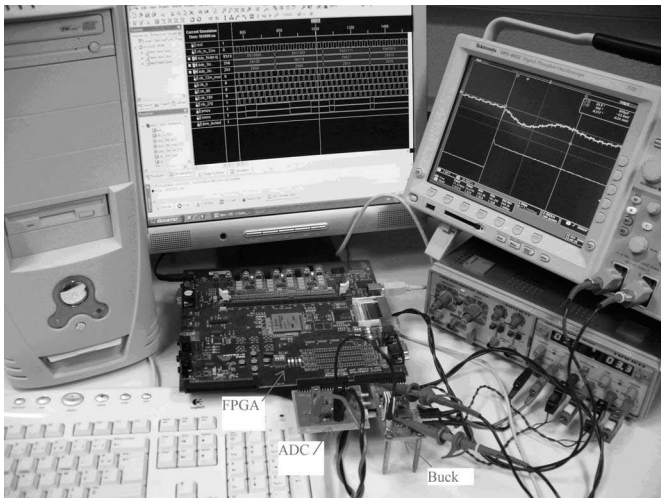



Fig. 3. Experimental test platform.

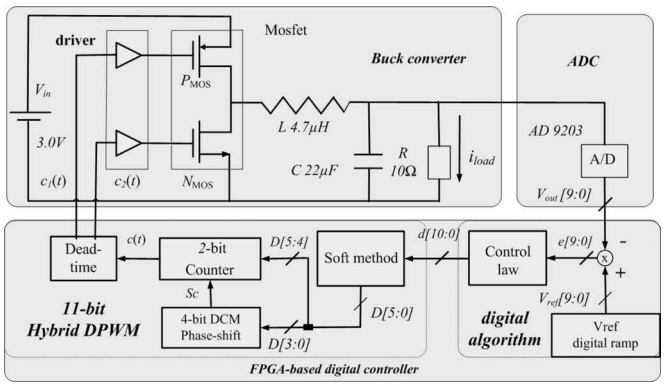



Fig. 4. Experimental test platform block diagram.

controller. The PID controller parameters are calculated so that the closed-loop dynamics corresponds to a second-order system with a resonant frequency, $\omega$, of 20 times the open-loop pulsation and a damping ratio, $\zeta = 0.7$. The PID discrete-time form

TABLE I
PARAMETERS OF THE DIGITALLY CONTROLLED SMPS

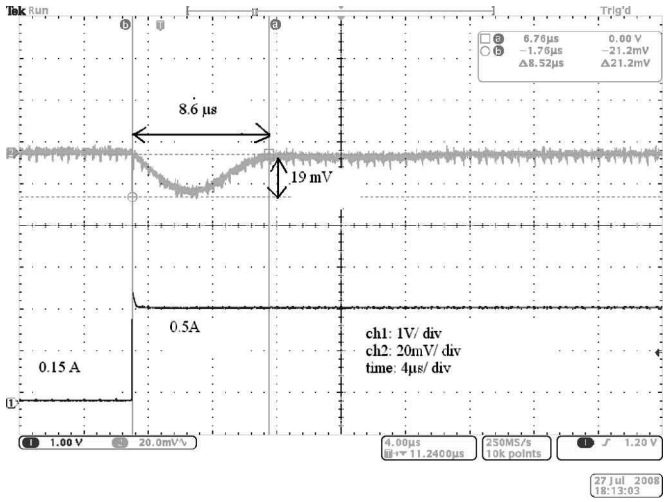
| | | |
|---|---|---|
| $Buck$ | Switching power converter | Step down |
| $R$ | Load | $10\Omega$ |
| $L$ | Inductor of power filter | $4.7\mu H$ |
| $C$ | Capacitor of power filter | $22\mu F$ |
| $V_{in}$ | Input voltage | $3.0V$ |
| $V_{ref}$ | Reference voltage | $1.5V$ |
| $f_s$ | Switching frequency | 4MHz |
| $SMC$ | Digital control algorithm | Sliding mode control |
| $ADC$ | AD9203 | 10-bit |
| $DPWM$ | Hybrid DWPM | 11-bit |
| $N_{Core}$ | Counter comparator resolution | 2-bit |
| $N_{DCM}$ | DCM phase-shift resolution | 4-bit |
| $N_{\Delta-\Sigma}$ | $\Delta$-$\Sigma$ resolution | 5-bit |
| $F_{CLK}$ | DPWM counter frequency | 16MHz |

comes as

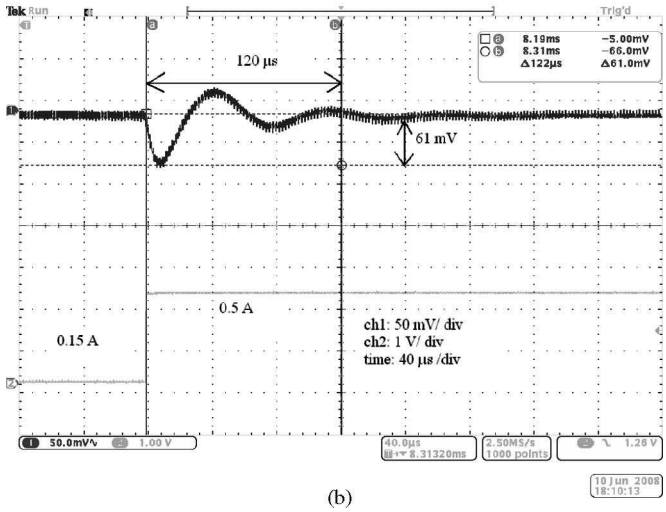
$$d[n] = a_1 d[n-1] + a_2 d[n-2] + b_0 e[n] + b_1 e[n-1] + b_2 e[n-2] \quad (8)$$

where $b_0 = 63.0649$, $b_1 = -125.4422$, $b_2 = 62.4044$, $a_1 = -0.7792$, and $a_2 = -1.7792$.

Fig. 5 shows the transient output voltage response of SM controller and PID controller for transient load from 0.15 to 0.5 A (10 $\Omega \rightarrow 3\ \Omega$). These results show that the dynamic response of SMC is very fast ($<8.6\ \mu$s) and the offset on the output voltage is also very small ($<19$ mV or 1.3%). Clearly, the proposed DPWM-based SM controller offers better disturbance rejection and faster speed of response than a classical PID.




(a)




(b)

Fig. 5. Transient output voltage response for 0.15–0.5 A load conditions: (a) SM controller, (b) PID controller.

## V. Conclusion

This paper presents a fully synthesizable DPWM-based digital SMC for low-power (some watts) and high-frequency (in megahertz and over) SMPS. The architecture contains a PWM-based SMC algorithm and an efficient hybrid DPWM. The proposed nonlinear SMC achieves a constant high switching frequency. Its hardware implementation is quite simple: only few memories, multipliers, and adders in FPGA/ASIC are needed. The hybrid DPWM combines a 5-bit $\Delta$–$\Sigma$ noise-shaping modulator with a 2-bit counter-comparator block. Instead of $2^{11} f_s$, the hybrid 11-bit DPWM architecture merely requires $2^2 f_s$ clock. It dramatically reduces the power consumption. The FPGA implementation is tested on a lab-scale buck converter (step-down SMPS) where the switching frequency is limited to 4 MHz. The experimental results validate the functionality of the proposed PWM-based digital SMC controller.

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