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Corentin Rizet, Jean-Paul Ferrieux, Philippe Le Moigne, Philippe Delarue, Alain Lacarney. Efficiency improvement in soft-switching three-level converters for high power UPS. IEEE Energy Conversion Congress and Exposition, 2010, Sep 2010, Atlanta, United States. 10.1109/ECCE.2010.5618089 . hal-00517982

**HAL Id: hal-00517982**

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Submitted on 6 Oct 2010

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# Efficiency improvement in soft-switching three-level converters for high power UPS

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**Abstract -- Efficiency of high power Uninterruptible Power Supplies (UPS) is a fundamental criterion regarding the permanent use of such a device. A state of the art on soft-switching over constraint of the UPS application has been made. The principle of Auxiliary Resonant Commutated Pole (ARCP) using autotransformer has been identified as the most interesting way to increase efficiency or switching frequency. Its application for multi-level converters has been studied. A simplified resonant pole has been proposed for both three-level rectifier and inverter used in UPS. The design criteria have been discussed. A single phase of a 125 kVA three-level UPS has been realized and tested. The concept has been validated.**

**Index Terms -- ARCP, multi-level, NPC, PFC, soft-switching, UPS, ZVS.**

## I. INTRODUCTION

This paper deals with both converters of an UPS. After introducing the UPS constraints, a state of the art of soft-switching used in order to increase efficiency is made. Then, the working principle used will be analyzed for the two-level converters. The topology of a simplified resonant pole will be described for both three-level rectifier and inverter of an UPS. The design will be set out. Finally the experimental results on the 125 kVA prototype will be discussed.

UPS are used in many applications for supplying energy with a high level of quality regardless of the grid. Most of the high power UPS work as two consecutive converters [1]. A rectifier provides a DC bus voltage from the grid and then an inverter generates a three-phase sinusoidal voltage (Fig. 1). DC bus voltage allows balancing a blackout of the grid during some time by energy storage. During UPS lifetime, efficiency

determines how much money the owners will spend and thus has become a critical point. The DC voltage level is set by the voltage level of the grid. Therefore, current level is imposed by the power. For a rated power over 100 kVA and a two-level topology, the switching frequency is around 5 kHz, due to the switching losses of the components used (usually an Insulated Gate Bipolar Transistor, IGBT).

A way to improve efficiency is the multilevel topologies. As described in [2], these topologies split the DC bus in several voltage sources. Thus the switching losses decreases as the voltage level switched. The quality of the waveforms is improved and then, the losses due to filtering are reduced. Nevertheless, the number of consecutive switches is risen, so the conduction losses too. In similar conditions, [3] achieves both better efficiency and higher switching frequency (around 10 kHz) with a three-level topology than a two-level one. But this frequency remains in the audible range, which may be unenviable in some applications like the data centers.

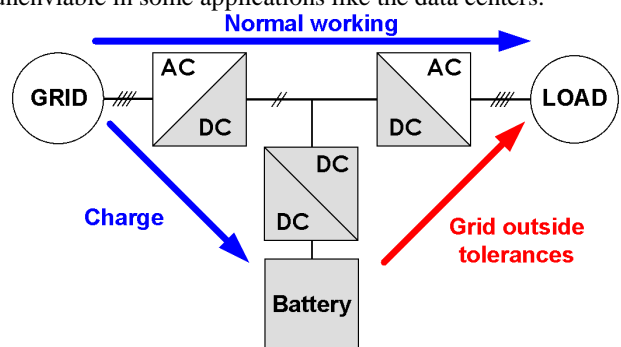


Fig. 1. UPS on-line

Another way is the soft-switching mode, which consists in cancelling the current or the voltage in the device before switching OFF or ON. Using a lossless snubber is therefore allowed for the other switching (ON or OFF). The conditions for cancelling can be introduced in the switching cell by the DC bus, by the load or locally around the switch. The main criterion to improve efficiency at this current level is to avoid conduction losses in the path of the main current. It means that only parallel topologies are suitable for. Efficiency must remain high at low current because of the low frequency alternative modulation. The voltage range of the main switches must be maintained. Auxiliary switches must work in soft-switching conditions. Regarding the industrial application, Pulse Width Modulation (PWM) must be maintained, and costs minimized. These constraints lead to the lossless snubber [4] and the resonant pole, in both zero current (ZCS) and zero voltage switching (ZVS) [5]-[9]. The auxiliary commutated resonant pole (ARCP), first described in [6], could be work with an autotransformer as auxiliary voltage source [7]-[9]. The main advantages are a half current cutback in the auxiliary switches and an open-loop control of the switching process. Reference [9] talks about an ARCP with an autotransformer in the neutral-point-clamped (NPC) three-level inverter, but this topology can not achieve the half-current cutback. References [10], [11] present the way to control safely an ARCP topology, taking into account the auxiliary losses. Derived from these concepts, a unidirectional resonant pole is described and tested in [12], [12] for a three-level power factor corrector (PFC) rectifier. The switching losses have been divided by two over the whole range of load (200 kVA). The low sizing of the auxiliary components and the simple and effective control make this resonant pole well-suited for the UPS.

## II. WORKING PRINCIPLE

ZVS turn-on, current rate control and snubber-assisted turn-off for the main devices are the key points of the ARCP. Fig. 2 shows a two-level ARCP inverter. The auxiliary switches  $T_{X1}$  and  $D_{A2}$  allow a resonant current  $I_R$  to flow in the resonant pole before the turn-on of the main switch  $T_1$ . The autotransformer  $T_P$  shares the resonant current between both auxiliary devices ( $T_{X1}$  and  $D_{A2}$ ). Its leakage inductance sets the current rate of the auxiliary current, then in the main devices ( $T_1$  and  $D_2$ ). The low current rate reduces the reverse-

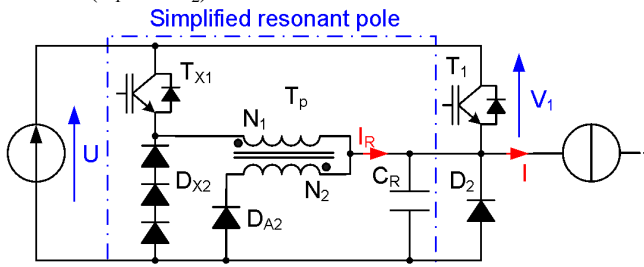


Fig. 2. Two-level simplified resonant pole converter

recovery losses of the main diode. After the turn-off of  $D_2$ , a resonance between the leakage inductance of  $T_P$  and the capacitor  $C_R$  swing the voltage  $V_1$  from  $U$  to zero, allowing the ZVS turn-on of  $T_1$ .

Fig. 3. shows the waveforms of the converter for a positive current, assuming its constant value during switching time. In the beginning, the switch  $T_1$  is ON, thus the voltage  $V_1$  is null. At the time  $t_1$ ,  $T_1$  is turned off. The main current  $I$  could go through the capacitor  $C_R$ . This snubber effect decreases the turn-off losses of  $T_1$ . Nevertheless, many charges must be gone out of the semi-conductor and causes mandatory losses. At  $t_2$ , when the voltage  $V_1$  is equal to the DC bus one, the diode  $D_2$  is turned-on. Before the turn-on of the main switch, the auxiliary switch  $T_{X1}$  is turned-on at  $t_3$ . The DC bus voltage is applied on the autotransformer. The ratio  $m$  (1) sets the mid-point voltage of the auxiliary pole, leading to the rise of the auxiliary current  $I_R$ . Thus the current in  $D_2$  ramps down. The leakage inductance of the autotransformer limits the current rate in the resonant pole, and then the recovery losses are decreased in the main diode.

At  $t_4$ ,  $D_2$  is turned-off. A resonance between the leakage inductance and the capacitor  $C_R$  tends to decrease the voltage  $V_1$  to zero. At  $t_5$ , by setting  $m$  above  $\frac{1}{2}$ ,  $I_R$  remains higher than the main one when  $V_1$  becomes null. So the anti-parallel diode of  $T_1$  begins to flow the remaining current. It stopped the resonance. Between  $t_5$  and  $t_6$ ,  $T_1$  may be turned-on at ZVS. The voltage across the secondary winding of the autotransformer is now the DC bus voltage, so the auxiliary current ramps down as the current in  $T_1$  rises up. At  $t_7$ , the auxiliary diode  $D_A$  is turned-off. The auxiliary current remains constant at a level which depends on the magnetization of the autotransformer. After a certain time  $T_{MAX}$ ,  $T_{X1}$  may be turned-off at ZCS. Some diodes ( $D_{X2}$ ) make the cancellation of the autotransformer flux possible. Between  $t_8$  and  $t_9$ , the DC bus voltage is applied across the upper part of the primary winding ( $N_1$ ). Thus the voltage across the auxiliary diode  $D_A$  is higher than twice the DC bus voltage (2). A parasitic current could flow in the resonant pole when the diode  $D_2$  is on. Three diodes should be arranged in a serial way to avoid this. The resonant current can not pass through these diodes, so the auxiliary losses should not increase. Both capacitors may be used as the resonant one. Using only one capacitor decreases the overvoltage due to a resonance between the parasitic DC bus inductance and it. As described in [10] and [12], a delay time ensures the turn-on of  $T_1$  and the turn-off of  $T_{X1}$  in the case of default. This topology provides a robust, simple and low loss solution.

$$m = \frac{N_2}{N_1 + N_2} \quad (1)$$

$$BV_{DA} = \frac{U}{1 - m} \quad (2)$$

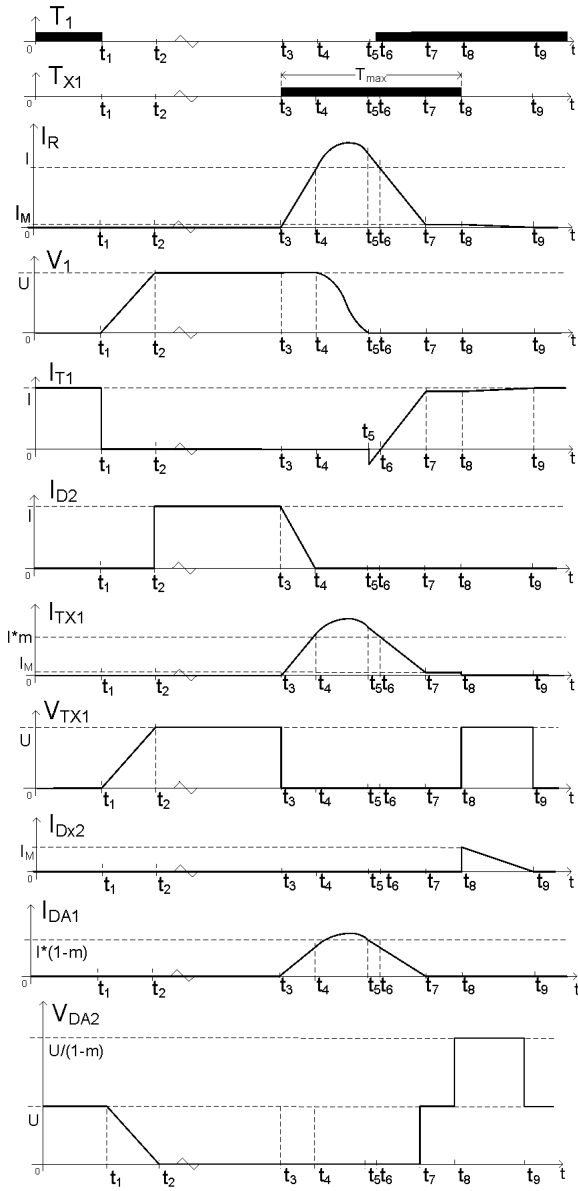


Fig. 3. Waveforms of the two-level converter

### III. APPLICATION IN A THREE-LEVEL UPS

Efficiency is a key point in the UPS market regarding the permanent use of such a device. The three-level topologies have achieved a better efficiency than two-level ones, by the use of better components (600 V rated IGBT), less voltage level switched and less filtering needs. The work of the rectifier at the maximum voltage level sets DC bus voltage from 800 V in European market to 900 V in North-American ones. This work focuses on a 125 kVA UPS, with a power factor of 0.9.

Fig. 4 describes one phase of a three-level simplified resonant pole UPS. The rectifier is made on the double-boost topology, used as a power factor corrector (PFC). It can be split in both two-level boost converters. It means the current of both cells ( $T_{E2}/D_{E1}$  and  $T_{E3}/D_{E4}$ ) is always positive, or negative. Therefore, each boost works with its simplified resonant pole as described in [12].

The inverter is based on the NPC topology and works with a bidirectional power flow. At the nominal point (power factor of 0.9), the active switching cells ( $T_{S1}/D_{C2}$  and  $T_{S4}/D_{C3}$ ) carry the most of the switching losses, around 90 %. In order to reduce the cost of the soft-switching topology, only these two cells have been assisted by a resonant pole. Nevertheless, the snubber capacitors  $C_{R2}$  and  $C_{R3}$  could suffer from a hard discharge during the reactive phases (an output voltage sign different from the output current one). The switching of the reactive cells ( $T_{S3}/D_{S1}$  and  $T_{S2}/D_{S4}$ ) swings the voltage across the capacitors. A way to protect both capacitors and switching devices is to modify the control of the topology. When the switching cell  $T_{S3}/D_{S1}$  is active, the main current is negative. No current flows through the component  $T_{S2}$ , it may be switched off. The switching cell changes to  $T_{S3}/D_{S2}$ , no matter for the output waveform or the losses. The control of the other reactive cell ( $T_{S2}/D_{S3}$ ) is the same with a positive current. The control strategy is illustrated in for the first switching cell. Firstly, the voltage across  $T_{S1}$  is measured and compared to zero. If the voltage is null, then the turn-on is allowed. After a delay time  $T_{MAX}$ , the turn-on should be effective. The turn-off is usual. Secondly, a simple delay time

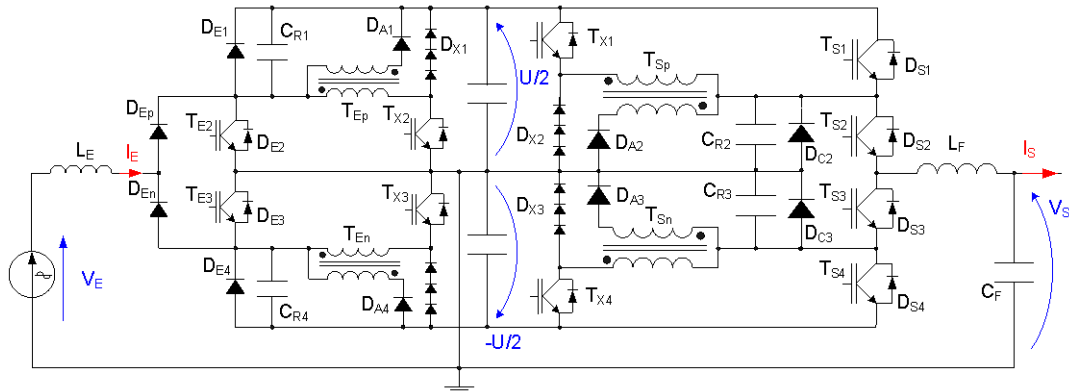


Fig. 4. Three-level soft-switching UPS

$T_{MAX}$  (longer than normal soft-switching time) controls the auxiliary device  $T_{X1}$ . Finally, a sensor looks for the sign of the current in the output inductor and turns-off the right component.

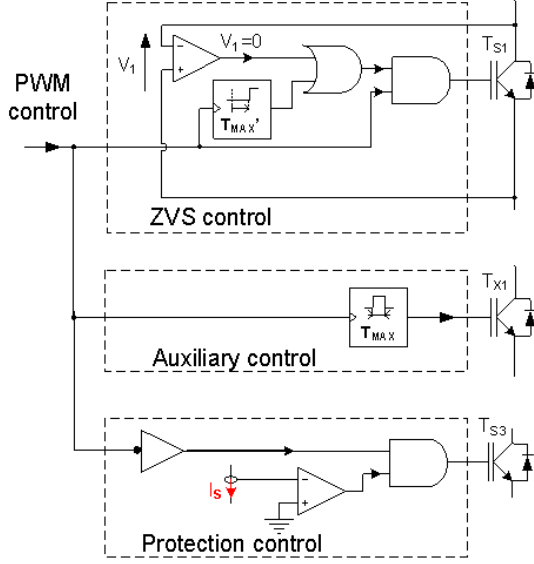


Fig. 5. Control of the proposed converter

#### IV. DESIGN CONSIDERATIONS

The design of the simplified ARCP topology needs a compromise between the level of losses and the duration of the switching processes. In order to reduce the losses of the main diodes by decreasing the current rate, the equivalent resonant inductance  $L_R$  may be defined by (3, 4). It is assumed that the current tail of IGBT could only decrease the voltage rate by reducing the capacitor current. The snubber capacitors may be chosen by (5), leading to decrease the turn-off losses of IGBT. Moreover, the IGBT used as main devices need some time to turn-on. The ZVS control is made in the driver, to minimize the delay time between the cancellation of the voltage and the effective turn-on. This time has been measured at 300 ns. This delay time is created in the resonant pole by the ratio  $m$  and the current rate (6). If this ratio equals  $\frac{1}{2}$ , there is no delay time.

$$\frac{di}{dt_{rise}} = \frac{m}{L_R} \cdot \frac{U}{2} \quad (3)$$

$$\frac{di}{dt_{fall}} = \frac{(1-m)}{L_R} \cdot \frac{U}{2} \quad (4)$$

$$\frac{dv}{dt_{OFF}} \leq \frac{i}{C_R} \quad (5)$$

$$t_d = \sqrt{L_R \cdot C_R} \cdot \sin \left[ a \cos \left( 1 - \frac{1}{m} \right) \right] \quad (6)$$

$$t_{ON} \leq (2-m) \cdot \left[ \frac{2}{U} \cdot \frac{L_R}{m \cdot (1-m)} \cdot i + \sqrt{L_R \cdot C_R} \cdot \left[ a \cos \left( 1 - \frac{1}{m} \right) + \frac{m}{1-m} \cdot \sin \left( a \cos \left( 1 - \frac{1}{m} \right) \right) \right] \right] \quad (7)$$

This time depends on the inductance  $L_R$ , due to the resonant current rate (3, 4). But the duration of the whole process is mainly driven by this value, owing to the charging and discharging time of the inductance (7). The needed demagnetizing time has been taken into account. This is illustrated in Fig. 6. The ratio  $m$  has limited effects on the total time. On the other side, the ratio sets the breakdown voltage of the auxiliary diode  $D_A$  and shares the resonant current between this diode and the auxiliary IGBT  $T_X$ . The losses of the auxiliary devices tend to decrease the delay time. So the higher the ratio is, the safer the switching process is and the faster the switching is, but the more unbalanced both auxiliary currents are and the higher the blocking voltage is. Here the choice for the ratio  $m$  is 0,66. The auxiliary diode is a 1700 V-rated. To reach the needed delay time, the equivalent inductance  $L_R$  must be equal to 350 nH. It is mostly the turn-on delay time of the IGBT which drives the design of the auxiliary resonant pole.

In order to minimize the conduction losses in the autotransformer, the number of turns has to be minimized. So the ratio between core area and winding area must be as large as possible. Finally the total number of turns is 15 (5 turns for  $N_1$ , 10 turns for  $N_2$ ). The resonant current has a large frequency spreading (up to 1 MHz). As a consequence, the windings must be designed to contain the increase of their apparent resistance at high frequency. A Litz wire has been use, with 400 wires with a 100  $\mu$ m diameter. The autotransformer has been designed as a planar with three concentric windings. The secondary winding  $N_2$  is shared in two parts, with the winding  $N_1$  between each part. By spacing correctly each part, a sufficient leakage inductance is created, and the AC resistance has been minimized.

The intrinsic current represents the energy needed to swing the capacitor voltage. The peak of the auxiliary current follows the main one plus the intrinsic current (8). Snubber capacitors have been set at 94 nF. Then the intrinsic current

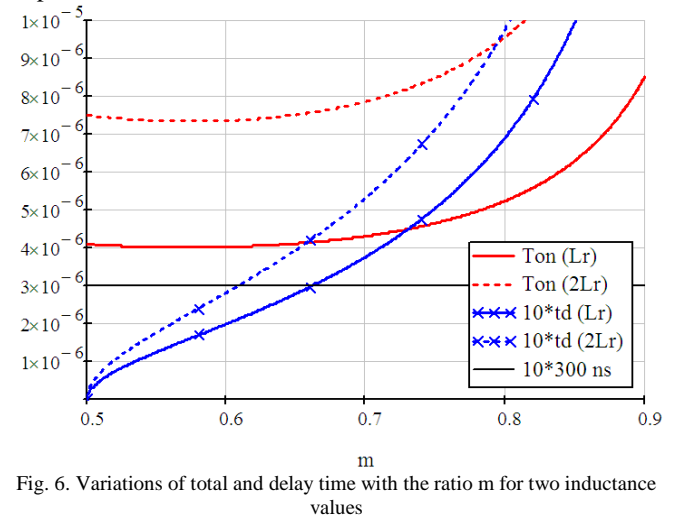


Fig. 6. Variations of total and delay time with the ratio  $m$  for two inductance values

equals 150 A, in comparison to the main RMS one that equal 180 A.

The total process time is set around 4  $\mu$ s. Assuming a dead time of 2  $\mu$ s, the minimum duty cycle have to be more than 10 %. According to the three-level topology, these duty cycles happen when the voltage reference crosses the zero level. It leads to a severe distortion on the main current.

The main IGBT have been rated at 400 A, regarding to the high crest factor of the RCD load. This type of load leads to a factor 3 between the maximum current and the RMS current (180 A). Thus two identical legs have been built. Each leg has a 200 A/650 V-rated devices, which are connected by a parallel path in order to use little package, according to the size of the snubber capacitors. The auxiliary switches must be chosen regarding their maximum current (9). Usually, a factor from 3 to 5 between the maximum current and the current range is set, depending on the type of semiconductors used (diodes or different IGBTs). Here, a 100 A/600 V-rated IGBT has been chosen as auxiliary device. Similarly, the auxiliary diodes are 75 A/1700 V-rated devices (10). The auxiliary resonant pole increases the overall cost of the UPS by around 10 %.

$$I_R \leq i + m \cdot \frac{U}{2} \cdot \sqrt{\frac{L_R}{C_R}} \quad (8)$$

$$I_X = m \cdot I_R \quad (9)$$

$$I_A = (1 - m) \cdot I_R \quad (10)$$

## V. EXPERIMENTAL RESULTS

### A. "One-shot" test

In order to validate the working process of the simplified resonant pole, an experimental prototype has been built and tested. A "One-shot" bench test has been set to easily look the switching process. First, Fig. 7 shows the whole process (turn-off and turn-on) of the positive active cell ( $T_{S1}/D_{C2}$ ) for a positive current (400 A).

Fig. 8 focuses on the ZVS switching of the inverter, for the same cell and for a 500 A current. The resonant current  $I_{R,S}$  linearly grows from zero to the main one  $I_S$  before swings with the voltage  $V_{ce}$  and decreases, as described before.

The detection of the zero voltage is illustrated by the switching process of the rectifier (Fig. 9). When the voltage across the IGBT crosses the zero level, the state of the gate voltage begins to swing to its high level. The continuity of the current in the IGBT ( $I_c$ ), half the main current ( $I_E$ ), proves the effectiveness of the on state of the IGBT. As a conclusion, the voltage shifting of the autotransformer is sufficient to balance both the ON-switch delay of the IGBT and the extra losses in the auxiliary devices. In Fig. 7, the parasitic resonance between the capacitors and the DC bus leakage inductance can be seen. The overvoltage due to this resonance remains under 150 V, so the converter is able to work with a DC bus

value as high as 500 V (with the 650 V-rated IGBT).

The UPS have to be able to supply a load with a large crest factor. Thus the prototype has been tested over a large current range (from 0 to 600 A). As said before, the overvoltage remains on acceptable value at a 600 A-level switched. The recovery phenomenon of the auxiliary diode leads to a negative peak on the resonant currents ( $I_{R,P}$  and  $I_{R,E}$ ).

### B. Steady-state operation

With its control board, the prototype is able to work as an UPS phase, meaning the rectifier charges the DC bus and the inverter supplies the load as the grid. Fig. 10 is the waveforms on the rectifier part, between the converter and the filter, for the nominal load. The positive resonant current ( $I_{RE,P}$ , in black) follows the main one. A zoom at the switching period lets us to see the switching process (Fig. 11). The waveforms of the inverter (Fig. 12) show the issue of the minimum duty cycle, leading to a severe distortion on the converter current

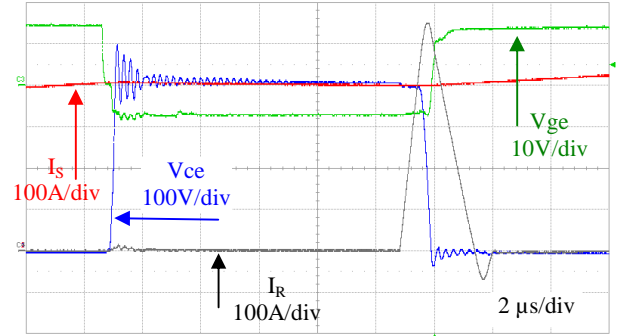


Fig. 7. Waveforms of the inverter (400 V, 400 A)

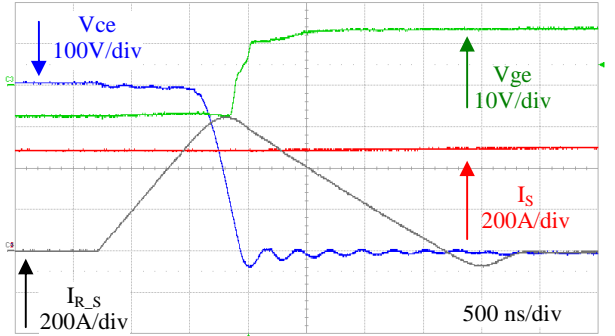


Fig. 8. Switch ON of the inverter (400 V, 500 A)

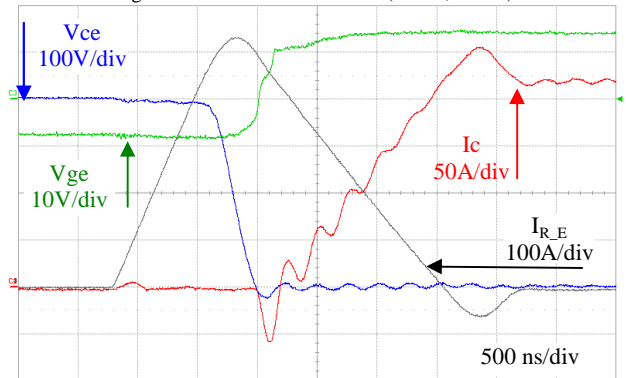


Fig. 9. Waveforms of the rectifier (400 V, 400 A)

( $I_{COM,S}$ , in red). This distortion has been visible on the output voltage  $V_S$  (in black). This issue could be addressed by a variable delay control, following the main current.

The measurement of the efficiency will be achieved by both electrical and thermal measures. By measuring the difference between the output and the input electrical power, the efficiency may be estimated. Many thermal sensors have been added on the prototype, especially on the heatsink. The amount of temperature could be measured. A calibration of the thermal properties of the prototype could be done by imposing a continuous current in the IGBT and measuring the power needed to obtain the same amount of temperature in the heatsink. The losses are directly measured with a quite good precision. The first measures show a half point increase at the nominal load, leading to an efficiency of 96 %. Other measures are going to assess more precisely the gain.

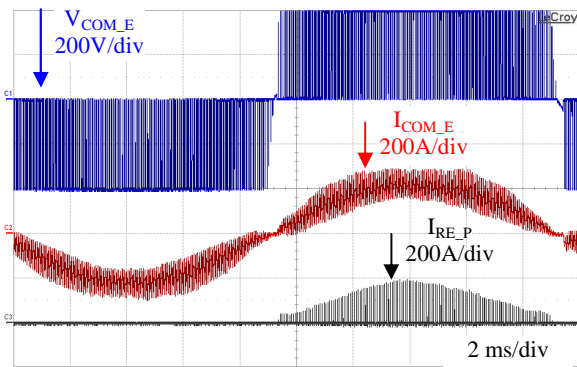


Fig. 10. Steady-state waveforms of the rectifier

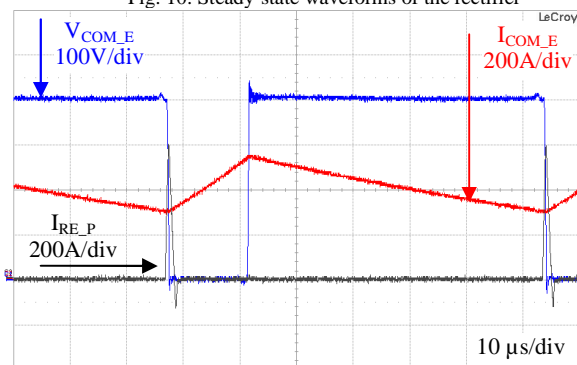


Fig. 11. Steady-state switching waveforms of the rectifier

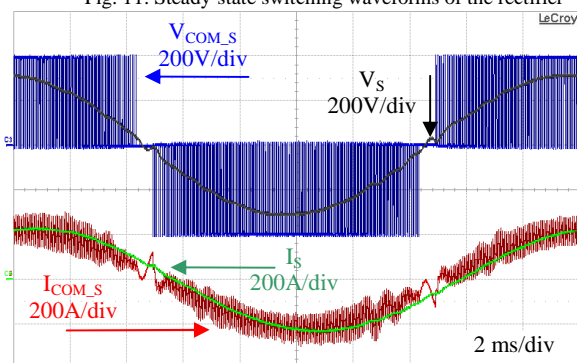


Fig. 12. Steady-state waveforms of the inverter

## VI. CONCLUSION

This work proposes a high efficiency topology for high power UPS. While using a three-level topology, a two-level unidirectional resonant pole may be used on both rectifier and inverter part. Usual control of the NPC topology has been modified to allow the work of the resonant pole. A simple open-loop control by time delay has proved a good robustness. A prototype has been carried out at 125 kVA of nominal power. The concept has been validated in steady-state operation. The measurements have shown the efficiency up to 96 % for both conversions.

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