Power- Supply Network Modeling

Jean-Luc Levant, Mohamed Ramdani, Richard Perdriau

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Jean-luc LEVANT*, Mohamed RAMDANI**, Richard PERDRIAU**
* ATMEL Nantes (jean-luc.levant@nto.atmel.com)
** Ecole Supérieure d'Electronique de l'Ouest Angers (mohamed.ramdani@eseo.fr, richard.perdriau@eseo.fr)

Abstract
This work deals with the extraction of ICEM parameters and its validation on the power supply network of a 8-bit microcontroller. The objective of the ICEM model [1] (Integrated Circuit Electromagnetic Model) for Components is to propose electrical modeling for conducted and radiation emission prediction [2]. The ICEM model is based on two sub-models. The first one models the power network of the I.C. and the second one models the I.C. activity as a current generator. The ICEM model can be used by the I.C. supplier to check the performances of the package, the number of power pins, and the noise rejection on analogue parts, ... The electronic system suppliers will use the model to optimize the power network and the decoupling network of the PCB and finally the level of conducted and radiated emissions. In this paper, only the power network modeling of the 8-bit microcontroller core is discussed. Two methods can be used to model the power network of the I.C. The first one is based on the extraction of the parasitic elements during the design phase (silicon lay-out, package, bond wires, ...). The second one, discussed in this paper, is based on the measurement when a silicon or an equivalent design is available. These two methods are presented in the ICEM cookbook.

1. Introduction

To carry out this work, a board was designed such a way that the following goals can be achieved : IC's power supply network modeling, I/Os electrical modeling, IC's external power supply modeling, noise rejection between core and I/Os modeling. Thanks to this, predicting the noise rejection between different grounds as well as studying the influence on the performances of analogue and digital functions become possible. In this paper, only the power network modeling of the core logic of the 8-bit microcontroller is demonstrated. The principle is exactly the same for the other power pins.

2. Setup measurement

2.1 Power supply topology of the 8-bit microcontroller

Figure 1 shows the amount of pairs of power supplies and their locations in a microcontroller. There are three pairs of power supply pins dedicated to I/Os interfaces and two pairs dedicated to the core. Each analogue function (PLL, ADC, USB) has its power supply pin.

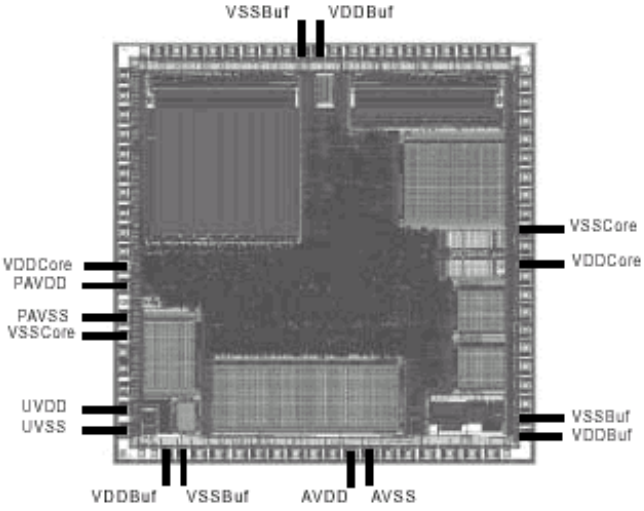


Figure 1: VDD/ VSS network of the microcontroller

2.2 Setup measurement

Figure 2 shows the setup used to model all the separated VDD pins. A network analyzer is used to extract the RLC model of each pin. A mechanical implementation of the microcontroller is directly linked to the network analyzer.

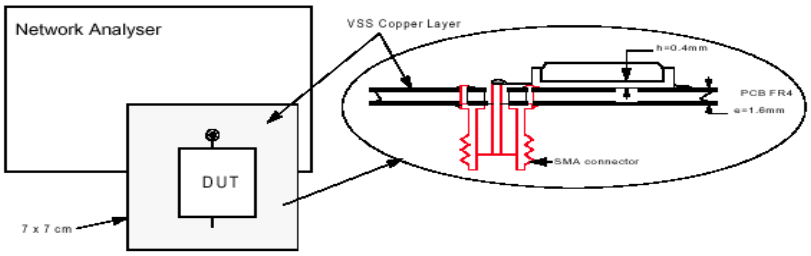


Figure 3 Hardware setup measurement.

For multiple pin modeling, the hardware setup is slightly modified.

3. Principle of this methodology

The presented analysis is based on an electrical model such as the Spice model. The bandwidth of the current consumed by the I.C. is 300MHz. Above this maximum frequency, the level of harmonics is low enough to not influence the level of conducted and radiated emissions. On the other hand, the length of the physical connexions (package, PCB traces, ...) is small enough to not consider the transmission line model. So the lumped model (RLC) is used to model the VDD and VSS pins as well as the pair of VDD/VSS pins.

The principle of this method is based on the measurement of the RLC model for each pin and pair of VDD/VSS pins. A network analyser and a hardware setup are used. The hardware setup consists of a SMA connector and a PCB where the I.C. is installed in order to extract the RLC model. This setup is modeled first. Figure 4 displays the PCB impedance (right) and the SMA impedance effect (middle). The electrical equivalent model is shown on the left side.

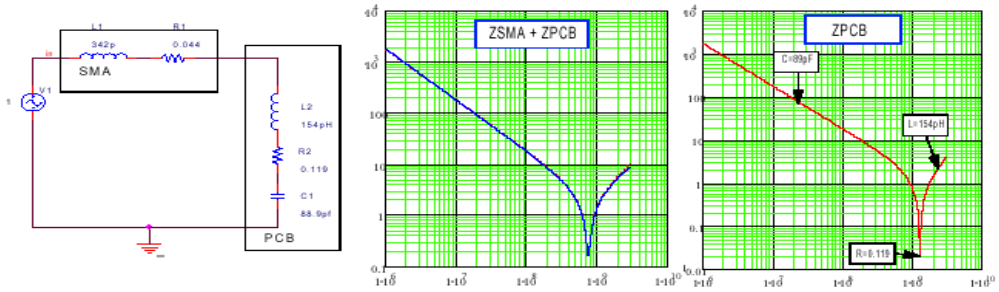


Figure 4: PCB and SMA model

4. VDD and VSS power network modeling

Different pairs of pins previously shown (figure 1) were measured and modeled. Each measurement is compared to the corresponding Spice model. Only some examples are shown in this paper. Figure 5 shows the setup used to model the VDDC1 and VDDC2 configuration (left) and plots the impedance of the VDDC1 and VDDC2 configuration versus the frequency(right). The dashed line curve is based on the Spice model. The electrical equivalent model is also given . This shows a good correlation in the frequency bandwidth of interest. The same method was applied on VSSC1 and VSSC2.

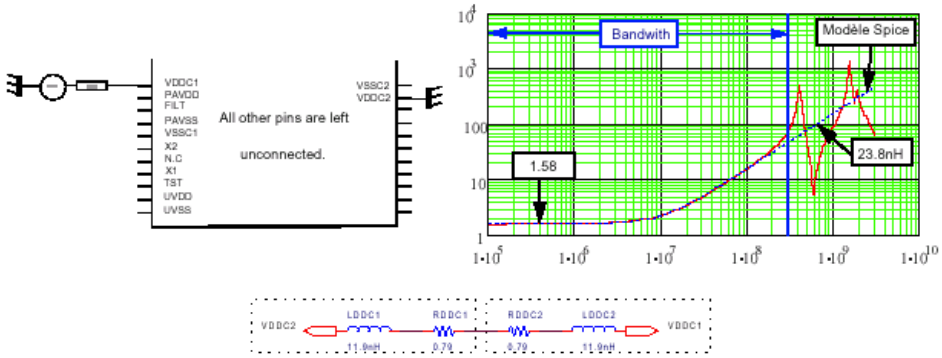


Figure 5: Measurement and model for VDDC1 and VDDC2 configuration

The VSSC1 and VSSC2 pins are modeled with the same method.

Figure 6 shows the setup used to model the pair of VDDC1 and VSSC1 pins and plots the impedance of the model and the measurement of the pair of pins. There is a good correlation in the frequency band of interest. The influence of the PCB and the SMA connector is shown on the plot.

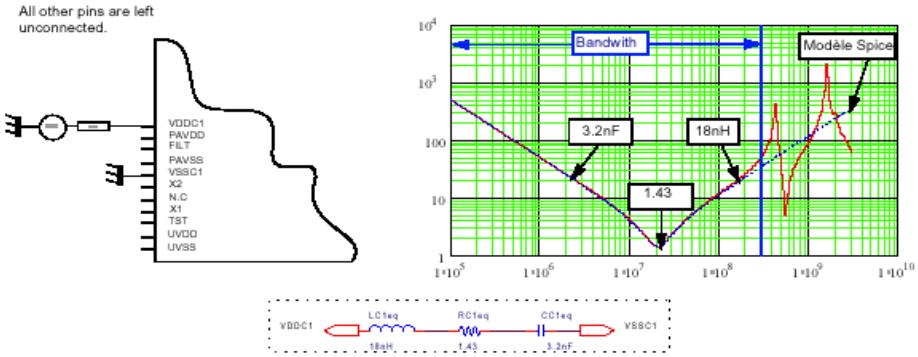
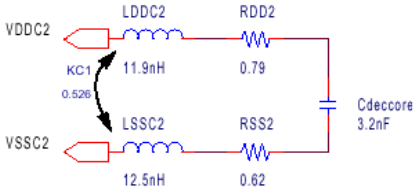


Figure 6: Impedance of the VDDC1 and VSSC1 power pins : simulation curve(blue) and measurement curve (red).

The RLC model of each VDD and VSS pin as well as the VDD/VSS pair of pins are well-known now. The magnetic coupling factor can be computed with the formula shown below.



$M = KCn\sqrt{LDCn.LSCn}$ where M is the mutual inductance.

The complete model of the VDDC1/VSSC1 and VDDC2/VSSC2 network is shown in figure 7. In this figure the prediction of the impedance of the complete model as well as the measurement are shown. The correlation is very good .

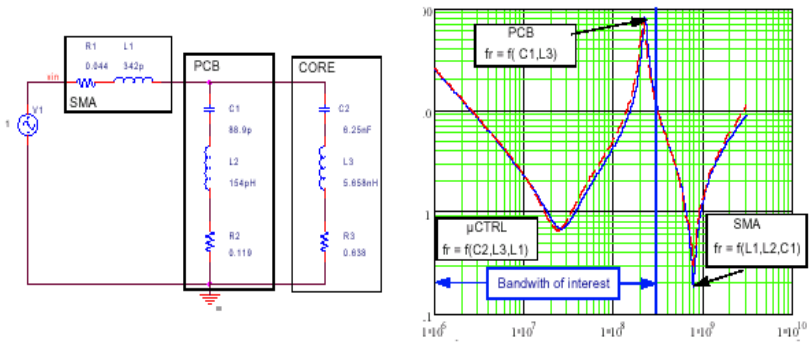


Figure 7. Impedance of the power-supply network: simulation curve(blue) and measurement curve (red).

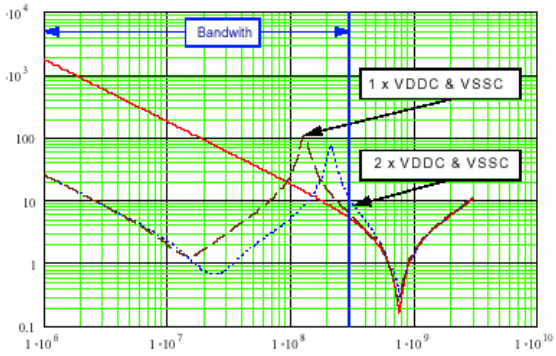


Figure 8: Number of pairs pins effect

The pairs pins amount effect on the impedance has also been studied as shown in figure 8. The full Spice system and the corresponding results are given in figure 9. The full Spice system and will be used for all the predictions around the logic core.

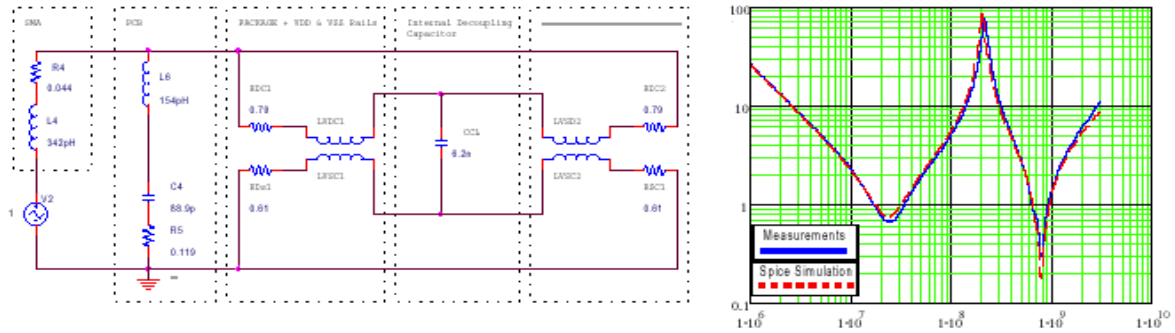


Figure 9: Full Spice model and measurement

5. Conclusion

In this paper, a modeling method of the I.C. power network has been shown . The results of the correlation between the prediction and the measurement are very good. It is important to notice two major points to achieve a good model. First of all, the model used has to be defined according to the electrical characteristics of the current flowing in the power network. It is easy to extract a RLC model . It is more difficult to extract a model based on a transmission line. Only the RLC model is presented in this paper. Secondly, the hardware setup has to be optimised and modeled in order to not include it in the I.C. model. It is done easily with a network analyser. The power network model of the other VDD/VSS pins are modeled in such ways.

[1] International Electro-technical Commission " IEC 62014-3: EMC for Component – Part 3: Integrated circuits Electrical Model (ICEM), ", IEC standard proposal, 2002
[2] International Electro-technical Commission "IEC 61967: Integrated Circuits, Measurements of Conducted and Radiated Electromagnetic Emission", IEC standard, 1999