HAL
open science

A Compact Model for the Ballistic Subthreshold Current in Ultra-Thin Independent Double-Gate MOSFETs

Daniela Munteanu, Mathieu Moreau, Jean-Luc Autran

To cite this version:

Daniela Munteanu, Mathieu Moreau, Jean-Luc Autran. A Compact Model for the Ballistic Subthreshold Current in Ultra-Thin Independent Double-Gate MOSFETs. Molecular Simulation, 2009, 35 (06), pp.491-497. 10.1080/08927020902801548 . hal-00515080

HAL Id: hal-00515080

https://hal.science/hal-00515080v1

Submitted on 4 Sep 2010

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Molecular Simulation
Journal of
Experimental Nanoscience
Taylor & Francis
Taylor & Francis Group

A Compact Model for the Ballistic Subthreshold Current in Ultra-Thin Independent Double-Gate MOSFETs

Journal:	*Molecular Simulation/Journal of Experimental Nanoscience*
Manuscript ID:	GMOS-2008-0205.R2
Journal:	Molecular Simulation
Date Submitted by the Author:	26-Jan-2009
Complete List of Authors:	Munteanu, Daniela; IM2NP-CNRS Moreau, Mathieu; IM2NP-CNRS Autran, Jean-Luc; IM2NP-CNRS
Keywords:	ballistic transport, Independent Double-Gate MOSFET, compact modeling, quantum effects, subthreshold current model

For Review Only
SCHOLARONE™
Manuscripts

A Compact Model for the Ballistic Subthreshold Current in Ultra-Thin Independent Double-Gate MOSFETs

D. Munteanu, M. Moreau, J.L. Autran*

Intitute Materials Microelectronics Nanoscience of Provence (IM2NP, UMR CNRS 6242)

Bâtiment IRPHE, 49 rue Joliot-Curie, BP 146, F-13384 Marseille Cedex 13, France

(*also with Institut Universitaire de France)

Corresponding author :

Dr. Daniela MUNTEANU

IM2NP, UMR CNRS 6242
Bâtiment IRPHE – BP 146
49, rue Joliot Curie
F-13384 MARSEILLE Cedex 13, France
Phone :+33 4 96 13 98 19
Fax : +33 4 96 13 97 09
E-mail : daniela.munteanu@univ-provence.fr

For Peer Review Only

ABSTRACT

We present an analytical model for the subthreshold characteristic of ultra-thin Independent Double-Gate (IDG) MOSFET working in the ballistic regime. This model takes into account short-channel effects, quantization effects and source-to-drain tunneling (WKB approximation) in the expression of the subthreshold drain current. Important device parameters, such as off-state current or subthreshold swing, can be easily evaluated through this full analytical approach. The model can be successfully implemented in a TCAD circuit simulator for the simulation of IDG MOSFET based-circuits.

Keywords: Independently Driven Double-Gate MOSFET, ballistic transport, quantum effects, subthreshold current model

For Peer Review Only

1. Introduction

Double-Gate (DG) MOSFETs are extensively investigated because of their promising performances with respect to the ITRS specifications for deca-nanometer channel lengths. The main advantage of this architecture is to offer a reinforced electrostatic coupling between the conduction channel and the gate electrode. A double-gate structure can efficiently sandwich the semiconductor element playing the role of the transistor channel, which can be a Silicon thin layer or nanowire, a Carbon nanotube, a molecule or an atomic linear chain [1]. In spite of excellent electrical performances due to its multiple conduction surfaces, conventional DG MOSFET allows only three-terminal operation because the two gate electrodes, i.e. the front gate and the back gate, are generally tied together. DG structures with independent gates have been proposed [2]-[3], having a four terminal operation. Independent Double-Gate (IDG) MOSFETs offer additional potentialities, such as a dynamic threshold voltage control by one of the two gates, transconductance modulation, signal mixer, in addition to the conventional switching operation. Thus, IDG MOSFETs are promising for future high performance and low power consumption very large scale integrated circuits. However, one of the identified challenges for IDG MOSFET optimization remains the development of compact models [4]-[7] taking into account the main physical phenomena (such as short-channel effects, quantum confinement, ballistic transport) governing the devices at this scale of integration. In this work, an analytical subthreshold model of ultra-thin IDG MOSFETs working in the ballistic regime is presented. The present approach captures the essential physics of such ultimate devices: short-channel effects, quantum confinement, thermionic current and tunneling of carriers through the source-to-drain barrier. Important device parameters, such as the off-state current (I_{off}) or the subthreshold swing, can be easily evaluated through this full analytical approach which also provides a complete set of equations for developing equivalent-circuit model used in ICs simulation.

For Peer Review Only

2. Physics of the ballistic transport

In nanoscale MOSFETs with channel lengths less than about 50 nm, the relaxation times of the carriers indicate that the drain current will have an intermediate character between drift-diffusion and ballistic/quasi-ballistic transport [8]. Then, ballistic transport has to be considered in the modeling of ultra-short Double-Gate devices. Since the conventional Drift-Diffusion model (usually used in device simulation) fails at describing ballistic transport, new specific models have to be developed this regime. The highest value of the source-to-drain current which can be obtained for a given MOSFET geometry corresponds to the pure ballistic current limit. As the channel length is increased, the current decreases from this maximum value due to scattering effects. The transport makes a transition from the ballistic to quasi-ballistic or drift-diffusive regime with the longer channel lengths [9]. The carrier transport in the channel is considered to be ballistic when carriers travel from the source to the drain regions without encountering a scattering event. This may be possible if the feature size of the device becomes smaller than the carrier mean free path [10]. If the carrier transport is purely ballistic in the channel, modeling the device behavior reduces to the description of the carrier transmission over and through the source-to-drain potential barrier [11]. The amplitude and the width of the channel barrier are modulated by the front gate, the back gate and drain voltages. As explained in [11] and shown in figure 1, carriers having energy higher than the maximum of the barrier are transmitted from source to drain by thermionic emission, while carrier with lower energy can traverse the channel only by quantum-mechanical tunneling through the source-to-drain barrier.

3. Drain current modeling

3.1. Potential profile in the subthreshold regime

The model proposed here is developed for ultra-thin Silicon film IDG MOSFETs working in the subthreshold regime. Figure 1 shows the schematic n-channel IDG MOSFET considered in this work.

For Peer Review Only

Carrier transport in the ultra-thin silicon film (thickness t_{Si}) is considered 1-D in the x-direction and the resulting current is controlled by both the front and back gate-to-source (V_{G1} and V_{G2}) and drain-to-source (V_D) voltages which impact the shape as well as the amplitude of the source-to-drain energy barrier. In the subthreshold regime, minority carriers can be neglected and Poisson's equation is analytically solved in the x-direction with explicit boundary conditions at the two oxide/silicon interfaces taking into account the electrostatic influence of V_{G1} and V_{G2}. We define the electrostatic potential ψ as the band bending with respect to the intrinsic Fermi level in the silicon film and choosing the Fermi level in the source reservoir as the potential reference. The expression of $\psi(x)$ is obtained by applying the Gauss's law to the particular closed dashed surface shown in figure 1 [12]:

$$-E(x)\frac{t_{Si}}{2}+E(x+dx)\frac{t_{Si}}{2}-E_{S1}(x)+E_{S2}(x)=-\frac{qN_A t_{Si}dx}{2\varepsilon_{Si}} \quad (1)$$

where N_A is the channel doping, E_{S1} and E_{S2} are the electric fields at the front interface and at the back interfaces, respectively. E_{S1} and E_{S2} are given by:

$$E_{S1}=\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V_{G1}-V_{FB1}-\psi}{t_{ox}} \quad (2)$$

$$E_{S2}=-\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V_{G2}-V_{FB2}-\psi_b}{t_{ox}} \quad (3)$$

where ψ and ψ_b, are the surface potentials at the front and back oxide/film interfaces, respectively. Due to the 1D character of the electrostatic potential ψ in the Silicon film the electric field E(x) can be approximated as $E(x)\approx-\frac{d\psi(x)}{dx}$ [13]. Using the development presented in [14] and after some algebraic manipulations, we obtained the following differential equation for the electrostatic potential in the Silicon film:

$$\frac{d^2\Psi}{dx^2}-\frac{2C_{ox}}{\varepsilon_{Si}t_{Si}}\Psi=\frac{1}{\varepsilon_{Si}t_{Si}}\left[qN_A t_{Si}-2C_{ox}(V_{G1}-V_{FB1}-\phi_F)-2C_{ox}(V_{G2}-V_{FB2}-\phi_F)\right] \quad (4)$$

For Peer Review Only

where V_{FB1} and V_{FB2} are the flat-band voltages at the front and the back gate interfaces, respectively, ϕ_F is the bulk potential of the Silicon film, and $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate capacitance per unit area. The analytical solution of equation (4) can be then expressed under the form:

$$\psi(x) = C_1 \exp(\alpha x) + C_2 \exp(-\alpha x) - \frac{R}{\alpha^2} \tag{5}$$

where the coefficients C_1 and C_2 are given by:

$$C_1 = \frac{\phi_S[1-\exp(-\alpha L)] + V_D + R\dfrac{1-\exp(-\alpha L)}{\alpha^2}}{2\sinh(\alpha L)} \tag{6}$$

$$C_2 = -\frac{\phi_S[1-\exp(\alpha L)] + V_D + R\dfrac{1-\exp(\alpha L)}{\alpha^2}}{2\sinh(\alpha L)} \tag{7}$$

with:

$$R = \frac{1}{\varepsilon_{Si} t_{Si}}\left(qN_A t_{Si} - 2C_{ox}(V_{G1} - V_{FB1})\frac{\gamma t_{ox} + t_{Si}}{2\gamma t_{ox} + t_{Si}} - 2C_{ox}(V_{G2} - V_{FB2})\frac{\gamma t_{ox}}{2\gamma t_{ox} + t_{Si}}\right) \tag{8}$$

$$\alpha = \sqrt{\frac{2C_{ox}}{\varepsilon_{Si} t_{Si}}} \tag{9}$$

$$\phi_S = \frac{kT}{q}\ln\left(\frac{N_A N_{SD}}{n_i^2}\right) \tag{10}$$

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{11}$$

where N_{SD} is the doping level in the source and drain regions.

3.2. Quantum confinement effects

Quantum-mechanical (QM) confinement of inversion-layer carriers are well-known to significantly affects the threshold voltage and gate capacitance of highly scaled bulk and DG MOSFETs. The aggressive scaling-down of MOSFETs in the deep submicrometer domain requires ultrathin oxides and

For Peer Review Only

high channel doping levels for minimizing the drastic increase of short channel effects. The direct consequence is a strong increase of the electric field at the Si/SiO_2 interface, which creates a sufficiently steep potential well for inducing the quantization of carrier energy. In bulk-Si and partially depleted (PD) SOI (n)MOSFETs, the confinement is in the potential well defined by the gate-oxide barrier (which is virtually infinite) and the Silicon conduction (or valence) band. Carriers are then confined in a vertical direction in a quantum well (formed by the Silicon conduction band bending at the interface and the oxide/Silicon conduction band-offset) having feature size close to the electron wavelength. This gives rise to a splitting of the energy levels into subbands (two-dimensional (2-D) density-of-states) [15-16], such that the lowest of the allowed energy levels for electrons (resp. for holes) in the well does not coincide with the bottom of the conduction band (resp. the top of the valence band). In addition, the total density-of-states in a 2-D system is less than that in a three-dimensional (3-D) (or classical) system, especially for low energies. Carriers occupying the lowest energy levels behave like quantized carriers while those lying at higher energies, which are not as tightly confined in the potential well, can behave like classical (3-D) particles with three degrees of freedom. As the surface electric field increases, the system becomes more quantized as more and more carriers become confined in the potential well. The quantum-mechanical confinement considerably modifies the carrier distribution in the channel: the maximum of the inversion charge is shifted away from the interface into the Silicon film.

In thin-film IDG MOSFETs, the potential well is defined by both the front and back gates [17]. In these devices carriers are confined due to two main phenomena (figure 2): (a) strong electric field at the interface leading to electric field-induced quantum confinement (EC-QM) and (b) t_{Si}-induced structural quantum confinement (SC-QM) due to the narrow potential well defined by thin Silicon film. Since carriers in thin-film IDG MOSFETs are subjected to structural confinement, in addition to the electric field-induced quantum confinement, quantum-mechanical effects on the threshold voltage and drain current are quite important [18], [19].

For Peer Review Only

If the Silicon film in the IDG MOSFETs is thinner than 15 nm [19], quantum confinement cannot be ignored, and Poisson's equation should be solved self-consistently with Schrödinger's equation. In this case, an analytical solution is not possible without making assumptions of either the shape of the potential distribution or of the electron distribution [20]. When an IDG MOSFET is considered to work in the weak inversion regime (and the free-carrier term in the Poisson's equation can be neglected), the quantum energy levels can be calculated using the expressions developed in [20] using a variational approach. Considering the limit case of an ultra-thin Silicon film, we can assume only one energy subband for the vertical confinement of carriers, given by [20]:

$$E_q \cong \left(\frac{\hbar^2}{2m_\ell}\right)\times\left[\left(\frac{\pi}{t_{Si}}\right)^2 + A_\ell{}^2\times\left(3-\frac{4}{3}\frac{1}{1+(A_\ell t_{Si}/\pi)^2}\right)\right] \tag{12}$$

$$A_\ell \cong \left(\frac{3}{4}\times\frac{2m_\ell qE_x}{\hbar^2}\right)^{1/3} \tag{13}$$

where m_ℓ is the electron longitudinal effective mass (vertical confinement) and E_x is the (spatially constant) transverse electric field in the ultra-thin body silicon film, dependent on the front- and back-gate voltage differences [20]:

$$E_x = -\frac{(V_{FB1}-V_{FB2})-(V_{G1}-V_{G2})}{t_{Si}+2\frac{\varepsilon_{Si}}{\varepsilon_{ox}}t_{ox}} \tag{14}$$

The first energy subband profile $E_1(x)$ can be easily derived as:

$$E_1(x) = q(\phi_S - \psi(x)) + E_q \tag{15}$$

3.3. Ballistic current modeling in the ballistic subthreshold regime

Once $E_1(x)$ is known as a function of V_{G1}, V_{G2} and V_D, the total ballistic current (per device width unit) can be evaluated as follows:

$$I_{DS} = I_{Therm} + I_{Tun} \tag{16}$$

For Peer Review Only

where I_{Term} and I_{Tun} are the thermionic and the tunneling components of the ballistic current respectively. For a two-dimensional gas of electrons [21], I_{therm} and I_{tun} are given by:

$$I_{Therm} = \frac{2q}{\pi^2 \hbar} \int_{-\infty}^{+\infty} dk_z \times \int_{E_{1,max}}^{+\infty} \left[f(E, E_{FS}) - f(E, E_{FD}) \right] dE_x \tag{17}$$

$$I_{Tun} = \frac{2q}{\pi^2 \hbar} \int_{-\infty}^{+\infty} dk_z \times \int_{0}^{E_{1,max}} \left[f(E, E_{FS}) - f(E, E_{FD}) \right] T(E_x)\, dE_x \tag{18}$$

where $f(E_F,E_{FS})$ is the Fermi–Dirac distribution function, E_{FS} and E_{FD} are the Fermi-level in the source and drain reservoirs respectively ($E_{FD} = E_{FS} - qV_{DS}$), k_z is the electron wave vector component in the z direction, the factor 2 accounts for the two Silicon valleys characterized by m_ℓ in the confinement direction (y-direction) and $T(E_x)$ is the barrier transparency for electrons and E is the total energy of carriers in source and drain reservoirs given by:

$$E = E_1 + E_x + \frac{\hbar^2 k_z^2}{2m_t} \tag{19}$$

where E_1 is the energy level of the first subband (given by equation (15)), E_x is the carrier energy in the direction of the current, m_t is the electron transverse effective mass. In equations (17) and (18), $E_{1,max}$ is the maximum of the source-to-drain energy barrier given by:

$$E_{1,max} = E_1(x_{max}) \tag{20}$$

where x_{max} is obtained from equation (4) with the condition:

$$\frac{d\psi(x)}{dx} = 0 \quad \text{for} \quad x = x_{max} \tag{21}$$

$$x_{max} = \frac{1}{2\alpha} \ln\left(\frac{C_2}{C_1}\right) \tag{22}$$

In equation (18), the barrier transparency is calculated using the WKB approximation:

For Peer Review Only

$$T(E_x) = \exp\left(-2\int_{x_1}^{x_2}\sqrt{\frac{2m_t(E_1(x)-E_x)}{\hbar^2}}dx\right) \qquad (23)$$
$$T_{WKB}(E_x > E_{1,max}) = 1$$

where x_1 and x_2 are the coordinates of the turning points (figure 1). x_1 and x_2 have literal expressions due to the analytical character of the barrier:

$$x_{1,2}(E_x) = \frac{1}{\alpha}\ln\left[\frac{A \pm \sqrt{\Delta}}{2C_1}\right] \qquad (24)$$

where the quantities A and Δ are defined as follows:

$$A = \phi_S + \frac{R}{\alpha^2} + \frac{E_q}{q} - \frac{E_x}{q} \qquad (25)$$

$$\Delta = A^2 - 4C_1C_2 \qquad (26)$$

The WKB approximation has the main advantage to be CPU inexpensive and reasonably accurate for channel lengths down to a few nanometers. Moreover, it has been shown in [22] that differences between results obtained considering the WKB approximation and full quantum treatment (tight-binding scheme) are surprisingly small (typically a few percents), which confers to the WKB approach a reasonable accuracy in the frame of the present analysis. The proposed model applies to (100) silicon inversion layers, but it can it be extended to different crystal orientations or channel materials.

4. Results and model validation

Figure 3 shows the first energy subband profile in the Si film calculated with the model in a L=10 nm intrinsic channel IDG MOSFET (t_{Si}=2 nm, t_{ox}=0.6 nm). In order to test the validity of the model, we compare these profiles with those obtained with a self-consistent Poisson-Schrödinger solver based on a real-space Non-Equilibrium Green's Function (NEGF) approach (DGGREEN2D [23]).

As shown in figure 3 a good agreement is obtained between the two barriers in the subthreshold regime. In particular, we note an excellent agreement for the positions of the maximum as well as the

For Peer Review Only

amplitude of the barrier between the analytical and numerical curves. The slight difference in the barrier width is due to the electric field penetration in the source and drain regions, only taken into account in the numerical approach.

The subthreshold $I_D(V_{G1})$ characteristics calculated with the analytical model for IDG MOSFET with L=10 nm and different back gate voltages are shown in figure 4. Drain current characteristics for DG MOSFETs are also shown in this figure. Figure 5 compares analytical model and numerical data for IDG MOSFET with different channel lengths. These figures show that in the subthreshold regime the analytical model very well fits numerical data obtained with DGGREEN2D for devices in the deca-nanometer range.

5. Discussion: impact of the source-to-drain tunneling current

Quantum-mechanical tunneling was often neglected in several previous works, which mainly focused on the modeling of thermionic emission or scattering [24-25]. However, below 8 nm the width of the channel barrier decreases significantly (figure 6), increasing the impact of the quantum tunneling on the device characteristics. We have analyzed the impact of carrier tunneling on device performances through a detailed comparison between model predictions with and without quantum-mechanical tunneling. Two cases are considered: (1) thermionic emission for $E_x > E_{max}$ and $T(E_x) = 0$ for $E_x < E_{max}$; (2) thermionic emission for $E_x > E_{max}$ and quantum tunneling with $T(E_x)$ given by the WKB approximation (equation 23). Figure 7 shows subthreshold $I_D(V_{G1})$ drain current characteristics calculated with the analytical model for channel lengths from 5 nm to 15 nm. Two series of curves have been plotted, considering or not the WKB tunneling contribution in the ballistic current. These results highlight the dramatic impact of the source-to-drain tunneling current on the subthreshold slope and also on the off-state current. In such a subthreshold regime, the carrier transmission by thermionic emission is reduced or even suppressed due to the high channel barrier. As a consequence, when the channel length decreases the tunneling becomes dominant and constitutes the main physical

For Peer Review Only

phenomenon limiting the devices scaling, typically below channel lengths of ~ 8 nm. Quantum-mechanical tunneling significantly degrades the off-state current especially in short channels, where the off-state current increase by more than two decades (L_g=5 nm). However, the off-state current should be slightly reduced for the shorter geometries since it is calculated assuming perfectly ballistic transport and thus ignoring the partial reflection of electron wave functions on the source barrier. The subthreshold swing also increases (with about 30% for L_g=8 nm with respect to L=15 nm) due to quantum-mechanical tunneling. As previously indicated for the off-state current, these results can be considered as an upper limit, since we assume perfectly ballistic transport without wave function reflection at the source barrier.

6. Conclusion

An analytical model for the subthreshold drain current in ultra-thin IDG MOSFETs working in the ballistic regime is presented. The model is particularly well-adapted for ultra-short IDG transistors in the decananometer scale since it accounts for the main physical phenomena related to these ultimate devices: 2-D short channel effects, quantum vertical confinement as well as carrier transmission by both thermionic emission and quantum tunneling through the source-to-drain barrier. The model is used to predict the variation with the channel length of essential subthreshold parameters, such as the off-state current and the subthreshold slope.

ACKNOWLEDGMENTS

This work was supported by the French Ministry of Research (ANR PNANO project “MULTIGRILLES”).

For Peer Review Only

REFERENCES

[1]. M. Bescond, *et al.* Atomic-scale modeling of Double-Gate MOSFETs using a tight-binding Green's function formalism. *Solid State Electron.*, **48**, 567 (2004).

[2]. M. Masahara, *et al.* Demonstration, Analysis, and Device Design Considerations for Independent DG MOSFETs. *IEEE Trans. Electron Devices*, **52**, 2046 (2005).

[3]. L. Mathew, *et al.* CMOS vertical Multiple Independent Gate Field Effect Transistor (MIGFET). *Proc. IEEE Int. SOI Conference*, 187 (2004).

[4]. W. Zhang, *et al.* Physical Insights Regarding Design and Performance of Independent-Gate FinFETs. *IEEE Trans. Electron Devices*, **52**, 2198 (2005).

[5]. G. Pei and E.C. Kan. Independently Driven DG MOSFETs for Mixed-Signal Circuits: Part I—Quasi-Static and Nonquasi-Static Channel Coupling. *IEEE Trans. Electron Devices*, **51**, 2086 (2004).

[6]. G. Pei, *et al*. A Physical Compact Model of DG MOSFET for Mixed-Signal Circuit Applications—Part I: Model Description. *IEEE Trans. Electron Devices*, **50**, 2135 (2003).

[7]. D. Munteanu, *et al*. Quantum Short-Channel Compact Modeling of Drain-Current in Double-Gate MOSFET. *Solid State Electron.*, **50**, 630 (2006).

[8]. B. Iñiguez, *et al.* Compact-Modeling Solutions For Nanoscale Double-Gate and Gate-All-Around MOSFETs. *IEEE Trans. Electron Devices*, **53**, 2128 (2006).

[9]. S. Martinie, *et al.* Impact of ballistic and quasi-ballistic transport on performances of Double-Gate MOSFET-based circuits. *IEEE Trans. Electron Devices*, **55**, 2443 (2008).

[10]. M. Lundstrom. *Fundamentals of Carrier Transport*, 2nd ed., Cambridge University Press, 2000.

[11]. D. Munteanu, J.L. Autran. Two-dimensional Modeling of Quantum Ballistic Transport in Ultimate Double-Gate SOI Devices, *Solid State Electron.*, **47**, 1219 (2003).

For Peer Review Only

[12]. D. Munteanu, *et al*. Compact Modeling of Symmetrical Double-Gate MOSFETs Including Carrier Confinement and Short-Channel Effects. *Molecular Simulation*, **33**, 605 (2007).

[13]. D. Munteanu, *et al*. Compact Model of the Quantum Short-Channel Threshold Voltage in Symmetric Double-Gate MOSFET. Molecular Simulation, **31**, 831 (2005).

[14]. D. Munteanu, *et al*. Compact modeling of drain current in Independently Driven Double-Gate MOSFETs. *Proc. International NSTI Nanotech Conference – Workshop on Compact Modeling*, 574 (2007).

[15]. Y. Taur, T H. Ning. *Fundamentals of Modern VLSI Devices*, Cambridge, UK: Cambridge Univ. Press, 1998.

[16]. S. A. Hareland, *et al.* A Physically-Based Model for Quantization Effects in Hole Inversion Layers, *IEEE Trans. Electron Devices*, **45**, 179 (1998).

[17]. T. Ernst, *et al.* Investigation of SOI MOSFETs with Ultimate Thickness. *Microelectronic Engineering*, **48**, 339 (1999).

[18]. V. Trivedi, J. G. Fossum. Quantum-Mechanical Effects on the Threshold Voltage of Undoped Double-Gate MOSFETs. *IEEE Electron Dev. Lett.*, **26**, 579 (2005).

[19]. M. Moreau, *et al.* Simulation Analysis of Quantum Confinement and Short-Channel Effects in Independent Double-Gate Metal-Oxide-Semiconductor Field-Effect Transistors. *Japanese Journal of Applied Physics*, **47**, 7013 (2008).

[20]. L. Ge, J. G. Fossum. Analytical modeling of quantization and volume inversion in thin Si-film DG MOSFETs. *IEEE Trans. Electron Devices*, **49**, 287 (2002).

[21]. D.K. Ferry, S.M. Goodnick. *Tranport in Nanostructures*, Cambridge University Press, Cambridge (1997).

[22]. M. Städele. Influence of source-drain tunneling on the subthreshold behavior of sub-10nm double-gate MOSFETs. *Proc. European Solid-State Device Research Conference (ESSDERC)*, 135 (2002).

For Peer Review Only

[23]. J.L. Autran, D. Munteanu. Simulation of electron transport in nanoscale independent-gate double-gate devices using a full 2D Green's function approach. *Journal of Computational and Theoretical Nanoscience*, **5**, 1120 (2008).

[24]. K. Natori. Ballistic metal-oxide-semiconductor field effect transistor. *J. Appl. Phys.*, **76**, 4879 (1994).

[25]. M. S. Lundstrom. Elementary scattering theory of the Si MOSFET. *IEEE Electron Dev. Lett.*, **18**, 361 (1997).

For Peer Review Only

FIGURE CAPTIONS

Figure 1. Schematic ultra-thin IDG MOSFET and its technological and electrical parameters considered in this work. The first energy subband profile $E_1(x)$ obtained from equation (11) is also represented (dotted line).

Figure 2. Energy-band diagrams in a vertical cross-section in the Silicon film of IDG n-channel MOSFETs showing two possible cases of carrier confinement: (a) electric field-induced quantum confinement (EC-QM) and (b) t_{Si}-induced structural confinement (SC-QM) due to the narrow potential well defined by the thin Silicon film. $E^{i}_{\ell,t}$ are the energy levels of the potential well (ℓ corresponds to the longitudinal effective mass, $m_\ell=0.98\times m_0$, and t corresponds to the transversal effective mass, $m_t=0.19\times m_0$).

Figure 3. First energy subband profiles $E_1(x)$ in the Silicon film calculated with the analytical model (equation (13)) and with the 2D numerical code DGGREEN2D [23]. Device parameters are: L=10 nm, t_{Si}=2 nm and t_{ox}=0.6 nm.

Figure 4. Subthreshold $I_D(V_{G1})$ characteristics calculated with the analytical model (lines). Values obtained with the 2D numerical code DGGREEN2D [23] are also reported for comparison (symbols). Device parameters are the same as in figure 3.

Figure 5. $I_D(V_{G1})$ characteristics of IDG MOSFET calculated with the analytical model. Values obtained with the 2-D numerical code DGGREEN2D [23] are also reported for comparison. Device parameters are: t_{Si}=2 nm and t_{ox}=0.6 nm.

For Peer Review Only

Figure 6. Variation of the source to drain energy barrier in the channel when decreasing the channel length (V_{G1}=V_{G2}=0 V, V_D=0.8 V). Device parameters are the same as in figure 5.

Figure 7. Subthreshold $I_D(V_{G1})$ characteristics calculated with the analytical model when considering or not the WKB tunneling component in the ballistic current. Device parameters are the same as in figure 5.

For Peer Review Only

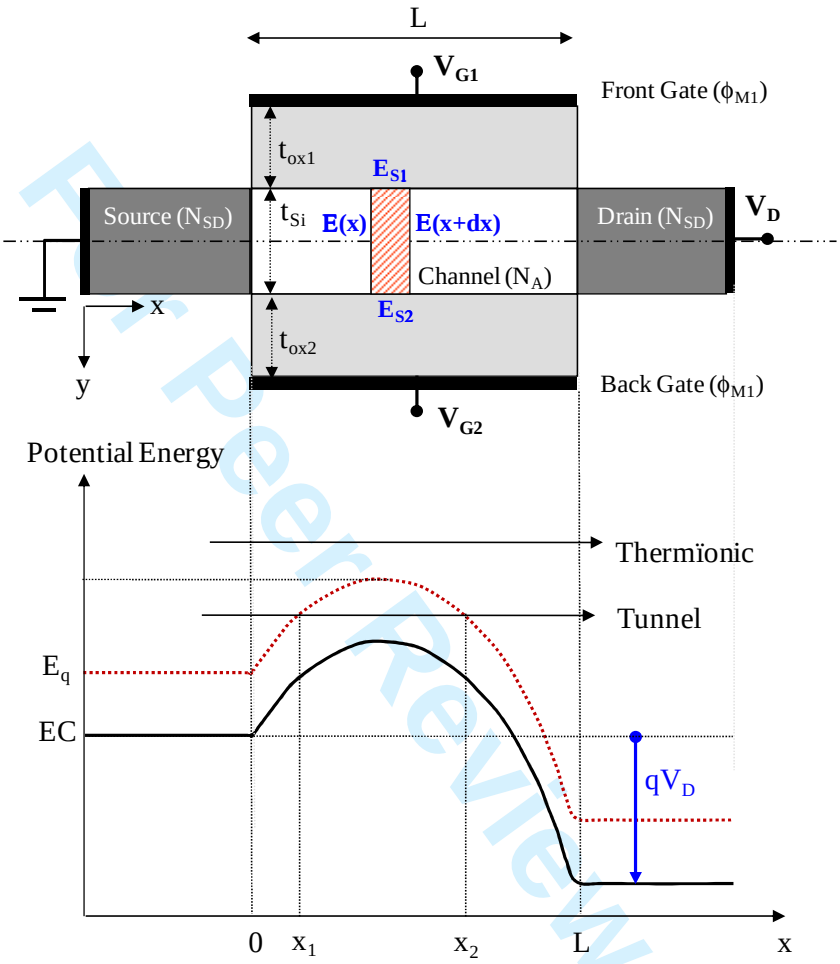

Figure 1.

Munteanu et al.

For Peer Review Only

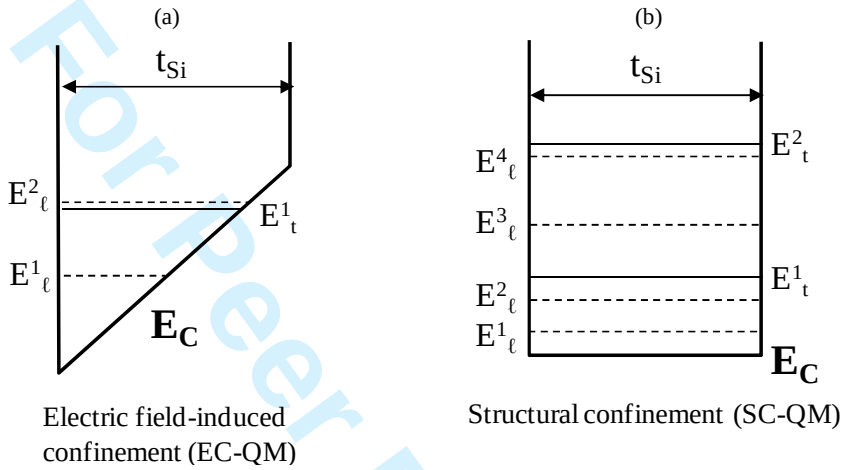

Figure 2.

Munteanu et al.

For Peer Review Only

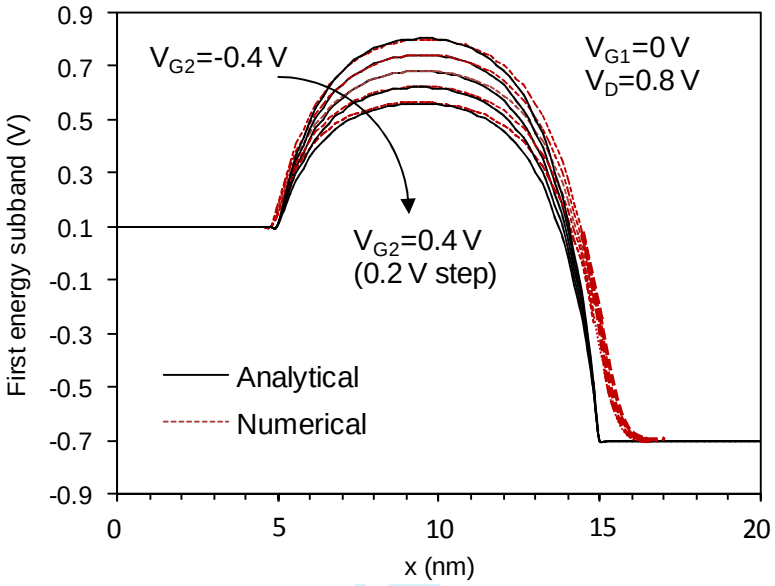

Figure 3.

Munteanu et al.

Review Only

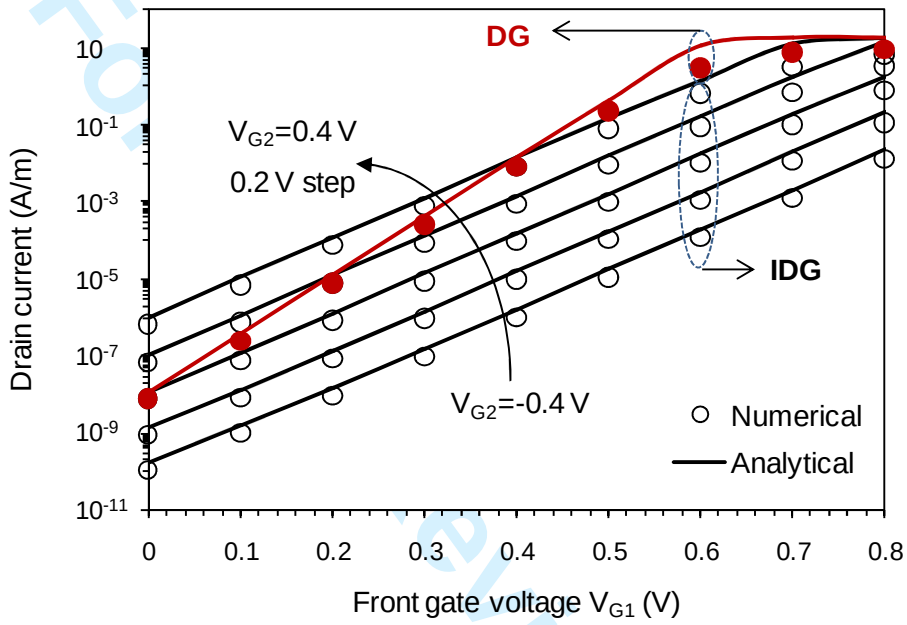

Figure 4.

Munteanu et al.

For Review Only

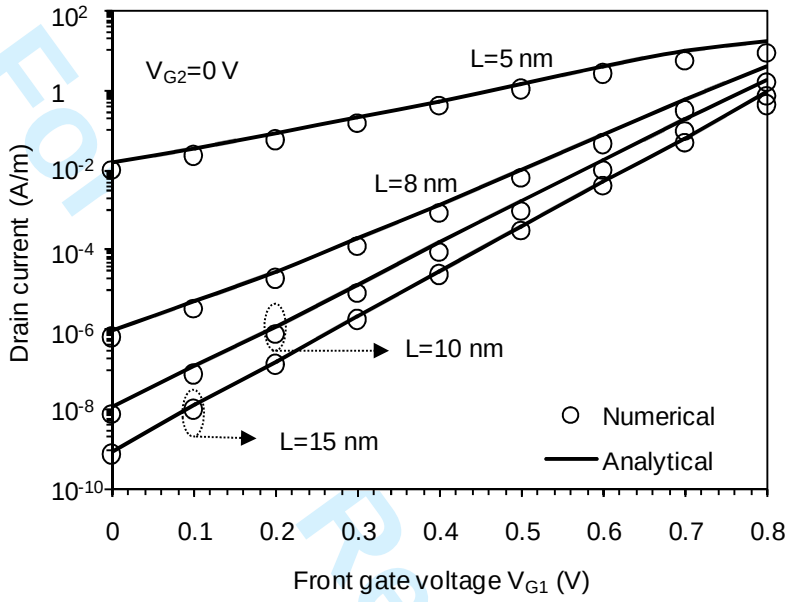

Figure 5.

Munteanu et al.

For Review Only

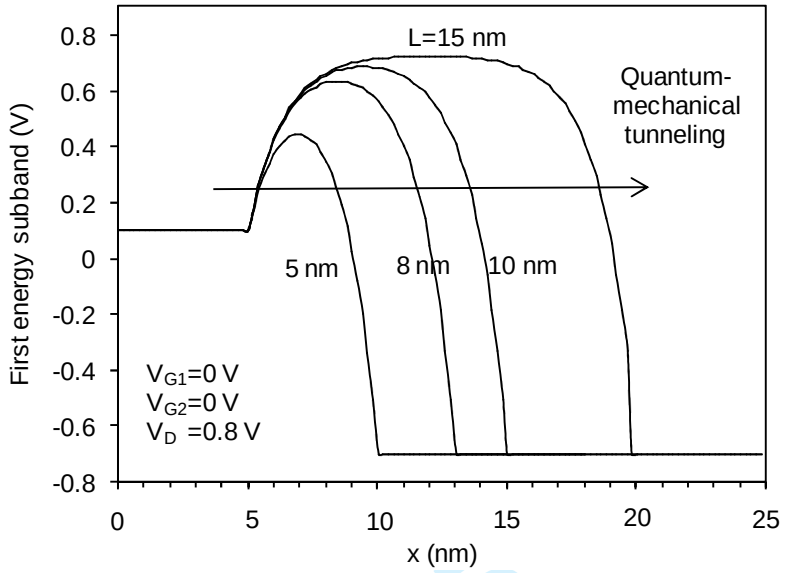

Figure 6.

Munteanu et al.

For Review Only

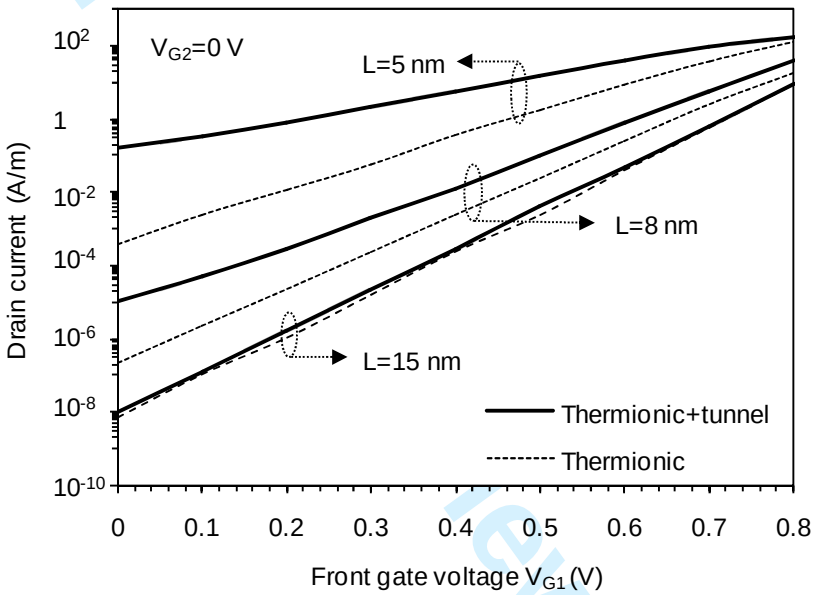

Figure 7.

Munteanu et al.

For Review Only