# Thermal shot noise in top-gated single carbon nanotube field effect transistors

Julien Chaste, Emiliano Pallecchi, Pascal Morfin, Gwendal Fève, Takis Kontos, Jean-Marc Berroir, Perti Hakonen, Bernard Plaçais

# Thermal shot noise in top-gated single carbon nanotube field effect transistors

J. Chaste,[1] E. Pallecchi,[1] P. Morfin,[1] G. Fève,[1] T. Kontos,[1] J.-M. Berroir,[1] P. Hakonen,[2] and B. Plaçais[1,*]

[1] *Laboratoire Pierre Aigrain, ENS-CNRS-UMR8551, 24 rue Lhomond, 75005 Paris, France*

[2] *Low Temperature Laboratory, Aalto University, Puumiehenkuja 2 B, FI-00076 Aalto, Finland*

(Dated: May 13, 2010)

## Abstract

The high-frequency transconductance and current noise of top-gated single carbon nanotube transistors have been measured and used to investigate hot electron effects in one-dimensional transistors. Results are in good agreement with a theory of 1-dimensional nano-transistor. In particular the prediction of a large transconductance correction to the Johnson-Nyquist thermal noise formula is confirmed experimentally. Experiment shows that nanotube transistors can be used as fast charge detectors for quantum coherent electronics with a resolution of $13\mu e/\sqrt{\text{Hz}}$ in the 0.2–0.8 GHz band.

PACS numbers: 73.63.Fg, 72.10.Di, 73.22.f

*Electronic address: Bernard.Placais@lpa.ens.fr

Field effect transistors (FETs), such as quantum point contact transistors [1], are an alternative to Coulomb blockade devices (SETs)[2] for fast single charge detection in nanostructures due to their smaller impedance. In the perspective of a future quantum electronics based on ballistic electrons [3], or the fast readout of charge qubits, a nanosecond time resolution is needed that is challenging but should be reachable by using nano-transistors. A well-known realization is a top gated single carbon nanotube [4], which works at high frequency [5] (see review in [6]). Ultimate gate coupling and finite density of states in the channel push these nano-transistors close to the quantum limit where gate capacitance $C_g$ approaches the quantum capacitance $C_q$ [5]. Beside large charge sensitivity, an important limiting factor of resolution is thermal noise from hot electrons which is prominent in low-dimensional conductors due to poor energy relaxation [7, 8]. Effect of dissipation can be investigated by measuring the out-of-equilibrium phonon population at finite bias $V_d$ [9] but also by noise thermometry [10]. The nano-transistor geometry offers an opportunity to revisit these hot electron effects using the additional control of electronic transmission.

The noise thermometry approach of electronic population relies on assumption of a thermal distribution and the Johnson-Nyquist formula $S_I = 4g_n k_B T_e$ relates the current noise spectral density $S_I$ to the electronic temperature $T_e$ via a so-called "noise conductance" $g_n$ [11]. In general one has $g_n = g_d$, the differential drain conductance. The situation is different in gated semiconductors where an additional contribution arises, at finite bias, associated with transconductance $g_m = \partial I_d/\partial V_g$ where $I_d$ is the drain current and $V_g$ the gate voltage. This term depends *a priori* on geometry, at least for the 3D and 2D transistors [11, 12]. We show here that the situation is different at 1D and that a simple relation exists between $g_d$, $g_m$ and $g_n$ which only brings in the gate coupling factor $\beta = C_g/C_q$.

The paper reports on current noise and transconductance of top-gated single nanotube transistors. Measurements were carried at 4K to take advantage of the enhanced noise resolution of cryogenic setups and in a GHz bandwidth to overcome the $1/f^\alpha$ low frequency noise and benefit from the good AC coupling in the contact impedance. Hot electron effects show up both in the thermal current noise and the width of the transconductance peak at the onset of conduction. Using a 1D nano-transistor model based on scattering theory [13] we obtain a generalized Johnson-Nyquist noise formula in the form,

$$S_I = 4\,(g_d + g_m/2\beta)\,k_B T_e\,, \tag{1}$$

where conductance terms and noise are to be taken at the same frequency. Eq.(1) is supported by the RF measurements of transconductance and noise and the electronic temperature reported below as function of bias voltage. As electronic temperature depends on current, one can alternatively express thermal noise as $S_I = 2eI_d\tilde{F}$, by introducing a pseudo Fano factor $\tilde{F} \lesssim 1$. The limit $\tilde{F} = 1$ corresponds to a classical shot noise as observed in vacuum diodes. The hot electron regime shows up in our nanotube transistor by a full thermal shot noise with $\tilde{F} \sim 1$ at low bias followed by some reduction ($\tilde{F} \simeq 0.7$) resulting from Pauli principle and the effect of electronic degeneracy which generally shows up at high bias.

The sample (Fig.1(a)) is taken from a batch which was extensively described and characterized in Ref.[5]. A symmetric double gate RF design is used (Fig.1(a)) on high resistivity silicon substrate. The high mobility CVD-grown nanotube (diameter $d \sim 2$ nm) is equipped with a top gate (length $L_g = 0.3\mu$m) deposited on a thin $AlO_x$ oxide (thickness $t_{ox} \simeq 6$ nm). Palladium drain and source metallisations are used for low Schottky barrier contacts. Our high-sensitivity cryogenic setup includes a low noise amplifier fitted to a 200–50 Ohms impedance matching transformer with a 0.8 GHz cutoff. Matched resistors are fitted at the input and output lines to obtain a broad 0.1–0.8 GHz measuring band. The 200 Ohms output load ensures DC voltage bias conditions and serves as an auxiliary white noise source for in-situ calibration. The lumped circuit element description of the nanotube transistor (Fig.1(b)) is used for RF data analysis and the theoretical model below. The gate capacitance, $C_g/L_g \simeq 0.07 \pm 0.02$ fF/$\mu$m, is taken from the room temperature RF probe station measurements [5]. With $C_q/L_g = 8e^2/hv_F = 0.4$ fF/$\mu$m ($v_F \simeq 8 \times 10^5$ m/s) we deduce $\beta \simeq 0.2$ [5]. We have used negative drain bias, which shows lower $1/f^\alpha$ noise and symmetric gate bias conditions. $I_d$ and $S_I$ are taken by reference to the pinch-off value (at $V_g = +1$ V).

Figure 2 shows the radio frequency transconductance $g_m^{RF}$ deduced from transmission measurements [5] as function of gate voltage for different bias conditions. The DC conductance $g_d^{DC}$ and transconductance $g_m^{DC}$ are obtained from the $I_d(V_g, V_d)$ characteristics (Fig.2-inset). Reflection coefficients, and $g_d^{RF}$, cannot be accessed with this setup. The sample shows large $g_m^{RF} \simeq 30$ $\mu$S, typically 3-times larger than $g_m^{DC}$, which suggests AC contact coupling. We observe a small temperature dependence of $g_m^{RF}$ (a $\sim 50\%$ decrease between 4K and 300K) which we take as a first indication of a hot electron regime.

In Fig.3 we discuss measurements of the transistor in the open state ($V_g = -0.5$ V) where $g_m^{RF} \simeq 0$. Here the nanotube behaves as a metallic wire with a finite transmission $D \sim 0.1$,

deduced from low bias current and presumably limited by contact barriers. As seen in the figure, a full shot noise limit is observed for $|V_d| \lesssim 0.4$ V, followed by a saturation plateau. Although the noise characterization is certainly relevant for understanding the saturation mechanism that takes place in nanotubes at very high bias, we prefer to leave this discussion for a future work. Using $S_I = 2eI_d\tilde{F} \gtrsim 4g_d^{DC}k_BT_e$ ($g_m \simeq 0$ and $g_d \gtrsim g_d^{DC}$ in Eq.(1)) we deduce $\tilde{F} \gtrsim 2k_BT_e/eV_d$ and an (over-) estimate of electronic temperature $k_BT_e/eV_d \lesssim \tilde{F}/2 \simeq 0.6$. Indeed, this ratio is larger than a theoretical expectation, $k_BT_e/eV_d \sim \sqrt{6D/\pi^2} \sim 0.25$, for a Wiedemann-Franz resistance limited thermal sink [14]. Importantly, both numbers show that a hot electron regime is expected and present in the nanotube. As discussed below, we can rely on the transconductance characteristics for an independent determination of the electronic temperature of the nanotube working as a transistor.

Fig.4 contains the main experimental results of the paper, namely the bias dependence of $I_d$, $S_I$ and $g_m$, at the transconductance maximum ($V_g = +0.5$ V). The $S_I(V_d)$ dependence is similar to that observed in the open state with, as a difference, a first noise plateau ($\tilde{F} \simeq 0.7$) observed in range $|V_d| = 0.1$–$0.3$ V. The two step increase of noise and the width of the plateau ($\sim 0.3$ V) are suggestive of the subband structure of the nanotube (intersubband-gap $\sim 0.3$–$0.5$ eV for a 2 nm diameter). In order to secure 1D transport conditions, we shall therefore focus below to the ($|V_d| \lesssim 0.3$ V) bias range.

For the theoretical analysis we rely on a simple 1D nano-transistor model. The nanotube is described as a fourfold degenerate 1D channel decomposed in three sections (see Fig.1(c)): a central part covered by the top-gate which acts as a local classical barrier and two ungated nanotube leads on both sides which constitute the drain and source reservoirs of the transistor. The leads are diffusive and assumed to be populated with Fermi distributions $f_s(E)$ and $f_d(E) = f_s(E + eV_d)$. The barrier (height $\Phi$) acts as an high-pass energy filter with quasi-ballistic high energy electrons (transmission $D(E) \lesssim 1$ for $E > \Phi$) and reflected low energy ones ($D(E) = 0$ for $E < \Phi$). With these assumptions and scattering theory [13] one can readily calculate current and noise to deduce the differential conductance $g_d = \frac{4e^2}{h} f_d(\Phi)$, the transconductance

$$g_m = \beta \frac{4e^2}{h}[f_s(\Phi) - f_d(\Phi)] \qquad , \tag{2}$$

and the noise conductance $g_n = \frac{2e^2}{h}[f_s(\Phi) + f_d(\Phi)]$. According to the equivalent circuit in Fig.1(b), we have taken $\partial\Phi/\partial V_g = -e\beta$. These three "conductances" depend on two parameters, the drain and source occupation numbers (at $E = \Phi$), and therefore obey the

constitutive relation $g_n = g_d + g_m/2\beta$ which gives rise to Eq.(1). Details of screening, which are encoded in the $\Phi(V_d, V_g)$ functional, or temperature $T_e(V_d, V_g)$ in $f_{s,d}(\Phi)$, are implicit in Eq.(1) which can be regarded as a universal result for 1D transistors. In terms of thermal shot-noise one has $\tilde{F} = \coth(eV_d/2k_BT_e) \lesssim 1.3$ (for $2k_BT_e/eV_d \lesssim 1$) at low bias where $g_m < 2\beta g_d$. At high bias one has $g_m \gg 2\beta g_d$ whenever $f_d(\Phi) \ll f_s(\Phi) \lesssim 1$; one also expect Pauli noise suppression with a reduction factor $(1 - f_s(\Phi))$ like in the usual 2D case [12].

As a first test of the model we obtain a good fit of the $g_m^{RF}(V_g)$ data in Fig.2 with Eq.(2) by taking $\Phi(V_g) = Const. - e\beta V_g$ and $E_F \ll \Phi$ in $f_{s,d}(\Phi)$ according to the equivalent circuit and the potential landscape in Figs.1(b) and (c). We have used a scaling factor 0.6 that accounts for residual electronic diffusion above the barrier. Electronic temperatures deduced from theoretical fits corresponds to a large absolute temperature ($k_BT_e \simeq 28$ meV at $V_d \sim 200$ mV), but still a small energy spread when compared to the bias voltage ($k_BT_e \simeq 0.14\, eV_d$) .

The model accounts qualitatively for a full shot-noise at low bias ($\tilde{F} \simeq 1$ for $V_d \lesssim 0.1$ V) and for the noise reduction at intermediate bias ($|V_d| = 0.1$–$0.3$ V). Using the electronic temperature from transconductance fits in Fig.2, we can *quantitatively* compare noise and transconductance in Eq.(1): At $V_d = -0.2$ V, where $S_I/2e \simeq 1.46 \pm 0.1$ $\mu$A, $g_m^{RF} \simeq 8.6 \pm 0.5$ $\mu$S and $V_{Te} = k_BT_e/e\beta \simeq 0.14 \pm 0.02$ V we obtain $g_m^{RF}V_{Te} \simeq 1.2 \pm 0.3$ $\mu$A in good agreement with theoretical prediction $S_I/2e \gtrsim g_mV_{Te}$ from Eq.(1). By comparison standard noise thermometry would give a smaller value $S_I/2e = 2g_dk_BT_e/e \simeq 0.5$ $\mu$A (taking $g_d = g_d^{DC} \simeq 9$ $\mu$S). We take this agreement as a strong support for the 1D model. Further experimental investigations should involve direct measurement of $g_d^{RF}$ to test Eq.(1) over the full bias range including the crossover $g_m^{RF} \lesssim 2\beta g_d^{RF}$.

Finally we can use our data to estimate the charge resolution $\delta q_{rms} = \sqrt{S_I}C_g/g_m$. The best signal to noise conditions, for $V_d \sim 0.3$ V and $I_dV_d \sim 1$ $\mu$W where $g_m \gtrsim 15$ $\mu$S and $S_I/2e \lesssim 2$ $\mu$A, give $\delta q_{rms} \lesssim 13\mu e/\sqrt{\text{Hz}}$ ($C_g \lesssim 40$ aF [5]) for our double gate device which corresponds to an *rms* charge resolution of 0.4 electron in the 0.8 GHz bandwidth of our set-up. Within a factor five of the best resolution achieved in SETs [2], this smaller sensitivity of the present CNT-FETs is balanced by a much larger bandwidth (0.8 GHz here against 0.08 GHz in [2]) and the possibility to operate at room temperature.

In conclusion, our comprehensive study of high-frequency transport and shot noise has confirmed that the single nanotube transistor is a model system and that hot electron

effects are prominent at 1D. In particular our data support a generalized Johnson-Nyquist expression for thermal noise in 1D transistors introduced in the paper. Finally we have benchmarked nanotube FETs against nanotube SETs for applications as fast single electron detectors.

**Acknowledgments**

Authors acknowledge fruitful discussions with G. Dambrine, V. Derycke, P. Dollfus, C. Glattli, H. Happy and M. Sanquer. The research has been supported by french ANR under contracts ANR-2005-055-HF-CNT, ANR-05-NANO-010-01-NL-SBPC, and EU-STREP project CARDEQ under contract IST-FP6-011285.

---

[1] S. Gustavsson, R. Leturcq, T. Ihn, M. Studer, K. Ensslin, D.C. Driscoll, and A.C. Gossard, *Nano Lett.* **8**, 2547 (2006).

[2] S. E. S. Andresen, F. Wu, R. Danneau, D. Gunnarsson and P. J. Hakonen, *J. Appl. Phys* **104**, 033715 (2008).

[3] G. Fève, A. Mahé, B. Plaçais, J.-M. Berroir, T. Kontos, A. Cavanna, Y. Jin, B. Etienne and D. C. Glattli *Science* **316**, 1169 (2007).

[4] S.J. Tans, A.R.M. Verschueren, and C. Dekker, *Nature* **393**, 49 (1998)

[5] J. Chaste, L. Lechner, P. Morfin, G. Fève, T. Kontos, J.-M. Berroir, D. C. Glattli, H. Happy, P. Hakonen, B. Plaçais, *Nano Lett.* **8**, 525 (2008)

[6] C. Rutherghen, D. Jain P. Burke, *Nature Nanotech.*. **4**, 911 (2009).

[7] H. Pothier, S. Gueron, N.O. Birge, D. Esteve, M.H. Devoret, *Phys. Rev. Lett.* **779**, 3490 (1997).

[8] M. Lazzeri, F. Mauri, *Phys. Rev. B* **73**, 165419 (2006).

[9] M. Steiner, M. Freitag, V. Perebeinos, J. C. Tsang, J. P. Small, M. Kinoshita, D. Yuan, J. Liu, P. Avouris, *Nature Nanotech.* **4** , 320 (2009).

[10] F. Wu, T. Tsuneta, R. Tarkiainen, D. Gunnarsson, T.H. Wang, and P.J. Hakonen , *Phys. Rev. B* **75**, 125419 (2007).

[11] A. van der Ziel, Proc. IRE **50**, 1808 (1962).

[12] Y. Naveh, A.N. Korotkov, and K.K. Likharev, *Phys. Rev. B* **60**, 2169 (1999).

[13] Y.M. Blanter, M. Büttiker, *Phys. Rep.* **336**, 1 (2000)

[14] A. Kumar, L. Saminadayar, D. C. Glattli, Y. Jin and B. Etienne, *Phys. Rev. Lett.* **76**, 2778 (1996).

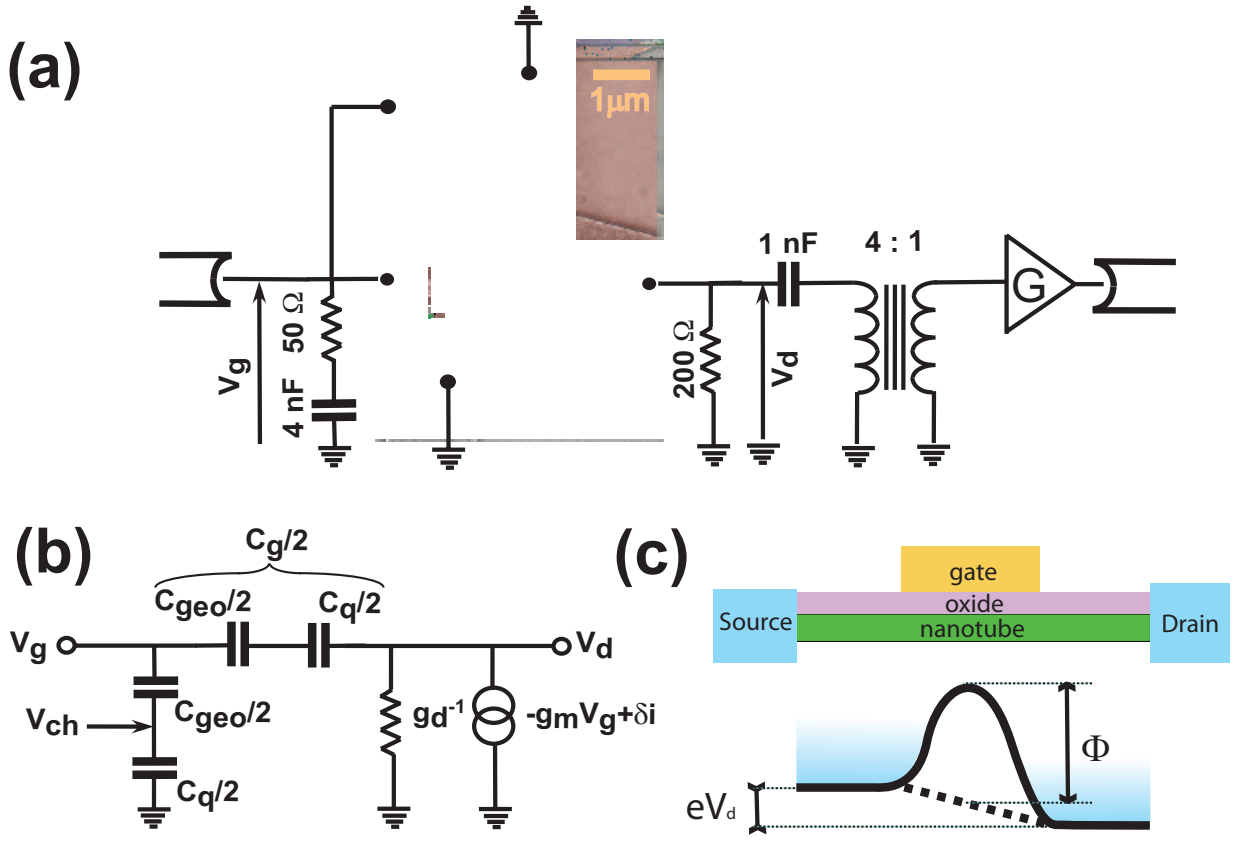


FIG. 1: (a) A double gate nanotube transistor embedded in the (4K) measuring scheme which includes bias resistors, DC blocks and a cryogenic low noise amplifier with a 200 : 50 Ohms matching transformer. The nanotube (colored in green), of diameter $\sim$ 2 nm, is covered in its middle part by a top gate (length 300 nm) which controls the local barrier. The leads on both sides act as electronic reservoirs. (b) The lumped element description of the nanotube transistor RF response includes the channel resistance $g_d^{-1}$, the transconductance $g_m$, the gate capacitance $C_g = C_{geo}C_q/(C_{geo} + C_q)$ with its geometrical (resp. quantum) contributions $C_{geo}$ (resp. $C_q$) and the noise current generator $\delta i$. The channel potential $V_{ch} = V_g \times C_g/C_q$ governs the barrier height $\Phi = -e(V_{ch} + Const.)$ which defines the gate coupling coefficient $\beta = \partial\Phi/\partial V_g = C_g/C_q$. (c) Sketch of the energy profile (solid line) and the electronic distribution (blue gray scale) of a top-gated nanotube transistor.

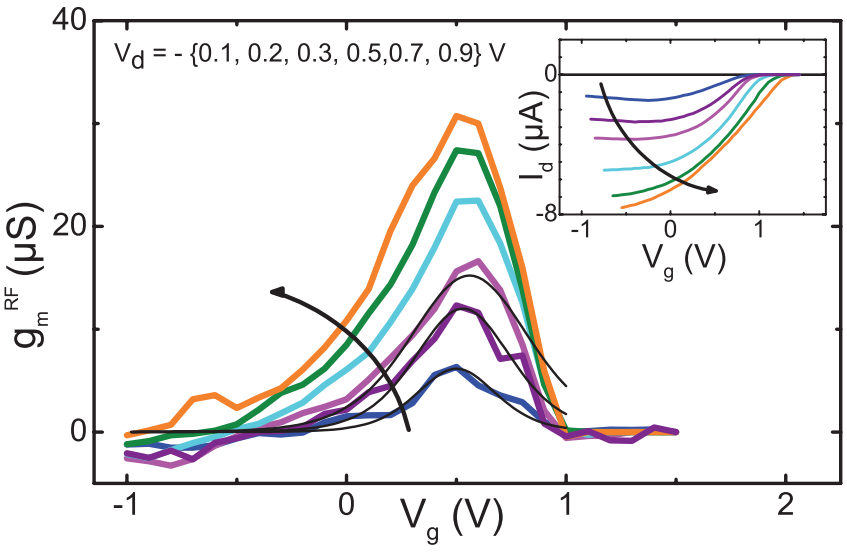


FIG. 2: Carbon nanotube transistor characteristics including the DC current (inset) and the RF transconductance $g_m^{RF}$ measured in the $0-0.8$ GHz band (main panel) as function of gate voltage $V_g$ for a representative set of (color encoded) bias voltages increasing according to the arrow. The transconductance maximum for $V_g \simeq +0.5$ V saturates at a large value $\gtrsim 30$ $\mu$S. Low bias data, for $V_d = -(100, 200, 300)$ mV, are fitted with Eq.(2) (solid lines) within a prefactor $\simeq 0.6$ added to account for non ideal ballistic transport above the barrier. The fitting parameter, $V_{Te} = k_B T_e/e\beta \simeq (120, 140, 170) \pm 0.01$ mV, gives (with $\beta = 0.2$) the thermal energies $k_B T_e = (24, 28, 34)$ meV.

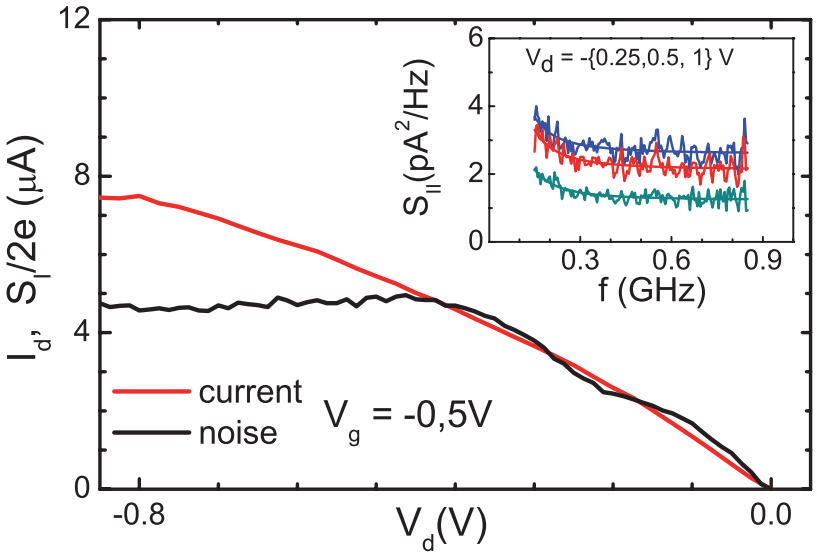


FIG. 3: Bias dependence of the DC current and current noise of the nanotube transistor in the metallic state ($V_g \leq 0$). The intrinsic nanotube shot noise $S_I$ is deduced by fitting the raw noise spectra (inset) with a $A + B/f^2$ law (solid lines) and subtracting a $(B/f^2)$ Lorenzian tail for the environment noise which contributes below 0.5 GHz and the white noise ($S_I/V_d \simeq 1.1$ (pA)$^2$V$^{-1}$) of the 200 Ohm bias resistance, which is independently measured at the pinch-off. Accurate shot noise data, in the 0.1–0.8 GHz band, are plotted in the main panel as function of bias voltage for comparison with DC current. We observe full shot-noise ($S_I/2e \simeq I_d$) for $V_d > -0.4$ V and a noise saturation for $V_d < -0.4$ V.

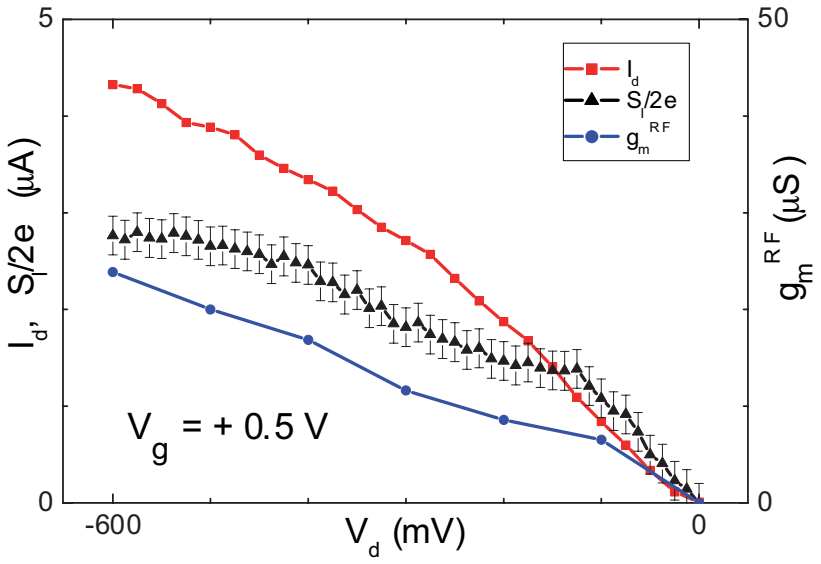


FIG. 4: Bias dependence of DC current $I_d$ (squares), RF current noise $S_I$ (triangles) and RF transconductance $g_m$ (circles) at the transconductance maximum ($V_g \sim +0.5$ V).