



HAL
open science

Silicon Nanophotonics Fabrication: an Innovative Graduate Course

Lukas Chrostowski, Nicolas Clément, Jean-Paul Rouger, Dan Deptuck,
Nicolas Jaeger

► **To cite this version:**

Lukas Chrostowski, Nicolas Clément, Jean-Paul Rouger, Dan Deptuck, Nicolas Jaeger. Silicon Nanophotonics Fabrication: an Innovative Graduate Course. The 17th International Conference on Telecommunications, Apr 2010, Doha, Qatar. hal-00476550

HAL Id: hal-00476550

<https://hal.science/hal-00476550>

Submitted on 26 Apr 2010

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Silicon Nanophotonics Fabrication: an Innovative Graduate Course

(Invited Paper)

Lukas Chrostowski^{*}, Nicolas Rouger[†], Dan Deptuck[‡] and Nicolas A. F. Jaeger^{*}

^{*}Electrical and Computer Engineering, University of British Columbia

Vancouver, British Columbia, V6R 1T3, Canada

Email: lukasc@ece.ubc.ca, <http://www.mina.ubc.ca/lukasc>

[†]Centre National de la Recherche Scientifique, Grenoble Electrical Engineering Lab, Grenoble University, France

[‡]CMC Microsystems, Kingston, Ontario, Canada

Abstract—We report our recent successful experiences related to the development of a transcontinental course in silicon photonics offered by the University of British Columbia in collaboration with CMC Microsystems. The course is offered to students from across Canada and has attracted participants from nearly every Canadian university with an advanced photonics research program.

The focus of the course is the rapidly developing field of silicon photonics. Its aim is to provide the students with a breadth of competencies in designing optical circuits and systems using a silicon-on-insulator platform. The students taking the course gain familiarity in design, fabrication, and testing in an area of photonics that is destined to play an increasingly important, and in the long run ubiquitous, role in optical circuitry, impacting on areas such as optical interconnects, communications systems, and sensor systems.

The course is structured using a blended-learning pedagogical approach consisting of an on-site workshop followed by design-based e-learning. The students' designs are fabricated using IMEC's passive photonic cSOI process, which is accessed through the European silicon photonics prototyping service ePIXfab. Student projects to date have included the design of integrated-optical circuits using combinations of ring resonators, waveguides, couplers, and photonic crystals for applications such as filters for WDM optical interconnects, demodulators for phase modulated signals, and lab-on-chip sensors.

I. INTRODUCTION

Motivated by a lack of formal educational opportunities in the area of nanophotonics design, in 2008 we set out to create an innovative graduate-level course that provides students from across Canada with an opportunity to have an integrated-optic circuit fabricated through a foundry service. These are designed using photonic nano-wires and/or photonic crystals. The resulting "Silicon Nanophotonics Fabrication" course is a partnership between the University of British Columbia (UBC) and CMC Microsystems (CMC). This partnership, together with nation-wide student participation, offers an enhanced student learning experience based on a cost-effective model. While the course was originally offered as an advanced graduate level course, it has been attended by select undergraduate students, Masters and PhD level graduate students, postdoctoral fellows, and people from industry.

The course objective is to train students how to design, test, and critically evaluate an integrated-optic or photonic

integrated circuit. This is accomplished by providing fifty hours of instruction and hands-on modelling tutorials in the form of a concentrated seven-day workshop at UBC, during which the students are presented with a program consisting of a blend of theory, design practice, and design and layout tool competency development. The students return to their home institution for a two month long circuit design and layout cycle. During this time, sophisticated software tools are provided by CMC and the students interact with the instructors using several internet-based methods including bi-weekly internet-hosted meetings and review sessions. This course provides the students with access to IMEC's passive photonic crystalline silicon-on-insulator (cSOI) process (accessed through the European silicon photonics prototyping service ePIXfab) [1]. During the workshop at UBC, students are familiarized with existing test and measurement stations so that they can build their own experimental setup and test their devices at their home institutions. We support the students in project selection, design, layout, and testing, with the entire cycle completed over a period just shy of one year.

The silicon-on-insulator (SOI) fabrication technology was chosen since it is a promising candidate for the future goal of integrating optics with electronics on a common silicon platform [2]–[4]. Using IMEC's passive photonic cSOI process it is possible to fabricate photonic crystals, waveguides (photonic crystal, strip, or ridge), gratings for fibre coupling, multiplexers (diffraction or arrayed waveguide), ring resonators/filters, and many other components. While nanophotonic technology has historically been developed in-house at universities, students in the program can save valuable research time by having their designs fabricated through the ePIXfab service on a multi-project wafer (MPW) shuttle run at IMEC, Europe's largest independent research centre in nanoelectronics and nanotechnology. This makes it possible to design, have fabricated, and test a high-quality device in less than one year. As discussed in this paper, providing students with an opportunity to design an integrated-optic circuit or system is a useful pedagogical tool in that it promotes active student engagement in the learning process.

II. PEDAGOGICAL STRATEGY

A. Learning Outcomes

The desired learning outcomes for a student attending the course are two-fold:

- 1) That the student be able to design integrated-optic circuits or systems that are robust to the variability inherent in any fabrication process, and
- 2) that the student develop an understanding of the complexities involved in a complete design cycle of an integrated-optic circuit, where the design cycle is composed of the software design, layout, fabrication by a third party, and testing and critical evaluation.

In order to achieve these outcomes we take the students through a complete design cycle, with the following learning objectives:

- (a) model a nanophotonic circuit or system, both analytically and numerically;
- (b) design a nanophotonic circuit or system, including necessary test structures, that is robust under expected variations in the fabrication process;
- (c) create a mask layout of a nanophotonic circuit that obeys constraints imposed by the fabrication process (i.e., design rules);
- (d) experimentally test and characterize the fabricated device;
- (e) compare theory with experiments and identify sources of error and discrepancy;
- (f) write a critical report on the nanophotonic circuit / process.

B. Learner-Centred Approach with a Focus on Design

This section describes the team's approaches towards providing an effective environment for the student's learning. The most important point is found in the learning objectives – "(b) design a nanophotonic circuit or system". Since we focus on the student's ability to design, we force the student to operate chiefly at the highest levels in Bloom's cognitive taxonomy [5]; the bulk of the student's work is in synthesizing the information with the specific goal of designing a circuit.

By requiring the student to design a device, where the success of the design will be validated by experiment, the onus is on the student to ensure the validity of the models and calculations. This encourages the student to question all assumptions in the models and determine their applicability to the problem. Thereby, the student's motivation to learn the material is dramatically enhanced since the stakes are much higher (i.e., the student knows that their device will not function if they do not learn the material or if they accept the theory without understanding its limitations). In order to produce a successful design, the student must also learn about process limitations and issues surrounding manufacturability in a real-world, industrial-class, foundry process.

This course is inspired by several student-centred instructional strategies to increase the effectiveness of student learning. We choose the content complexity to be student-appropriate and by using the "blended learning" method [6].

Our programme goes through a progression of increasing cognitive level of complexity starting with content for novices and aiming to develop experts in the field. Instructional strategies appropriate to the students' competencies are chosen. First, we begin by providing a knowledge and an understanding of fundamental photonics concepts. The students then apply this knowledge to perform numerical and analytic calculations and analyze photonic components. The bulk of the students' work during the course is in synthesizing the information provided by designing an integrated-optic circuit. Finally, the students evaluate their device performance. This allows them to assess the accuracy of their understanding and limitations in the technology for possible future iterations in their design. Hands-on education also complements their cognitive learning, specifically, by utilizing computer aided design, i.e., modelling, device mask layout, and verification or design rule checking and in building and using an experimental setup for device characterization/testing.

In the early stages of learning during the workshop, we first introduce the concepts in traditional face-to-face lectures. During the lectures, we employ a "worked-example" approach [7]. This is a useful instructional strategy for introducing the methodology necessary for solving complex problems [8], in our case the design of a photonic circuit. For instance, students are given example calculations for determining the optical coupling coefficient between two waveguides. The formalism employed can subsequently be adapted by the student in designing a device geometry for a required coupling coefficient. By following the worked-example approach, we avoid the pitfalls of having an excessive cognitive load caused by jumping to the problem solving and design stage too quickly [9]. Once students have understood the concepts, we transition towards active learning.

We emphasize active learning via the problem-based learning (PBL) approach [10]. This approach was originally developed for training medical students [11] has since been successfully used in other disciplines including electrical engineering [12]. Learning is based on a challenging and open-ended problem, and the instructors take on the role of facilitators. During our workshop tutorials, the class is given a series of problems, which they solve in small teams. Solutions to each problem are presented by the students, discussed immediately, and questions are answered before proceeding to subsequent problems.

There is an increasing emphasis placed on design in engineering curricula. In undergraduate education it is particularly important to gradually introduce design skills spanning the range from structured and guided design to open-ended project design [13]. In our programme, we similarly teach design skills, initially with short exercises with clear specifications and with known solutions and finally by providing the students the opportunity to define their own design specifications for their open-ended project.

Since the goal of this course is to train students in design, and, once the students have achieved the necessary level of proficiency in the subject, we augment the problem-based

learning approach by emphasizing the design aspect – termed design-based learning (DBL) [14]. This approach is used for the design portion of the course, which in our case spans several months. Students are asked to brainstorm potential project ideas, briefly explain them to their peers to receive early feedback, and then proceed to develop a project proposal. Via an on-line discussion forum, the instructors, as well as peers, provide feedback at several stages throughout the students’ design processes.

One of the main innovations in this course is in providing the students with access to a mature nano-phonic fabrication technology. This allows them to design and test a device of particular interest to them. We believe that training in design, fabrication, and experimentation is an important component of graduate education. As an example, a formal graduate course on micro-electro-mechanical systems (MEMS) fabrication and testing is offered at ETH Zurich [15]. However, due to time constraints, this particular course does not offer any design component, but rather has a strong fabrication element. In contrast, our course is mainly focused on the design and testing, with the fabrication performed elsewhere. This avoids the fabrication process-related challenges and ensures that the course can be completed in a reasonable length of time.

In many courses computer software is seen to enrich teaching strategies in that it provides a hands-on component which gives immediate feedback and results in increased student motivation [16]. The motivation for using software is even stronger, in our case, since it is a vital component of the design-cycle. Additionally, the use of modelling software contributes positively to the learning environment as it is used extensively during the workshop to help students grasp the concepts being taught.

C. Blended Learning

One of the principal constraints in this course is that students are enrolled from across the country. This limits the potential face-to-face interaction time and has led us to adopt a blended learning (BL) model [6], [17]. Blended learning, sometimes referred as a “hybrid course”, includes a combination of face-to-face learning (with the instructors and with peers), independent learning, and e-learning (live or self-paced on-line learning). The blended learning environment is considered by many to be the most efficient teaching approach [18]. In our case, we start with a face-to-face workshop and use a remote design-based e-learning approach for the rest of the course.

Collaborative learning is beneficial in the blended approach [19] as it promotes knowledge building, sharing, and distribution. Group collaborative learning is encouraged in several ways in this course. During the workshop students work in small teams to solve the tutorial problems, they discuss their project ideas with peers working on similar topics, and they build camaraderie through group activities such as lunches, dinners, and sight-seeing trips. During the rest of the course, students participate in web video conferences with the instructors and communicate with each other and the instructors via an on-line discussion forum. In the forum, which is moderated

by the instructors, the students are encouraged to answer one another’s questions and to share their learning experiences and discoveries. Students post, discuss, and obtain solutions to various problems encountered in their designs. Many problems encountered are common to several students working on similar topics, which further promotes the collaborative model employed.

This course features a substantial component of remote learning, specifically, during the design and test stages. For the test portion, one may consider offering a remote laboratory service, as has been implemented for other remote-learning engineering courses (e.g., [20], [21]). However, while the priority in our course is for students to obtain experimental data in order to validate their designs, we believe that a significant portion of the design aspect of the course is the design of the experiments themselves. While we provide guidelines and a list of suggested equipment for the typical two-port experiment, the student has the opportunity to learn how to assemble an optical setup (at their home institution, at UBC, or at CMC) and master the skills of optical alignment. This lesson provides a valuable experience in understanding the challenges encountered during such experiments. Furthermore, while a well-structured remote-learning laboratory may be suitable for undergraduate courses in optical communications [20], our graduate design course requires much more experimental flexibility; specifically, students have a range of experimental requirements, such as embedding microfluidics, performing mechanical actuation, studying thermal properties, and providing an environmental (gas) stimulus, each of which will need access to specialized equipment.

III. IMPLEMENTATION AND COURSE DETAILS

A. Schedule

The course is scheduled with an eye toward one major constraint, IMEC’s fabrication schedule [22]. Specifically, the deadline for the mask submission is in November. Additionally, since the typical academic calendar year begins in September, the students are more likely to be available for travel during the summer months. Also, by holding the workshop portion of the course in the summer, July or August, the students have sufficient time to work on and complete their designs. The course schedule is shown in Table I. The students have a break of several months while IMEC fabricates the devices. The fabricated chips are provided to the students in March. The last few months are allocated for device testing, model comparison, and report writing.

TABLE I
COURSE SCHEDULE

Date	Activity
July or August	1 $\frac{1}{2}$ week full-time workshop: lectures and tutorials Design and modelling
September-October	
Sept 10th	Deadline – Design proposal
October 1st	Deadline – Model and design results
October 15th	Deadline – Chip layout (draft, submission to CMC)
November 10th	Deadline – Chip layout (final, submission to CMC)
December 1st	Deadline – Design report
March 1st	Testing of fabricated chips
June	Deadline - Final Report

B. Assessment Strategies

The assessment is based entirely on the student's design, including modelling, testing, and critical assessment, and is evaluated by several formal course submissions:

- Design proposal, description, and literature review
- Modelling, design, and simulation results
- Mask layout (with details including dimensions and lithography requirements)
- Test results (including experimental setup, measurements, and comparison with model)
- Final report (5-8 page two-column manuscript-style)

In design-based learning, we consider the creative aspect of the design in our assessment [14].

C. Workshop Instructional Topics

The workshop portion of the course consists of lectures, software instruction tutorials, and modelling and design sessions. The lecture topics covered are similar to other courses on photonics design (e.g., the JePPIX Course/Training on Photonic Integration Technology offered by ePIXnet at the Technical University of Eindhoven [23] and the 3-day ePIXfab MPW training course [24]). Lectures are intended to introduce the theory of photonic device design:

- Optical waveguides (E&M review; wave propagation; optical modes; slab, buried-channel, SOI-strip waveguides; material and modal dispersion; losses; effective index method)
- Waveguide couplers (coupled-mode theory; numerical methods)
- Fabry-Perot resonators (quality factor; free-spectral range; finesse; transmission spectrum; extinction ratio; photonic crystal cavities; dispersion)
- Ring resonators (analytic solutions; coupling coefficient; impact of dispersion, temperature, and loss)
- Design considerations (parameter variation methodology; test structures; fibre grating couplers; consideration for experimental constraints)

Guest lectures (by software vendor representatives, e.g., Lumerical Solutions Inc., and other faculty, e.g., UBC Professor of Physics Dr. Jeffrey Young) are used to complement the expertise of the instructors. The instructors emphasize the particularities of silicon nanophotonics such as the high modal dispersion in SOI waveguides and its effect on resonators, ring resonators in particular. The limits of analytic modelling are introduced, which motivate the necessity for numerical modelling. Several numerical methods are presented (2D Finite Difference, 2D/3D Beam Propagation Method, and 2D/3D Finite Difference Time Domain method).

The software tutorial sections introduce the students to the commercial software packages used in this course: RSoft Design Group BeamPROPTM, Lumerical Solutions Inc. FDTD Solutions, and The MathWorksTM MATLAB[®] for numerical modelling; and Design Workshop Technologies dw-2000TM for layout. Additionally, the open source 2D Finite Difference Optical Eigenmode Solver for Dielectric Waveguides [25]

is used. Design, modelling, layout and initial verification are done using the students' own computers, with access to software tools provided through CMC. The software tutorials include numerical modelling examples relevant to the course topics and student designs.

Through the hands-on modelling tutorials, simple problems are addressed such as numerical accuracy in meshed structures and the consequences of various assumptions. As an example, the students are asked to calculate the effective index of an asymmetric slab waveguide using the 2D Finite Difference Eigenmode Solver [25] and, to their surprise, they find that their numerical answers depend on their choice of grid spacing. Several fundamental modelling concepts can be introduced using this example. For instance, a correct mesh definition (where the simulated waveguide thickness is always the same) can guarantee a predictable numerical error (red solid line in Fig. 1). However, when the boundaries of the waveguide are a function of the mesh definition, the error due to the mesh and the numerical method is not well controlled (blue dashed line in Fig. 1). Although these are classical and well known results, the students need to understand the sources and magnitudes of errors in their modelling results. The accuracy in their modelling must be controlled, as for example, a minor error in an effective index can have a major effect on the coupling coefficient in a directional coupler and ultimately on the fabricated circuit's performance.

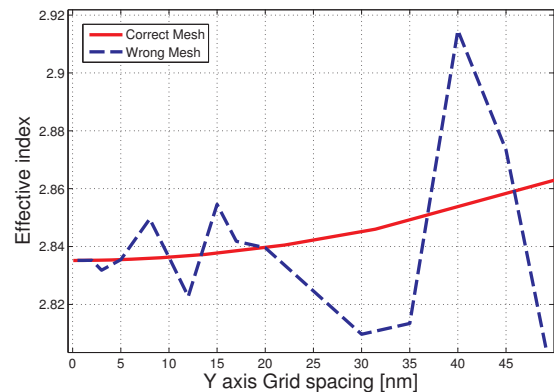


Fig. 1. Effective index of an SOI slab waveguide – impact of the mesh on the numerical accuracy using the Finite Difference method. The top cladding material is air, the core is a 220nm thick silicon waveguide and the bottom cladding material is silicon dioxide.

The students are given instruction on mask layout using the provided Design Workshop Technologies dw-2000TM layout and verification tool. The students lay out an example device and receive feedback from the instructors. In addition, they are trained to use a “technology package” developed by CMC that customizes the functionality of the tool for IMEC’s fabrication technology. The technology package includes some design automation capability (e.g., pcells and macros) as well as a full set of design rules. Having design rule checking (DRC) built directly into the layout tool enables the designer to converge on a DRC-clean layout much more quickly than is possible via a series of iterations between the designer and the foundry. Iterations between the designers (in this case,



Fig. 2. Mask layout for the 2009-10 course, consisting of a full IMEC FXT cell with a total area of $> 12.1 \times 7.4$ mm. Twenty-three (23) student designs were merged on this layout. We used IMEC's "fxt3 FC 630" template taking advantage of their predefined vertical fibre coupler shallow etch mask; hence, the students designed only the deep etch mask (a second chip was provided for those who needed to design both the shallow and deep etch masks). This template contains 3 columns of input/output grating couplers, with a coupler pitch of $25 \mu\text{m}$. Each column is approximately 4 mm wide, and there is a total of 940 input/output pairs on the chip, of which more than 800 have been used by the student designs.

20+ students) and the foundry can be very time consuming, hence it is highly desirable to have error-free designs prior to submission to the foundry. Additionally, students learn how to create a design that is robust under normal variations in the fabrication process, i.e., they produce a physically realizable and manufacturable design that will yield working devices.

On the last day of the workshop, the students brainstorm design ideas, discuss them in a group setting, and obtain feedback from the instructors. Over the next two months, they independently research a specific chosen topic, design their circuit, and lay out the mask that CMC will verify against technology constraints before transferring to IMEC for device fabrication.

D. IMEC Technology

Photonics implemented on SOI substrates has generated significant interest since this technology can be CMOS compatible and offers a wide range of possibilities [2]–[4]. The high refractive index contrast between silicon and silicon dioxide enables one to design waveguides and devices with sub-micron features, greatly miniaturizing photonic integrated circuits [2], [26]. Devices using the SOI/CMOS technology have been fabricated recently with attractive optical functions and good performance including: high quality-factor resonators [27], [28], 80% efficiency vertical grating couplers [29], waveguides with small propagation losses (less than 2.5 dB/cm [4]), and low-loss, small-bend-radius waveguides (radii as small as 2

μm with 0.029 dB loss per 90° turn [4]). Optical cavities on SOI can be implemented as ring or racetrack resonators or as photonic crystal cavities [30]. Several resonator applications have already been demonstrated, mostly for the near infrared wavelength range (around 1550 nm or 1310 nm), such as sensors [31], modulators [32] and multiplexers [33].

The technology chosen for this course is offered by IMEC as a multi-user foundry service based on a CMOS process [1]. The lithography relies on a 193 nm deep-UV lithography which enables features down to $\sim 120 \text{ nm}$ and a minimum pitch of $\sim 300 \text{ nm}$. The designs are fabricated on 200 mm silicon-on-insulator wafers with a 220 nm crystalline top silicon film and a 2000 nm buried oxide. The IMEC foundry offers flexibility in choosing the amount of design surface area, choices in process steps (e.g., 70 nm shallow etch, 220 nm deep etch, etc.), and several process specifications (e.g., exposure dose sweeps and critical dimension parameters). This process yields waveguides with propagation losses of 2.5 dB/cm [4].

In the 2009-10 course, student designs were partitioned onto two chips. On the first chip, the students designed only the deep etch mask making use of one of IMEC's predefined vertical fibre coupler masks for the shallow etch step. On the second chip, the students designed both the deep and shallow etch masks. The former had the advantage of saving the cost of one mask level, and the latter had the advantage of greater design flexibility. For the first chip, twenty designs

were merged on a single layout for a total area of over 12.1 x 7.4 mm, as shown in Figure 2. This chip provided over 800 input/output pairs, affording each student on average twenty four-port devices. The layout was patterned 186 times on a 200 mm wafer. An exposure dose sweep was utilized across the wafer for the deep etch yielding 13 different exposures. Thus, if correctly leveraged, each student could receive multiple copies of 260 unique devices in order to study the effect of parameter variation on the circuit response.

E. Example Student Designs

Students are given the freedom to choose their own topic of interest, for both the application and the design implementation. While the focus of the lectures is on waveguide-based devices, the students have the freedom to design photonic crystal-based devices. Various nanophotonic devices were modelled, designed, and characterized by the students. However, designing a working device within two months is very demanding on the students, as, at every step of their modelling, they must quantify the effects of their assumptions.

Ring resonators are a good example both of the wide spectrum covered by this course and of its strong link to the very exciting applications offered by nanometer size photonic systems (add/drop multiplexers, wavelength division multiplexers, high sensitivity sensors, modulators, etc.). The design of a ring resonator is comprised of several aspects: the optical wave propagation inside the ring (effective index), the coupling region behaviour, and the loss and dispersion mechanisms [34]. These are dependent on the waveguide dimensions, the guided optical mode (wavelength and optical power), and external parameters such as the temperature. This results in a multi-variable system, e.g.,

$$|S_{21}(\lambda, T, W, R, L_{\text{gap}}, L_{\text{Coup}})|^2 = \frac{a^2 + t^2 - 2at \cdot \cos(\delta)}{1 + a^2t^2 - 2at \cdot \cos(\delta)} \quad (1)$$

where $|S_{21}|^2$ is the through-port power, t is the field transmission coefficient of the coupler, a is the round-trip field loss coefficient, δ is the phase shift after a round inside the resonator, all of which depend on λ , T , W , R , L_{gap} and L_{coupler} , which are, respectively, the wavelength, the temperature, the waveguide width, the resonator radius, the gap between the coupled waveguides, and the coupler length. In this example, the students have to go beyond the frontiers of their knowledge to develop a model for their design while considering several effects in their complex 3D devices, namely the high dispersion, the significant effects of temperature, the scattering at the waveguide sidewalls, the waveguide bend effects, and the dielectric perturbation of the straight waveguides in the coupler. Example modelling results are shown in Fig. 3.

In order to accurately characterize their future devices, including the effects of specific phenomena, the students must also design slightly modified versions of their systems. For example, in a racetrack resonator, reducing the coupler length while keeping a same total length of the resonator should provide a same FSR and loss level but different coupling coefficients. This helps the student to further experimentally

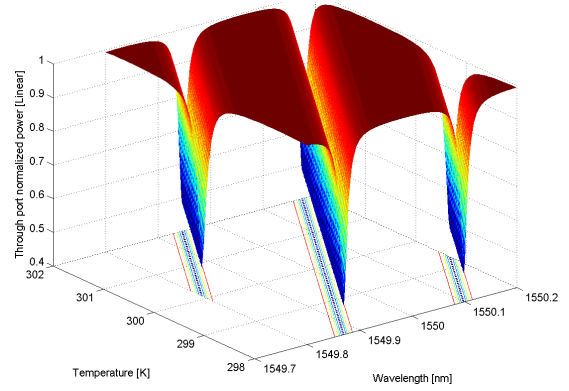


Fig. 3. An example of the design's complexity: a semi-analytic model of the through-port transmission in an SOI racetrack resonator (as in [34]).

investigate the coupling behaviour in sub-micron directional couplers while measuring how the coupling coefficient is modified as a function of the coupler's length. Hence, the student comes to understand that the task is not only to design a particular device based on a set of chosen specifications but also involves designing several variations and test structures. This is necessary to verify the underlying principles of the particular device that the student is trying to create.

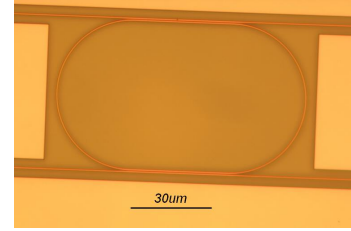


Fig. 4. Microscope photograph of a fabricated add/drop multiplexer implemented with a racetrack resonator.

Following this approach, an example of the result of a student's particular project is a fabricated racetrack resonator designed for a communication system operating at 1550 nm as shown in Fig. 4. The through-port spectrum for a device having a bend radius of 90 μm , a directional coupler length of 15 μm , and a coupler gap of 185 nm is shown in Fig. 5. The measurements give a free spectral range of 0.88 nm, a quality factor of 12903, an extinction ratio of 16.4 dB, an equivalent loss level of 3.13 dB/cm, and a group index of 4.584, which are in close agreement with the values obtained by the student's modelling work. Insertion losses were approximately 17 dB, of which 12 dB of the losses are due to the two grating couplers [35] and the rest likely due to a misaligned or a poorly cleaved optical fibre.

In order to compare their experimental results with their modelling, the students also have access to Scanning Electron Microscopy (SEM) micrographs of their fabricated devices. For example, Fig. 6 provides the width and the gap between the waveguides in the coupler region of the resonator. Fig. 6 also provides the dimensions of holes in a photonic crystal waveguide. This information is used to provide the actual geometry of their device for a comparison between the modelled and the experimental results.

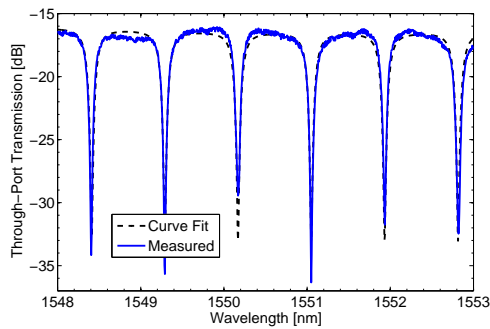


Fig. 5. Comparison of the experimental results to a curve-fit of the analytic through-port transmission spectrum for an SOI racetrack resonator.

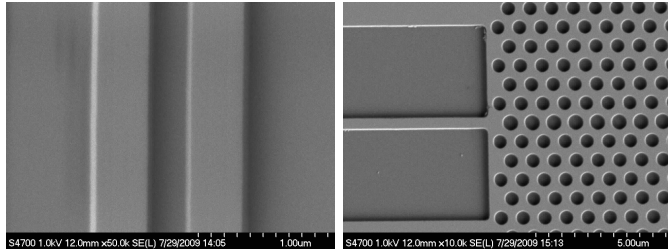


Fig. 6. (left) SEM image of the directional coupler in a racetrack resonator used to determine the fabricated waveguide width and coupler gap. (right) nanowire waveguide end-fire coupled to a photonic crystal waveguide.

One of the specific points of interest in this particular student project was an investigation of the temperature effects in racetrack resonators since these devices can be temperature tuned [36] or be used as temperature sensors. The temperature dependence on the transmission spectrum was investigated experimentally, as shown in Fig. 7. The experiments showed that the resonant wavelength shifts 0.080 nm/K, in agreement with the model (Ref. [34] and Fig. 3) and previous reports [2].

IV. OUTCOMES ASSESSMENT

The success of the course can be measured by the correlation of actual outcomes as compared to the intended outcomes, specifically, by evaluating the success of the student designs. As the 2009-2010 course is still on going (designs created by the students on the two chips are being fabricated at IMEC, which totals 28 distinct designs submitted by 20 students), we can only use the 2008-2009 results at the time of writing. In 2008-2009, 8 students submitted numerous variations on distinct optical circuit/system designs. Of these 75% of the fabricated circuits/systems were functional with reasonable agreement between the computer models and the predicted performance. In the remaining 25%, the devices were functional in the sense that measurements could be made on them, but the students who had designed them were unable to adequately explain the discrepancies between the measurements and the models. As a result of the 2008-2009 fabrication cycle several high quality papers were prepared of which one was submitted to a journal for publication (Ref. [34]) and is now in press.

The feedback obtained from students over the past two years has generally been very positive. Immediately following the 2009 workshop, 100% of the 19 respondents agreed with the statements: a) the course description and registration material

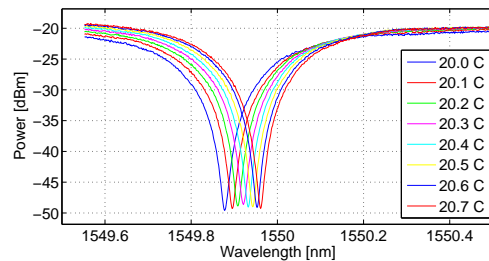


Fig. 7. Measured spectra for a resonator at different substrate temperatures.

accurately reflected the content of the course; b) the reference material and/or audio visuals supported the course content; c) I anticipate using the course materials and/or on-line support for future reference. Furthermore, 89% agreed that the exercises and/or on-line support activities were conducive to learning, 100% of the students were satisfied with the overall quality of this course, and 100% would recommend this course to others. Comments included: “[the course] provided me a jump start with this new technology that would have been very difficult to achieve at [my company] otherwise.”; “The fabrication is reliable: the process is well characterized before the fabrication of our devices. This helps with the modelling.”; “The teamwork was great, both during the modelling and during the characterization.”; “I liked the exercises and tutorials, but... more time was needed. I learn by doing, so the tutorials were the most useful.”; and “[I liked the] openness of discussions, approachable instructors, rhythm is going back and forth from lectures to hands-on tasks.” Students from the first cohort (2008-2009) appreciated being able to receive a fabricated chip only 6 months after starting their design project.

While many students have commented that they learned a great deal from this course, several students felt that the workload was very high and that the period of time allocated for the design component was too short. In response, the course credits were increased from 4 credits to 6 credits (a typical single-semester course at UBC has a weight of 3 credits), and the design time has been increased by holding the instructional workshop prior to the regular start of the academic year.

V. SUMMARY AND CONCLUSION

We have developed an effective strategy for offering an innovative “Silicon Nanophotonics Fabrication” course in which students learn how to model and design a nanophotonic circuit, have it fabricated, and test it, all within one year. The effectiveness of our approach is evident in the following metrics: sophisticated and functional student designs (demonstrating the high level of understanding achieved by the students), publishable results, and positive student feedback. This course provides the necessary foundations and a head start for students who wish to pursue research in this field. Not only does it contribute significantly to training in an important area, we believe that this course opens the door to a wealth of photonics related innovation.

The framework of this course should be applicable to others developing similar courses. Of particular importance

is that the course can be delivered via e-learning to a geographically dispersed audience, particularly, using a blended learning approach. The challenges met and overcome in this course include the logistics of offering a trans-Canadian course taken by students from numerous universities (e.g., visiting student enrolment, travel, accommodations, etc.), the diversity of the students' backgrounds and knowledge of optics and waveguides, and the need for transcontinental communication. An important lesson learned is that sufficient time should be allocated for the students to complete their designs; therefore, in the future we will aim to hold the workshop portion in July so that students have three months to complete their designs. Building on the success from the past two years of this course, the future of this course is promising and the course could be offered to a larger audience.

ACKNOWLEDGMENT

The authors would like to thank: Drs. James Pond, Todd Kleckner, and Sibyl Drissler at Lumerical Solutions Inc. for their guest lecture and for providing access to and supporting the FDTD software; Dr. Jeff F. Young for his guest lecture; IMEC for advice, technical assistance, and educational use of design technologies; RSoft Design Group and Design Workshop Technologies for their flexibility in accommodating course needs; Rasmus Brandt for development of the dw-2000 technology package; to our many colleagues at CMC who made course delivery possible; Raha Vafaei and Nadia Makan for the use of some of their measurement results in our examples; and all of the students who have taken this course for their feedback, participation, and contributions to the course content.

REFERENCES

- [1] [Online]. Available: http://www.epixfab.eu/technology/imec_std/
- [2] L. Pavesi and G. Guillot, *Optical Interconnects: The Silicon Approach*. Springer Berlin / Heidelberg, 2006, no. 978-3-540-28910-4.
- [3] M. L. Calvo and V. Lakshminarayanan, *Optical Waveguides - From theory to Applied Technologies*. CRC Press, 2007, no. 1-57444-698-3.
- [4] W. Bogaerts, P. Dumon, et al., "Compact wavelength-selective functions in silicon-on-insulator photonic wires," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 12, Issue 6, 2006.
- [5] L. Anderson and L. Sosniak, *Bloom's taxonomy: A forty-year retrospective*. NSSE, 1994.
- [6] D. Garrison and H. Kanuka, "Blended learning: Uncovering its transformative potential in higher education," *The internet and higher education*, vol. 7, no. 2, pp. 95–105, 2004.
- [7] R. Clark, F. Nguyen, and J. Sweller, *Efficiency in learning: Evidence-based guidelines to manage cognitive load*. Pfeiffer, 2005.
- [8] J. van Merriënboer, *Training complex cognitive skills: A four-component instructional design model for technical training*. Educational Technology Pubs, 1997.
- [9] J. Sweller, "Cognitive load during problem solving: Effects on learning," *Cognitive Science*, vol. 12, no. 2, pp. 257 – 285, 1988.
- [10] D. Boud and G. Feletti, *The challenge of problem-based learning*. Routledge, 1998.
- [11] H. Schmidt, "Problem-based learning: rationale and description," *Medical Education*, vol. 17, no. 1, pp. 11–16, 1983.
- [12] L. Costa, M. Honkala, and A. Lehtovuori, "Applying the Problem-Based Learning Approach to Teach Elementary Circuit Analysis," *IEEE Transactions on Education*, vol. 50, no. 1, pp. 41–48, 2007.
- [13] H. Rehman, A. Ra'a, and Y. Al-assaf, "An integrated approach for strategic development of engineering curricula: Focus on students' design skills," *IEEE Transactions on Education*, vol. 52, pp. 470–481, 2009.
- [14] Y. Doppelt, "Assessing creative thinking in design-based learning," *International Journal of Technology and Design Education*, vol. 19, no. 1, pp. 55–65, 2009.
- [15] R. Grundbacher, J. Hoetzel, and C. Hierold, "MEMSlab: A Practical MEMS Course for the Fabrication, Packaging, and Testing of a Single-Axis Accelerometer," *IEEE Transactions on Education*, vol. 52, pp. 82–91, 2009.
- [16] J. Castro-Schez, E. Del Castillo, J. Hortolano, and A. Rodriguez, "Designing and Using Software Tools for Educational Purposes: FLAT, a Case Study," *IEEE Transactions on Education*, vol. 52, no. 1, 2009.
- [17] N. Hoic-Bozic, V. Mornar, and I. Boticki, "A Blended Learning Approach to Course Design and Implementation," *IEEE Transactions on Education*, vol. 52, no. 1, pp. 19–30, 2009.
- [18] F. Alonso, G. López, D. Manrique, and J. Viñes, "An instructional model for web-based e-learning education with a blended learning process approach," *British Journal of Educational Technology*, vol. 36, no. 2, pp. 217–235, 2005.
- [19] M. Khine and A. Lourdasamy, "Blended learning approach in teacher education: combining face-to-face instruction, multimedia viewing and online discussion," *British Journal of Educational Technology*, vol. 34, no. 5, pp. 671–675, 2003.
- [20] D. Gurkan, A. Mickelson, and D. Benhaddou, "Remote laboratories for optical circuits," *IEEE Transactions on Education*, vol. 51, no. 1, pp. 53–60, 2008.
- [21] O. Bellmunt, D. Miracle, S. Arellano, A. Sumper, and A. Andreu, "A distance PLC programming course employing a remote laboratory based on a flexible manufacturing cell," *IEEE Transactions on Education*, vol. 49, no. 2, pp. 278–284, 2006.
- [22] [Online]. Available: http://www.epixfab.eu/mpw_shuttles/schedule
- [23] [Online]. Available: <http://www.epixnet.org/index.php?id=348>
- [24] [Online]. Available: http://www.epixfab.eu/epifab/training/mpw_training_contents/
- [25] A. Fallahkhair, K. Li, and T. Murphy, "Vector finite difference mode-solver for anisotropic dielectric waveguides," *Journal of Lightwave Technology*, vol. 26, no. 11, pp. 1423–1431, June 1, 2008.
- [26] W. Bogaerts, R. Baets, P. Dumon, V. Wiaux, S. Beckx, D. Taillaert, B. Luyssaert, J. V. Campenhout, P. Bienstman, and D. V. Thourhout, "Nanophotonic waveguides in silicon-on-insulator fabricated with cmos technology," *Journal of Lightwave Technology*, vol. 23, Issue 1, 2005.
- [27] F. Xia, L. Sekaric, M. O'Boyle, and Y. Vlasov, "Coupled resonator optical waveguides based on silicon-on-insulator photonic wires," *Applied Physics Letters*, vol. 89, no. 4, p. 041122, 2006.
- [28] J. Niehusmann, A. Vörckel, P. H. Bolivar, T. Wahlbrink, W. Henschel, and H. Kurz, "Ultra-high-quality-factor silicon-on-insulator microring resonator," *Optics Letters*, vol. 29, no. 24, pp. 2861–2863, 2004.
- [29] G. Roelkens, D. V. Thourhout, and R. Baets, "High efficiency grating coupler between silicon-on-insulator waveguides and perfectly vertical optical fibers," *Optics Letters*, vol. 32, no. 11, pp. 1495–1497, 2007.
- [30] T. Asano, B. Song, and S. Noda, "Analysis of the experimental Q factors (~ 1 million) of photonic crystal nanocavities," *Appl. Phys. Lett.*, vol. 79, pp. 4289–4291, 2001.
- [31] G. Rostami and A. Rostami, "An ultra high-precision temperature sensor design based on two-port ring resonator," A. Serpenguzel, G. Badenes, and G. C. Righini, Eds., vol. 6593, no. 1. SPIE, 2007, p. 65930W.
- [32] M. Geis, S. Spector, R. Williamson, and T. Lyszczarz, "Submicrosecond submilliwatt silicon-on-insulator thermo-optic switch," *Photonics Technology Letters, IEEE*, vol. 16, no. 11, pp. 2514–2516, Nov. 2004.
- [33] A. Vörckel, M. Münster, W. Henschel, P. H. Bolivar, and H. Kurz, "Asymmetrically coupled silicon-on-insulator microring resonators for compact add-drop multiplexers," *Photonics Technology Letter*, vol. 15, no. 7, pp. 921–923, 2003.
- [34] N. Rouger, L. Chrostowski, and R. Vafaei, "Temperature effects on Silicon-On-Insulator (SOI) racetrack resonators: a coupled analytic and 2D finite difference approach," *Journal of Lightwave Technology*, (in press) 2010.
- [35] D. Taillaert, F. V. Laere, M. Ayre, W. Bogaerts, D. V. Thourhout, P. Bienstman, and R. Baets, "Grating couplers for coupling between optical fibers and nanophotonic waveguides," *Japanese Journal of Applied Physics*, vol. 45, no. 8A, pp. 6071–6077, 2006.
- [36] M. W. Pruessner, T. H. Stievater, M. S. Ferraro, and W. S. Rabinovich, "Thermo-optic tuning and switching in SOI waveguide Fabry-Perot microcavities," *Optics Express*, vol. 15, no. 12, pp. 7557–7563, 2007.