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# UHV Fabrication of the Ytterbium Silicide as Potential Low Schottky Barrier S/D Contact Material for N-Type MOSFET

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Ytterbium silicide provides a low Schottky barrier height to electron on n-type silicon. This property makes this material very attractive for the realization of Source/Drain contacts for n-type MOSFETs. In this communication, the study of structural and electrical properties of YbSi<sub>2-x</sub> fabricated at different temperature in Ultra-High Vacuum condition without any protective layers is presented. N-type SB-MOSFETs with ytterbium silicide based S/D contacts were fabricated at optimal silicidation temperatures on SOI substrate with an ultra thin body.

## Introduction

With continuous MOSFET dimension down scaling, conventional devices, with ohmic contact based source/drain (S/D), are approaching their performance limitations (1). One of the critical parameters making difficult the development of next CMOS generations (<30 nm) is the S/D series resistance. In order to overcome this issue, it was proposed, as alternative way, to replace highly doped ohmic contact S/D by metallic Schottky S/D with a very low Schottky barrier height (SBH) for electrons or holes (2).

The metallic Schottky S/D based on platinum silicide (PtSi) was successfully used for the realization of p-MOS because of its low SBH to holes (0.15 eV) on p-Si (3). For the fabrication of n-type SB MOSFETs, rare earth (RE) silicides present a great interest because they provide the lowest barrier to electrons on n-type silicon. Among the RE metals, ytterbium (Yb) features the lowest work function (2.59 eV) (4). Therefore, Yb silicide (YbSi) is a very promising material to obtain a low Schottky barrier height (SBH)  $\Phi_{Bn}$  that promotes electron injection.

RE silicides are usually formed by *ex situ* rapid thermal annealing (RTA). Because of the extremely high sensitivity of the RE metals to oxygen, it is necessary to use a protective cap layer (5) to limit or suppress any oxidation reaction at the silicide/silicon interface. However, the implementation of an additional cap layer makes the process of devices fabrication more complicated and implies several restrictions on the choice of the barrier material: i) no intermixing between the cap and the silicided metals, and ii) the sacrificial cap has to be removed selectively to the other materials such a metallic gate, silicide contacts, dielectrics etc. An alternative solution to prevent oxidation during the silicidation is to form the silicide under ultra-high vacuum condition (UHV).

In this paper, we propose a detailed analysis, of the ytterbium silicide formed by *in situ* UHV annealing, without using any protective layers. This analysis was performed

with X-ray photoemission spectroscopy (XPS) and X-ray diffraction (XRD), transmission and scanning electron microscopy (TEM) and low temperature-dependent current-voltage measurements for the Schottky barrier height (SBH) extraction. Finally, SB-MOSFETs with ytterbium silicide based S/D contacts were fabricated on an ultra thin body SOI substrate.

## Fabrication and Characterization of YbSi<sub>x</sub> thin film

### Sample preparation

The YbSi<sub>x</sub> film was formed on lowly doped ( $10^{15} \text{ cm}^{-3}$ ) n-type Si (100) substrates. Wafers were cleaned in sulfuric peroxide mixture (SPM, 1:1) for 5 min, rinsed in de-ionized water (DI H<sub>2</sub>O) and blown dried with the nitrogen (N<sub>2</sub>). Wafers were subsequently dipped into 1% hydrofluoric acid (HF) for 30 s to remove the native oxide, rinsed, and dried as previously. Immediately after the cleaning procedure, the samples were loaded into the introduction chamber of the evaporator. A 20 nm thick layer of ytterbium was deposited by e-beam under UHV (base pressure is  $\sim 5 \times 10^{-9}$  mbar) with a typical deposition rate of 1 Å/s. Before each deposition step, the Yb-target was cleaned by evaporation of about 20 nm, the shutter being closed. Finally, the wafers were transferred to the annealing chamber ( $5 \times 10^{-9}$  mbar), without breaking the vacuum and annealed during 1 hour at different temperatures. After cooling down to room temperature, the samples were unloaded and the unreacted Yb was removed using a SPM (1:1) solution.

The SBH measurements were performed on specific samples that account for the lateral disposition of S/D regions in a typical MOSFET architecture. These test structures consisted in 1000 μm x 1000 μm two square silicided pads separated by a gap defined by e-beam lithography to produce back-to-back junctions. To define the pattern, Hydrogen Silsesquioxane (HSQ) was used. After annealing, HSQ approaches the structure of SiO<sub>2</sub>. The thickness of the obtained oxide is 200 nm. The cleaning procedure, the silicidation and the removal of the unreacted metal was same as for the previous samples.

### XRD and XPS analysis

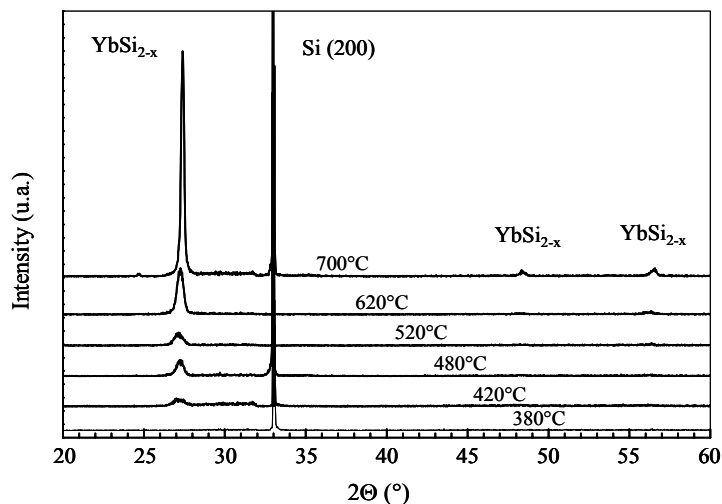


Figure 1. XRD analysis for Yb(20 nm)/Si (001) stacks UHV annealed for 1 hour.

Fig.1 presents the XRD analysis for Yb(20 nm)/Si (001) stacks annealed for 1 hour at different temperatures. For all samples, the XRD spectra were acquired after the wet etch of unreacted Yb. The ytterbium silicide forms at the temperatures higher than 380°C and presents only one YbSi<sub>2-x</sub> phase. The peak of YbSi<sub>2-x</sub> phase becomes stronger with increase of the annealing temperature ( $T_{an}$ ) that corresponds to an increase of the crystallized YbSi<sub>2-x</sub> thickness. Below 420°C, only the Si substrate diffraction peak was recorded. The cross-sectional TEM analysis of the sample annealed at 380°C, not presented here, shows the formation of very thin (~7 nm) Yb-Si layer. Any evidence of crystalline grains in this layer was not found, from what it is concluded that the Yb-Si film formed at this temperature is still amorphous. It is worth noting that contrary to the ytterbium silicide fabricated by *ex-situ* RTA without protective cap layers (5) the formation of ytterbium oxide was not detected for all annealing temperatures.

For the evaluation of the quality of the formed Yb-Si layers and their possible contamination by oxygen, XPS analyses were performed. Fig. 2 shows the atomic concentration depth profiles for the samples annealed for 1 hour at 380°C, 420°C and 620°C.

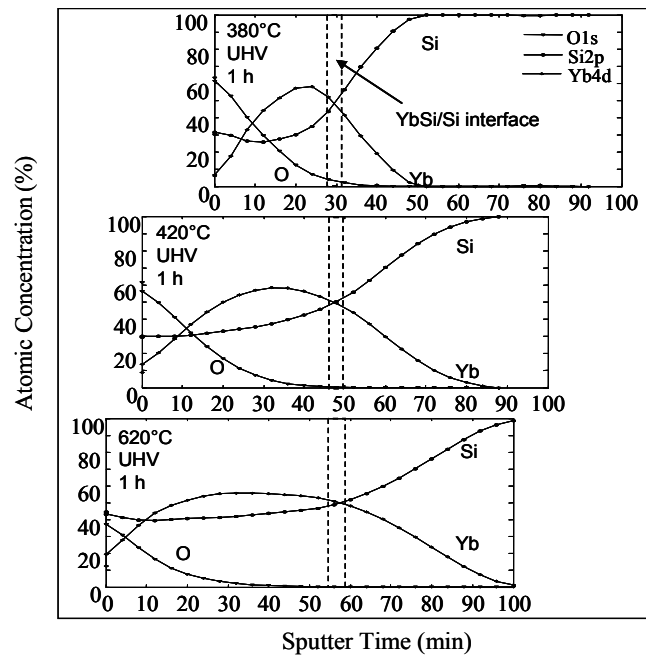


Figure 2. Atomic concentration depth profiles for the YbSi/Si samples annealed during 1 hour at 380°C, 420°C and 620°C.

Comparing these three growth conditions, it can be easily observed that for the high annealing temperatures, 420°C and 620°C, only the top part of the formed Yb-Si film is contaminated with oxygen. The very important fact is that contamination did not propagate down to the YbSi/Si interface, because it can be responsible for the high SBH value (6). On the other hand, the sample annealed at the lowest temperature, 380°C, contains oxygen over the whole thickness of the formed Yb-Si layer. This fact can have a negative impact on the Schottky barrier height. Based on XRD analyses, we can conclude that the formed oxides are in the amorphous state because of the absence peaks corresponding to the ytterbium or silicon oxides. Luo *et al.* (7) gave a detailed analysis on the growth kinetics of Er and Tb silicides in UHV. They demonstrated that after the

annealing the formed film was composed of the three parts: epitaxial RE silicide, amorphous RE-Si layer and unreacted RE metal. The presence of the amorphous layer on the top part of the formed silicide was also demonstrated for the Er silicide fabricated by RTA (8, 9). In our case, samples were treated with a SPM solution after UHV annealing in order to remove completely unreacted Yb. Thus, it was concluded that the amorphous layer was completely oxidized during the etch.

### Schottky barrier height measurements

SBH measurements were performed on back-to-back Schottky diodes. The current-voltage curves were recorded in the temperature range between 320 K and 160 K and transformed into Arrhenius plots ( $1/T^2$  versus  $1/T$ ) for some selected biases. Each Arrhenius plot was fitted thereafter with a complete Schottky transport model that continuously combines thermionic emission (TE), field emission (FE), and barrier lowering (BL) due to image charge (3).

The measurements were performed the samples annealed for 1 hour at temperatures in the 380-620°C range. The extracted SBH to electron are presented in Fig.3. No significant variation of the barrier height was noted in this temperature range with an average value close to 0.32 eV. The lowest SBH value (0.29 eV) was found the diodes fabricated at 520°C. The highest SBH value (0.33 eV) was measured for the sample annealed at 380°C. As it was mentioned above, the Yb-Si film formed at this temperature is: i) amorphous and ii) fully contaminated with the oxygen. These two facts can explain such a high SBH value.

The influence of the substrate doping level on the Schottky barrier height was also investigated. For this purpose, back-to-back Schottky diodes were implemented on a moderately doped ( $5 \times 10^{17} \text{ cm}^{-3}$ ) n-type Si (100) substrate. The  $\text{YbSi}_{2-x}$  film was formed at the sole temperature of 480°C. The corresponding barrier height was extracted at 0.28 eV (Fig.3). Thus, a reduction of SBH of 40 meV was obtained. This result shows a perspective for using the dopant segregation technique for ytterbium silicide.

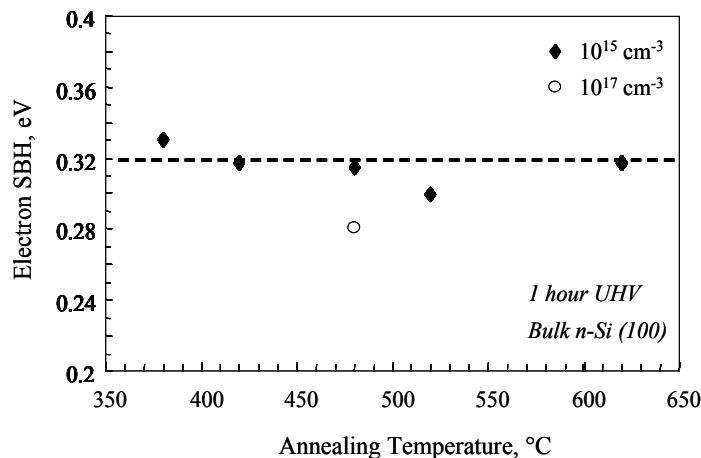


Figure 3. Evaluation of SBH to electron with UHV annealing temperature. The measurements were realized for the samples on the low doped (black diamonds) and moderately doped (open circle) substrates.

## YbSi based SB-MOSFETs

It is well known that ytterbium reacts with  $\text{SiO}_2$  (10). This reaction becomes stronger when the silicidation temperature is increased. It was noted that for diodes fabricated at  $T_{\text{an}} > 480^\circ\text{C}$ , a leakage current was measured for several devices. Therefore, to avoid the reaction of metallic ytterbium with the isolation/spacer region, the maximum silicidation temperature for the MOSFET fabrication was restricted to  $480^\circ\text{C}$ .

For RE integration, SOI MOSFETs devices originating from STMicroelectronics, which have the great advantages to offer a very simple integration path because no other process steps than silicide formation and metal stripping are needed. These devices feature a high-K dielectric with TiN / polysilicon gate on a thin SOI body (8nm). For the fabrication of the Source/Drain contacts, a 12 nm thick Yb layer has been deposited and annealed in UHV for 1h at  $480^\circ\text{C}$ . A SPM stripping solution was subsequently applied to remove the unreacted metal. Fig.4 shows the static characteristics of a  $1\ \mu\text{m}$  YbSi S/D MOSFET. These characteristics reveal the signature of a high Schottky barrier ( $\sim 0.3\text{eV}$ ) at the S/D junction. In particular, current flattening on the  $I_d\text{-}V_g$  characteristics at the transition between the subthreshold and the weak accumulation regime and the non saturation of the  $I_d\text{-}V_d$  characteristics are clearly observed

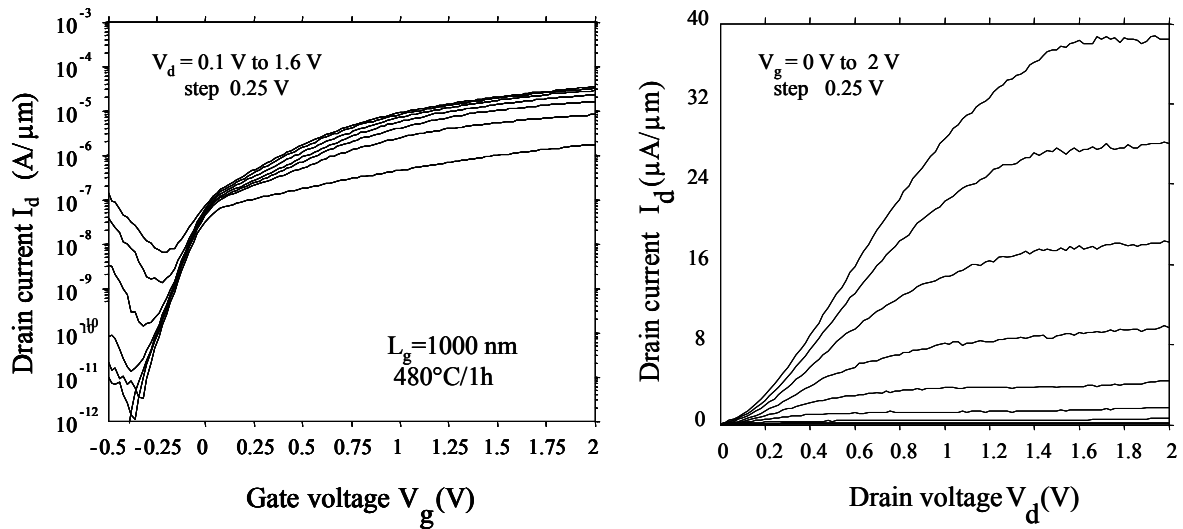


Figure 4. I-V characteristics of  $1\ \mu\text{m}$  gate long n-type SB-MOSFETs, with Yb silicide source/drain contacts obtained by UHV at  $480^\circ\text{C}/1\text{h}$ .

In conclusion, the structural and electrical analysis of  $\text{YbSi}_{2-x}$  thin film fabricated in UHV condition without any protective cap layer was presented. The fabrication of n-type SB-MOSFETs with YbSi-based S/D formed at  $480^\circ\text{C}$  was also demonstrated. Beyond the demonstration of YbSi integration in a self-aligned silicide scheme, it is anticipated that YbSi coupled to a low temperature dopant segregation technique can substantially decrease the specific contact resistance for n-type devices (11, 12).

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