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Arsenic-Segregated Rare-Earth Silicide Junctions: Reduction of Schottky Barrier and Integration in Metallic n-MOSFETs on SOI

Guilhem Larrieu, *Member, IEEE*, Dmitri A. Yarekha, Emmanuel Dubois, *Member, IEEE*, Nicolas Breil, and Olivier Faynot

Abstract—As an attempt to considerably reduce the equivalent contact resistivity of Schottky junctions, this letter studies the integration of rare-earth silicides, known to feature the lowest Schottky barriers (SBs) to electrons, coupled with a dopant segregation based on arsenic (As^+) implantation. Both erbium (Er) and ytterbium (Yb) have been considered in the *implant-before-silicide* (IBS) and *implant-to-silicide* flavors. It is shown that the two schemes coupled with a limited thermal budget (500 °C) produce an SB below the target of 0.1 eV. The implementation of IBS arsenic-segregated $\text{YbSi}_{1.8}$ junctions in an n-type SB-MOSFET is demonstrated for the first time resulting in a current-drive improvement of more than one decade over the dopant-free counterpart.

Keywords—Dopant segregation (DS), MOSFETs, rare-earth (RE) silicide, Schottky barrier (SB), silicon, Silicon-on-insulator (SOI).

I. INTRODUCTION

AS CMOS scaling approaches the deep decananometer range, the metallic source/drain (S/D) architecture holds the distinctive advantage to relax severe constraints imposed to conventional implanted S/D [1] because the doped extensions are replaced by low-resistance metallic junctions that potentially offer atomically sharp silicide/silicon interfaces. As far as electron transport is considered, rare-earth (RE)-based silicides are known to present the lowest Schottky barrier (SB) heights (SBH), around 0.27–0.28 eV in the best case [2], [3]. However, n-MOSFETs featuring RE-silicide S/D have revealed that the barrier height remains too large, resulting in device performance that is limited by the efficiency of thermionic and tunnel emission [4]–[6]. Considering that the SBH should not exceed

0.1 eV in order to position SB-MOSFETs advantageously with respect to conventional technology [7], the elaboration of an efficient barrier-modulation technique appears inescapable to promote electron injection through the barrier. Recently, according to the so-called dopant-segregation (DS) technique, it has been demonstrated [8]–[11] that dopant implantation and subsequent pileup at the metal/semiconductor interface significantly lowers the effective barrier height of Schottky junctions at reduced thermal budget. As far as DS technique in functional devices is considered, n-MOSFETs have been demonstrated based on arsenic S/D implantation cointegrated with midgap silicides, e.g., nickel [8] and cobalt [9] silicides. The same technique was also applied using a sulfur implantation, a double donor, combined with NiSi [10]. Nevertheless, the association of n-type dopants to a conduction band-edge silicide (e.g., $\text{ErSi}_{1.7}$, $\text{YbSi}_{1.8}$) appears as the most promising approach that takes advantage of the low initial SBH and of the additional barrier lowering and thinning induced by DS. This methodology that combines a band-edge silicide to its appropriate dopant type has been demonstrated for p-type MOSFETs through the implementation of PtSi coupled with boron (acceptor) segregation [11]. In this letter, arsenic-segregated RE metallic junctions based on the *implantation-before-silicidation* (IBS) and *implantation-through-silicide* (ITS) approaches are compared in terms of SB reduction. For the first time, arsenic-segregated $\text{YbSi}_{1.8}$ S/D junctions are also implemented in a thin-film Silicon-on-insulator (SOI) n-MOSFET, and the improvement of current drive over dopant-free RE SB-MOSFETs is discussed.

II. SCHOTTKY-JUNCTION ENGINEERING USING DS

For the sake of SB measurement, simple metallic junctions were fabricated on lowly doped ($10 \Omega \cdot \text{cm}$) n-type (100) Si wafers. The dedicated test structures consisted of $200 \times 200 \mu\text{m}^2$ square-shaped silicided contacts separated by a micrometer gap defined by lithography to produce back-to-back junctions [12]. Because of the extremely high sensitivity of RE elements to oxygen, care has been taken to limit or suppress any oxidation reaction at the silicide/silicon interface by operating in ultrahigh vacuum (UHV) during the RE deposition and silicidation steps. After a 1-% HF dip to deoxidize the silicon surface, a 15-nm-thick erbium or ytterbium layer was deposited using e-beam evaporation. Samples were transferred to the annealing chamber (5×10^{-9} mbar) without breaking vacuum and annealed for 1 hour at 480 °C for Ytterbium and 500 °C

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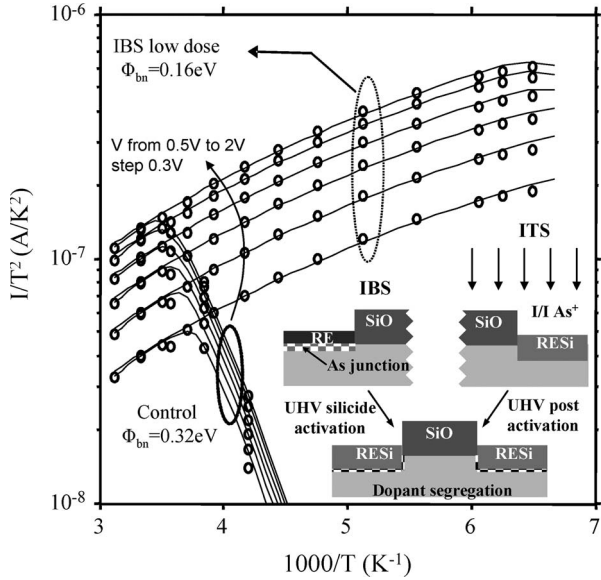


Fig. 1. $\text{YbSi}_{1.8}$ contacts formed at 480°C : experimental Arrhenius plot of back-to-back junctions and calculated characteristics using a transport model that includes thermionic and tunnel emission as well as barrier lowering by image-charge induction. The inset schematically illustrates how dopant segregation is introduced using the IBS and ITS schemes.

for Erbium in order to form $\text{YbSi}_{1.8}$ and $\text{ErSi}_{1.7}$ silicide layers, respectively. Depending on the process sequence, the implanted species (As^+) are either segregated simultaneously with the formation of the silicide, IBS or during a second annealing, after the formation of the silicide, in the ITS scheme (refer to the inset in Fig. 1). Monte Carlo simulations based on the TRIM code [13] were performed to determine the implantation conditions that favor the confinement of dopants in the narrow top layer. For the IBS scheme, two implantation doses have been considered (3×10^{13} and 10^{15} cm^{-2}) at low energy (1 keV). Under these conditions, impurities remain located in the top-most region where the silicidation reaction consumes silicon and can segregate at the interface while keeping the nonsilicided silicon region under the metallic contacts free of defects. For the ITS scheme, an implantation energy of 20 keV associated to a dose of 10^{15} cm^{-2} keeps the concentration level of implanted species under the upper bound of 10^{17} cm^{-3} at the silicide/silicon interface. The ITS postsilicidation thermal treatment was performed at 500°C under UHV for 30 min. Control samples, with Yb and Er silicides, were processed in parallel using the same silicidation sequence but without the implantation step. Based on the back-to-back junction configuration, SBH were determined using an extraction procedure that couples experimental data with a transport model that accounts for thermionic and tunnel emission as well as barrier lowering due to image-charge induction [14]. As an illustration, Fig. 1 shows the Arrhenius plots representative of the SBs to electrons (Φ_{bn}) of $\text{YbSi}_{1.8}$ contacts in the IBS case with a dose of $3 \times 10^{13} \text{ cm}^{-2}$ and for the control sample. The high-temperature section of the Arrhenius characteristics is known to be governed by the series resistance of the silicon gap between contacts [12]. Because the IBS and dopant-free samples exhibit the same high-temperature resistance, it can be concluded that the silicon resistivity in the intercontact gap remains unaffected

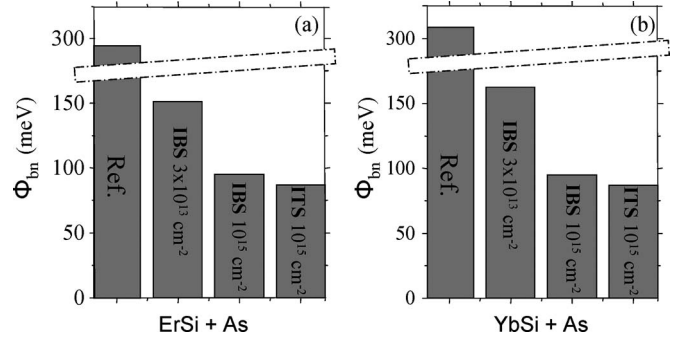


Fig. 2. Summary of SBH for electrons with As segregation on (a) $\text{ErSi}_{1.7}$ contacts formed at 500°C and (b) $\text{YbSi}_{1.8}$ contacts formed at 480°C . The ITS postsilicidation anneal was performed at 500°C under UHV for 30 min.

by the implantation step involved in the segregation technique. From Fig. 1, it also clearly appears that As segregation leads to an important reduction of the barrier height that evolves from 0.32 eV for dopant-free contacts to 0.16 eV for the IBS scheme, even with a low implanted dose. Fig. 2 presents a synthetic view of SBH to electrons (Φ_{bn}) extracted on both $\text{ErSi}_{1.7}$ contacts [Fig. 2(a)] and $\text{YbSi}_{1.8}$ contacts [Fig. 2(b)] with arsenic segregation implemented using both the IBS and ITS schemes. For the sake of comparison, the barrier height of the dopant-free control sample was extracted at 0.28 eV and 0.32 eV for $\text{ErSi}_{1.7}$ and $\text{YbSi}_{1.8}$ contacts, respectively. Implemented on RE silicide, arsenic segregation obtained by IBS leads to an SBH lowering of 50% for a dose of $3 \times 10^{13} \text{ cm}^{-2}$ and an SBH below the 0.1-eV target for a dose of 10^{15} cm^{-2} . The ITS scheme with an As-implanted dose of 10^{15} cm^{-2} and an activation anneal at 500°C under UHV, features an SBH below 80 meV. The low-activation temperature prevents the diffusion of dopants in the silicon [11]. The observation that both the IBS and ITS schemes enable sub-0.1-eV SBH makes these segregation techniques attractive for integration in a low thermal-budget MOS process.

III. DEVICE INTEGRATION

IBS arsenic-segregated $\text{YbSi}_{1.8}$ junctions with a dose of 10^{15} cm^{-2} at 480°C have been integrated in a thin-film SOI MOSFET architecture because they provide the lowest SB coupled with a minimal thermal budget. The process was started with an 8-nm-thick SOI layer where devices were isolated using a trench down to the buried oxide. The gate stack was composed of a 3-nm-thick high- k dielectric (HfO_2), on the top of which was deposited a 10-nm-thick TiN layer and a 50-nm-thick layer of n-doped polysilicon. Using this gate process, an equivalent oxide thickness of 1.7 nm was obtained. The gate stack was subsequently patterned, followed by the formation of thin SiO_2 gate sidewalls. Lastly, $\text{YbSi}_{1.8}$ S/D contacts with and without DS were integrated using a conventional self-aligned silicide process. The excess of Yb was selectively removed with respect to $\text{YbSi}_{1.8}$ using a sulfur-peroxide mixture.

Fig. 3 compares the I_d - V_g characteristics of 1- μm [Fig. 3(a)] and 100-nm [Fig. 3(b)]-long MOSFETs with As-segregated $\text{YbSi}_{1.8}$ S/D and similar transistors without DS (control devices). From a qualitative standpoint, the $\text{YbSi}_{1.8}$ control

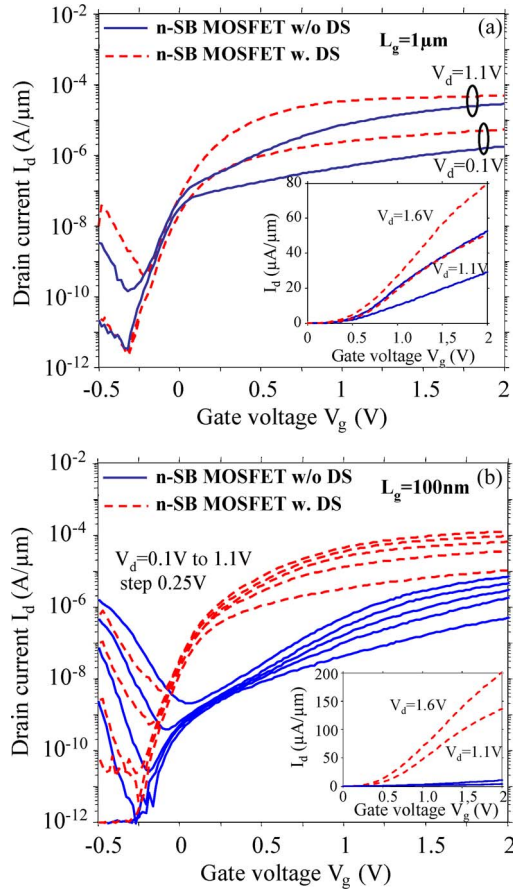


Fig. 3. Measured $I_{DS}-V_{GS}$ characteristics of n-type SB-MOSFETs that integrate $\text{YbSi}_{1.8}$ S/D junctions with and without dopant segregation. Arsenic-segregated junctions are performed by IBS at 480°C with a dose of 10^{15} cm^{-2} . Gate length is (a) $1\ \mu\text{m}$ and (b) 100 nm . In the inset, the $I_{DS}-V_{GS}$ characteristics in linear format for $V_d = 1.1\text{ V}$ and 1.6 V .

SB-MOSFET exhibits a perceptible flattening of the $I_{ds}-V_{gs}$ characteristics at the transition between the subthreshold and weak-inversion regimes ($0 < V_g < 0.5$), which reveals a major drawback of SB n-MOSFETs with RE silicide contacts [4]–[6]. This effect is the clear signature of limited injection at the source when the channel is pushed in strong inversion due to the large SB ($\sim 0.32\text{ eV}$). Obviously, such a limitation is not observed for DS S/D Schottky extensions owing to the drastic SBH reduction. The benefit in terms of current drive is unveiled by the $I_{ds}-V_{gs}$ in linear scale [inset Fig. 3(a)] that reveals a $\sim 50\%$ improvement for the $1\text{-}\mu\text{m}$ device. The benefit of DS is even better illustrated in the case of the 100-nm gate-length device [Fig. 3(b)] because the lower channel resistance exacerbates current performance limitations due to the S/D extensions. In particular, Fig. 3(b) clearly shows poor operation of the dopant-free S/D SB-MOS because current injection is severely hampered by a prohibitive SBH. In contrast, the As-segregated counterpart does not show such limitation and features a maximum current drive $I_{on} = 252\ \mu\text{A}/\mu\text{m}$ at $V_g = V_d = 2\text{ V}$ which represents more than a $10\times$ improvement over the control device.

IV. CONCLUSION

Based on arsenic pileup obtained by segregation at low temperature (500°C), the ITS and IBS schemes have been successfully implemented to produce RE silicide SB to electron below 0.1 eV . The low temperature (500°C) integration of arsenic-segregated $\text{YbSi}_{1.8}$ Schottky extensions in thin-film SOI MOSFETs has been demonstrated for the first time. DS is shown to dramatically improve current injection as revealed by more than a decade increase of the drive current at 100-nm of gate length. In summary, the association of n-type dopants (donors) to conduction band-edge silicides opens new perspectives to competitively integrate metallic S/D contacts in n-MOSFETs with the distinctive advantage to considerably relax constraints associated to ion implantation and thermal activation.

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