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A Simple Method for Measuring Si-Fin Sidewall Roughness by AFM

Xiaohui Tang, Vincent Bayot, Nicolas Reckinger, Denis Flandre, *Senior Member, IEEE*, Jean-Pierre Raskin, *Senior Member, IEEE*, Emmanuel Dubois, and Bernard Nysten

Abstract—The gate oxide reliability and the electrical behavior of FinFETs are directly related to the surface characteristics of the fin vertical sidewalls. The surface roughness of the fin sidewalls is one of the most important structural parameters to be monitored in order to optimize the fin patterning and postetch treatments. Because of the nanometer-scale dimensions of the fins and the vertical orientation of the sidewall surface, their roughness measurement is a serious challenge. In this paper, we describe a simple and effective method for measuring the sidewall morphology of silicon fins by conventional atomic force microscopy. The present methodology has been employed to analyze fins as etched by reactive ion etching and fins repaired by sacrificial oxidation. The results show that sacrificial oxidation not only reduces the roughness of the sidewalls, but also rounds the top corners of silicon fins. The present method can also be applied to characterize sidewall roughness of other nanostructures and materials such as the polysilicon gate of transistors or nanoelectromechanical beams.

Index Terms—Atomic force microscopy (AFM), FinFET, roughness of silicon fin sidewall, sacrificial oxidation.

I. INTRODUCTION

FIN FET [1], a nonplanar double-gate transistor usually built on a silicon-on-insulator (SOI) substrate, is a promising candidate for CMOS scaling down to the 10-nm regime. In previous years, several electrical characterizations of FinFET [2] have demonstrated its effective control of short-channel effects [3], higher current drive, and scalability [4]. The CMOS compatibility of its fabrication process flow explains the growing interest of the microelectronics industry for the advanced MOS architecture.

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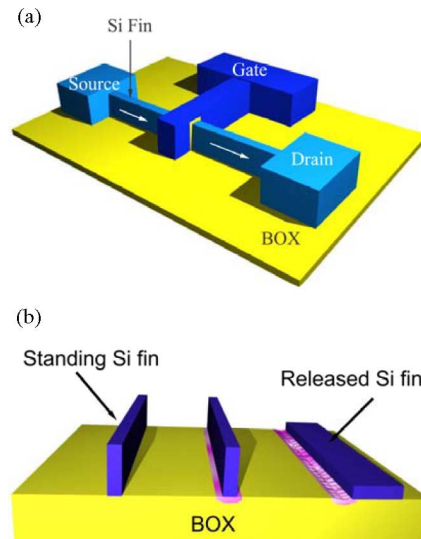


Fig. 1. (a) 3-D scheme of a FinFET showing the fin sidewall and current drive direction. (b) 3-D scheme of Si fins showing a standing fin and released fin after etching away the BOX.

In a FinFET, the drive current flows along the vertical sidewalls of Si-fin [see arrow direction in Fig. 1(a)]. The surface quality of the sidewalls, thus, strongly influences the gate insulator reliability and the device electrical performance. Rough sidewalls result in carrier mobility and lifetime reduction [5], current drive decrease, subthreshold swing deterioration, leakage current, and low-frequency noise increase [6], [7]. It is worth noting that the Si-fin sidewall roughness impacts *n*-type FinFETs more severely than *p*-type FinFETs. Indeed, the inversion charge centroid of electrons is closer to the surfaces of the fin sidewalls than that of holes [8]. Hence, electron mobility is more affected than hole mobility through surface scattering phenomenon. It is, therefore, of foremost importance to quantitatively characterize the Si-fin sidewall roughness and effectively improve the as-etched Si-fin sidewall quality for building high-performance FinFETs. Besides the specificity of the FinFET architecture, the control of the line-edge roughness (LER) of the gate becomes a major issue as the size of the CMOS devices further shrinks. A gate length less than 10 nm with large LER causes fluctuations of the device characteristics. The International Technology Roadmap for Semiconductors (ITRS) [9] specifies a requirement of 2.8 nm for the LER for the year 2009 and smaller values for subsequent years. Similar concerns exist for the fabrication of reliable nanoelectromechanical systems (NEMSs) featuring sub-100 nm dimensions [10], [11].

Up to now, only few works evaluating the Si-fin sidewall and LER have been reported. This is because rare instruments are suited for such measurements. Although atomic force microscopy (AFM) with its high resolution has proven to be a powerful tool to study, image, and manipulate the surface of nanoscale systems [12], [13], it still has certain limitations for profiling vertical sidewalls. For instance, Marrinello *et al.* [14] tilted the measured sample by an angle for the point-shaped tip to close untouchable regions at sidewall's bottom, and Martin and Wickramasinghe [15] used a modified tip (a boot-shaped tip) to obtain a high lateral resolution. However, these methods are not really suitable for scanning the sidewall of a Si-fin along the channel direction [current flow direction, see Fig. 1(a)], even using assembled cantilever probes, as recently reported by Dai *et al.* [16], [17]. In the other hand, Gondran *et al.* [18] proposed to cleave the sample along the length of the fin (channel direction) and polish the sample edge using focused ion beam to approach the fin's sidewall. This method is rather complicated since it requires sophisticated equipment to prepare the sample, without mentioning the difficulty to cleave the sample perfectly parallel to Si-fin sidewall to be measured.

In this paper, we present a simple and effective method to deeply analyze the sidewall morphology of Si-fins using conventional AFM. Contrary to the methods mentioned previously, the present technique requires neither special tips nor cleaving of the sample. The main idea is to release the fins to present the sidewall surface to be measured [see Fig. 1(b)]. The release of the Si-fins can be obtained by simply etching away the buried oxide (BOX) on which the Si-fins stand on. After that release step in a hydrofluoric acid (HF) based solution, the Si-fins present one of their sidewall surfaces parallel to the substrate, thus being exposed to AFM tip for the analysis. This simple procedure is quite powerful to quickly analyze, and then optimize the etch conditions and the postetch treatments for the fabrication of high-quality Si-fins. The sidewall roughness of as-etched and repaired Si-fins has been measured by using the present method.

II. SAMPLE PREPARATION

A *p*-type SOI wafer with a BOX thickness of 400 nm, which is a common substrate for building *n*-type FinFETs, is used as starting material. The 200-nm-thick Si film is thinned down to 80 ± 1 nm by a wet etching in a solution ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ 1:8:64 mixture) [19]. Then, a 30-nm-thick oxide is deposited on top of the film by low-pressure chemical vapor deposition to serve as a hard mask. Fins with a width of 30 nm are patterned using electron-beam lithography. The longitudinal direction of the fins is chosen parallel to the [1 1 0] wafer direction, so that the fin sidewall surface is in the (1 1 0) plane. The hard mask is etched by CHF_3 with a gas flow rate of 500 sccm and a power of 50 W. The Si-fins are etched by reactive ion etch (RIE), which is performed under a pressure of 25 mTorr with a SiCl_4 gas flow rate of 20 sccm and a power of 40 W. In this step, the Si etch rate is 43 nm/min, and the selectivity for Si to SiO_2 is about 15:1. Sacrificial oxidation [20] is carried out at 950 °C for 5 min to smooth and repair the sidewalls

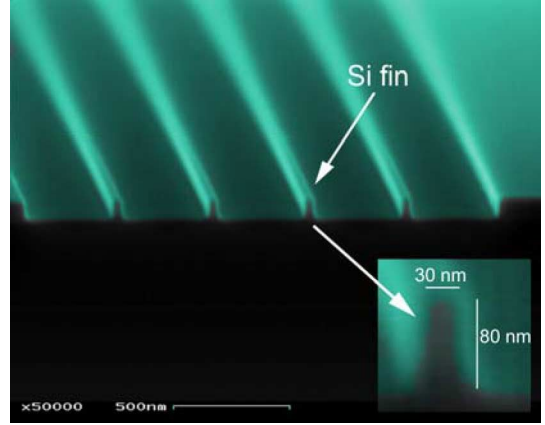


Fig. 2. SEM cross sections of repaired Si-fins. The fins have a width of 30 nm and a height of 80 nm.

damaged by RIE. Fig. 2 shows a scanning electron microscope (SEM) image of the repaired fins (sample A): the fin has a width of 30 nm, a height of 80 nm, a length of 848 μm , and a pitch of 400 nm. It can be seen that the fin sidewalls are quite steep, which permits the fin to be flat when it is released after removing the BOX. In order to compare the sidewall roughness before and after sacrificial oxidation, as-etched fins (sample B) are also characterized using the same technique. Finally, the fins are released for the characterization of the sidewall surface. For this purpose, both samples are immersed in buffered HF (BHF) for 20 s at room temperature to remove the BOX of the SOI wafer and rinsed in deionized water to clean the residual BHF. The BHF is composed of 40% NH_4F and 49% HF (85.5:12.5), and the etch rate of the BOX in BHF is about 60 nm/min. The 30-nm-wide fins are completely released after an etch time of less than 20 s since the etching is carried out from two sidewalls. In this step, not only the BOX is removed, but also the residual hard mask is removed in 20 s. As a result, the Si-fins are floating, either broken or intact, and lay on the silicon substrate, as shown in Fig. 3 (a) and (b), and Fig. 4 (a) and (b). It is worth noting that the thermal oxide (grown during sacrificial oxidation) surrounding the Si-fins of sample A is also removed during their release from the BOX.

III. ROUGHNESS MEASUREMENT OF SI-FIN SIDEWALLS

AFM analysis is performed under ambient condition on a multimode Nanoscope IV (Veeco Instruments) operating in amplitude-modulated mode. The used cantilever (Super Sharp Silicon SPM-sensor from Nanosensors) [21] has a resonance frequency around 70 kHz and a typical spring constant of 5 Nm^{-1} . On this type of sensors, the tip has an aspect ratio better than 4:1 and the apex radius of curvature is less than 5 nm. The free and set-point amplitudes are set to 15 and 10 nm, respectively. Image processing and analyses are performed using home-made procedures developed under Igor Pro software (Wavemetrics). Images are flattened with a plane fit procedure (subtraction of an average plane), and are analyzed without any further treatment.

For each sample, images of several released Si-fins are acquired to perform a statistical analysis of the sidewall roughness.

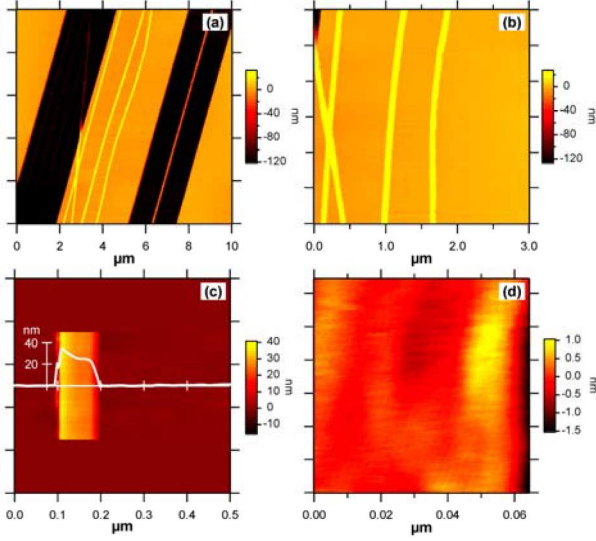


Fig. 3. AFM images of repaired Si-fins (sample A). (a) General view of released and standing up fins. (b) Zoom on four released fins. (c) Details of left fin visible in (b). (d) Zoom on the sidewall of the fin presented in (c). The white curve in (c) is the cross section profile of the fin measured along the horizontal line.

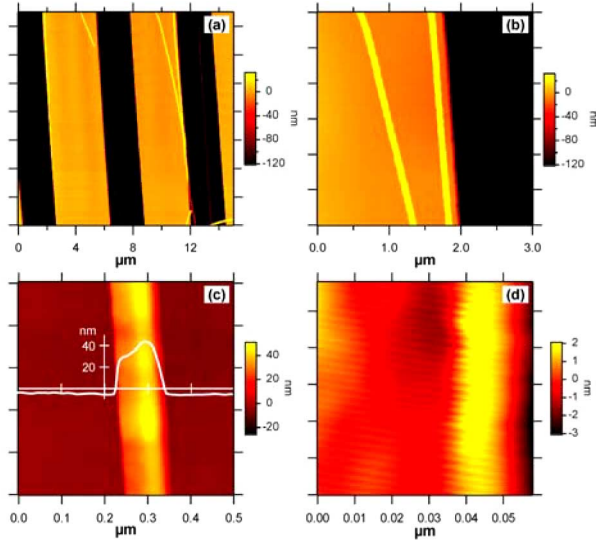


Fig. 4. AFM images of as-etched Si-fins (sample B). (a) General view of released fins. (b) Zoom on two released fins. (c) Details of left fin visible in (b). (d) Zoom on the sidewall of the fin presented in (c). The white curve in (c) is the cross section profile of the fin measured along the horizontal line.

Images of the repaired and as-etched Si-fins are shown in Figs. 3 and 4, respectively. Figs. 3(c) and 4(c) present cross section profiles of the released Si-fins. The measured height (corresponding to the fin width) ranges between 25 and 35 nm, which are consistent with the targeted value of 30 nm. The sidewall width (corresponding to the fin height) is measured around 100 nm, i.e., a value slightly larger than the actual height of the fins (80 nm). This larger value may be explained by image widening (or dilation) effects [22], namely, the finite tip size produces a widening of the lateral size of the surface features. In the present case, the maximum widening D can be estimated based on the relation

$D = 2R + h/A_r$, where R is the tip apex radius of curvature, A_r is the tip aspect ratio factor, and h is the sidewall height. With $R \leq 5$ nm, $A_r = 4$, and $h = 30$ nm, the widening is estimated to be equal or less than 17.5 nm leading to an expected apparent width ≤ 97.5 nm, consistent with the measured values.

From the large-scale images (typically $1 \mu\text{m} \times 1 \mu\text{m}$), the large-scale LER of the Si-fins was estimated as follows. 5-pixel-wide and $1\text{-}\mu\text{m}$ -long line profiles were measured along released fins. The LER was estimated by calculating the rms roughness of the line profiles and by averaging the values measured on different profiles measured on various fins. The obtained values are equal to 2.0 ± 1.3 nm for the as-etched fins and 1.1 ± 0.3 nm for the repaired fins.

Small-scale images [$60 \text{ nm} \times 60 \text{ nm}$, see Figs. 3(d) and 4(d)] are also acquired on several Si-fins. The rms roughness of the fin sidewall is calculated from those images. The average values are 0.25 ± 0.05 and 0.55 ± 0.10 nm for the repaired and as-etched fin sidewalls, respectively. The roughness of the sidewall surface is approximately reduced by a factor of 2 after repairing.

To further illustrate this, the circular average power spectral density (PSD) of the $60 \text{ nm} \times 60 \text{ nm}$ images is then calculated. The PSD curves extracted from several images are merged to obtain an average PSD curve, which statistically represents the fin sidewall surfaces. Based on the average PSD curves, the variation of the rms roughness (σ) as a function of the length scale (r) is calculated using the following relation:

$$\sigma(r) = \left[2\pi \int_{1/r}^{s_{\text{max}}} \text{PSD}(s) s ds \right]^{1/2}$$

where s is the spatial frequency and s_{max} is the maximum spatial frequency or Nyquist frequency, $s_{\text{max}} = N/(2L)$, with N and L being the image lateral pixel number and size, respectively.

The length-scale dependence of σ is presented in Fig. 5. It shows that the repaired and as-etched Si-fins have comparable sidewall roughness at length scales lower than 2 nm. It is worth noting that, when the length scale is much smaller than the curvature radius of the tip (i.e., less than 5 nm in the present case), roughness determined by AFM may not reflect the actual roughness anymore. When the length scale is higher than 3 nm, the rms roughness is significantly improved after sacrificial oxidation.

In addition, it is found that the sidewall surface is rougher than the wafer surface after RIE (red lines in Figs. 5 and 6). This can be explained by the followings. The roughness of the wafer surface is mainly introduced by ion bombardment damage in RIE, while the roughness of the sidewalls is caused not only by ion bombardment damage, but also by the imperfectness of the hard mask in electron-beam lithography. The repair (at 950°C for 5 min) used here is efficient to restore the wafer surface roughness to the original value of the Unibond SOI wafer (0.2 nm), but it is incomplete for the sidewall surface with a higher roughness. To further smooth the sidewall surface, a longer oxidation time is needed. In the beginning of the thermal oxidation, the oxidant is sufficiently supplied, the rate-limiting process is the interface reaction where the oxide thickness is proportional to oxidation time. When the oxidation is further carried out, the rate-limiting

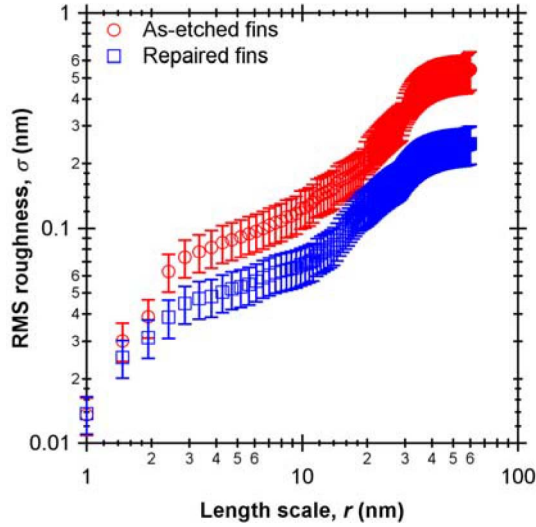


Fig. 5. RMS roughness as a function of length scale calculated from merged circular-averaged PSD's of the small-scale images of the Si-fin sidewalls. Error bars correspond to \pm the standard deviation on the data.

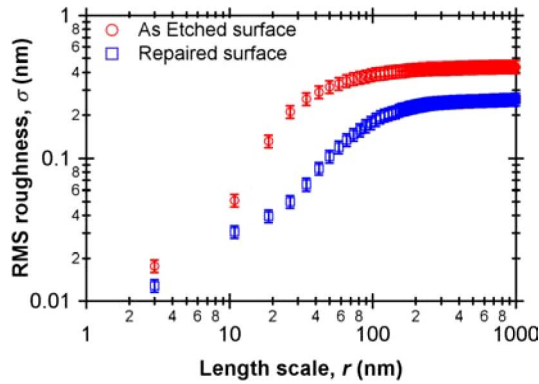


Fig. 6. RMS roughness as a function of length scale calculated from the circular-averaged PSD's of the image of the Si wafer surfaces. Error bars correspond to \pm the standard deviation on the data.

process becomes oxidant-supplying process, where the oxide thickness is proportional to square root of oxidation time. The surface smoothing happens during the oxidant-supplying period, because the oxidation supply rate at convex parts is higher than at concave parts of the oxidized Si surface [23]. Therefore, the oxidation time should be long enough to pass the rate-limiting period, thereby flattening the rougher sidewall. This is crucial for selecting postetch treatments and designing high-performance FinFET devices. In addition to sacrificial oxidation, the sidewall roughness of the Si-fins also can be improved by the other methods, such as hydrogen annealing [24] and chemical dry etching [25].

IV. CORNER TRANSFORMATION OF SI-FIN

The top corner shape of the Si-fins significantly affects the performance of FinFET device, i.e., sharp corners result in larger subthreshold sweep and higher off-state current [26], [27]. Hence, the measurement and control of the curvature radius for

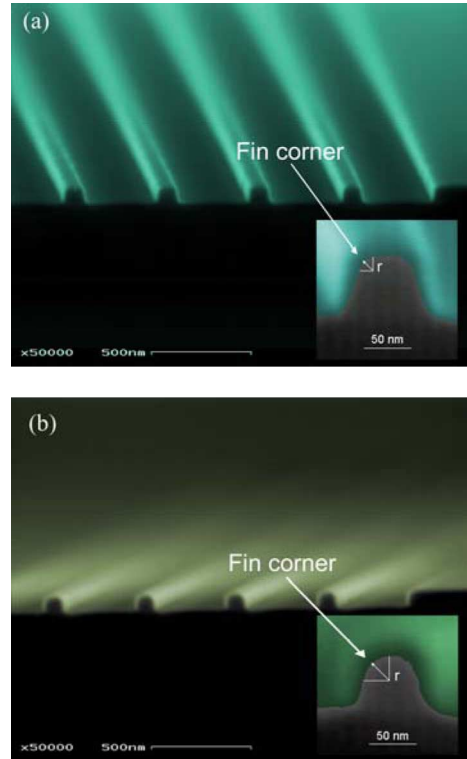


Fig. 7. (a) SEM cross sections of as-etched Si-fins by RIE. (b) SEM cross sections of repaired Si-fins by sacrificial oxidation, showing that sacrificial oxidation increases radii of curvature of the top corners.

the top corners of the fin are an important technological issue. Fig. 7(a) and 7(b) shows SEM images of cross-sectional profiles for four fins before and after the repair by sacrificial oxidation, respectively. It is clear that, after the repair, the top corners of the fins become rounded. According to the images, the radii of curvature of the top corners are estimated. For a fin with a cross section of $80 \text{ nm} \times 80 \text{ nm}$, the radius of curvature is increased from 15 to 28 nm after the repair. This implies that the corner effect can be eliminated and suppressed by sacrificial oxidation. The rounding of the top corners is attributed to higher oxidation rate in the regions of the top corners because oxygen atoms penetrate these regions from the sidewall as well as from the upper surface.

V. CONCLUSION

In this paper, we present a simple and effective method to release Si-fins for measuring their sidewall roughness by AFM. Like in a “lift-off” process, the BOX of the SOI wafer on which the Si-fins are placed is removed away, and the fins are lifted off. Some of them lay down with the sidewall exposed so that AFM measurements can be easily performed. This method is used to analyze Si-fins etched by RIE and Si-fins repaired by sacrificial oxidation. The results reveal that sacrificial oxidation has not only improved the rms roughness of the sidewalls, but also rounded the top corners of the Si-fins.

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Denis Flandre (S'86–M'91–SM'03) was born in Charleroi, Belgium, in 1964. He received the Electrical Engineer, Ph.D., and Postdoctoral Thesis degrees from the Université Catholique de Louvain (UCL), Louvain-la-Neuve, Belgium, in 1986, 1990, and 1999, respectively.

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Prof. Flandre has been a recipient of several awards. He participated, organized, or lectured in many short courses on SOI technology, devices and circuits, in universities, industries, and conferences. He has been a member of the Boards of the European (EU) Networks of Excellence for High-Temperature Electronics (HITEN), Silicon Nanodevices (SINANO/NANOSIL), and SOI technology (EUROSIL). He is a member of the SOI Consortium. In UCL, he is a member of the Research Center in Micro- and Nanoscale Materials and Electronics Devices (CERMIN), of the Director Board of the Cyclotron Research Center (CRC), Louvain-la-Neuve, and the Chairs the direction committee of the UCL Micro-/Nanotechnology Facility (Winfab).



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in silicon-on-insulator (SOI) technology for low-power, low-voltage applications. In 1998, he joined the Department of Electrical Engineering and Computer Science (EECS), The University of Michigan, Ann Arbor. During 2000, he was an Associate Professor in the Microwave Laboratory, UCL, where has been a Full Professor and the Head of the Microwave Laboratory since 2007. He has been involved in the development and characterization of micromachining fabrication techniques for microwave and millimeter-wave circuits, and microelectromechanical transducers/amplifiers working in harsh environments. He has authored or coauthored more than 350 scientific papers. His current research interests include modeling, wideband characterization, and fabrication of advanced silicon-on-insulator (SOI) MOSFETs as well as micro- and nanofabrication of microelectromechanical system (MEMS)/nanoelectromechanical system (NEMS) sensors and actuators.

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Emmanuel Dubois received the Ingénieur degree from the Institut Supérieur d'Electronique et du Numérique (ISEN), Lille, France, in 1985, and the Ph.D. degree from the University of Lille, Lille, in 1990.

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Dr. Dubois was the Coordinator of FP4-IST-QUEST (1997–1999), FP5-IST-SODAMOS (2001–2003), FP6-IST-METAMOS (2005–2008) European Projects, and was a Task Leader in the SINANO Network of Excellence (2005–2007). He is currently a Task Leader of the Silicon-Based Nanostructures And Nanodevices For Long-Term Microelectronics Applications (NANOSIL) European (EU) Network of Excellence (2008–2010) and a member of the Technical Advisory Committee of the Integrated Systems Technology (IST) Integrated Project PULLNANO.

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Prof. Nysten is the President of the Belgian Society of Microscopy (BVM-SBM) and the Wallonia Network for Nanotechnologies (NanoWal).

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