# Towards an airborne high temperature SiC inverter

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***Abstract*—SiC devices enable for high temperature operation of power converters. The paper describes the laboratory step by step work towards an airborne high temperature inverter : 200C cooling source, 4 kVA power. From 'JFET only' to 'full three phase power stage' tested up to 250C, including capacitor. Device samples are characterized in order to set the requirements for the gate driver and to evaluate maximum switchable power. Switching losses are measured using high precision shunt and voltage probes. A prototype is built and operation under full load (15A) is verified.**

## I. Introduction

*a) Project overview:* In the aircraft industry, the strong will to generalize the use of electrical actuators leads to an increasing demand on Power Electronics. The use of electricity allows for a significant reduction in aircraft weight, energy consumption and polluting fumes generation. In the more electrical aircraft, a general use of electrical actuator will allow a 10 % reduction in investment and maintenance costs and a 20 % reduction in aircraft weight. To get the full benefit of the electrification of actuators, Power Electronics converters must be integrated or placed in the vicinity of electromechanical systems. For example, the engine area where ambient temperature can reach 200°C, [1].

A 3-phase inverter is a suitable pilot converter to demonstrate high-temperature operation up to 200°C. Previous work has shown the feasability of inverters working at such temperatures using SiC JFETs as power switches, [2], [3], [4], [5], [6]. Different high temperature applications are concerned with the proposed study. Aircraft applications are for example SMART-EMA (Electro Mechanical Actuator) for braking systems (1 to 5 kW) and for engine speed control (1 to 2 kW), the specific mision profile is briefly described in table I.

*b) A step by step work:* Work started with first generation JFET (2A-1500V) implemented on a standard printed circuit board (FR4 double sided) with standard power components. High temperature was applied locally to the JFET's cases [2]. Today a full inverter leg has been heated up to 250°C and operated at currents up to 15A with a bus voltage of 540V, [7]. Recently we have implemented a module integrating the three legs, (6 JFET), with bank capacitor. This converter is presented in this paper. The ultimate step of this project is the integration of the full inverter whith drivers using Multi Chip Module technology and Silicon On Insulator gate drivers.

TABLE I
Basic aircraft mission profile

| | |
|---|---|
| Duration | 50 000 hours |
| Thermal cycles | 15000 |
| Thermal cycle | -55°C to 200°C |
| Power range | 1-50 kW |
| DC input | +/- 270V |
| AC output | 230V |
| Cooling temperature | up to 200°C |

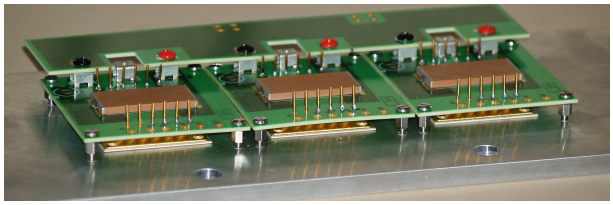

Fig. 1. First three phase inverter built with separate inverter legs

*c) The* SEFORA *project:* The main objective is to demontrate the reliable operation of power transistors with junction temperatures above 300°C, and packaging with ambient temperature above 200°C. SiC-JFET switches can be operated at frequencies above 100 kHz and at junction temperatures higher than 200°C. That has been already shown by different research studies. The research program SEFORA focuses on the prototyping of a 3-phase JFET voltage inverter including adapted and reliable packaging for high-temperature applications, transistor drivers on SOI technology, high-temperature capacitors, high-temperature voltage, current and temperature sensors and protection schemes. A pilot converter is designed with the following specifications :

- supply DC bus: 570V
- output current : 6A per leg output
- switching frequency: 20kHz to 300 kHz
- JFET junction temperature: near and above 300°C
- package ambient temperature: 200°C

SEFORA is a three year project started in 2007. It brings together french research laboratories and european companies. SiC JFET components are becoming available outside laboratories, the devices used in this work come from SiCED. High temperature operation is possible. An issue of high temperature is passive components. Capacitors are almost inexistent at

300°C while magnetic cores can be purchased on the web. The capacitor used in this work has been characterized up to 300°C. SiC JFETs have been tested working at 300°C and this temperature is limited by the environment of the SiC chips as the theoretical practical limit for SiC is around 500°C to 600°C for 1000V breakdown voltage, [7].

## II. Characterization

15A - 1200V SiC JFETs and the tank capacitor are characterized to study temperature effects on majors parameters. This knowledge is the basis for the design of the inverter. Temperature is set by a hot air furnace and verified by thermocouples placed on the metal case of the devices, ranging from 30°C to 300°C.

### A. JFET characterization

*1) JFET static characterization:* These results are mainly provided by [8]. Forward characterization at 25°C and 225°C shows the effect of temperature on the reduction of the saturation current : from 42A at ambient to 25A, see figure 3 and figure 4. The resistance of the conducting JFET, RDSon, can be extracted, see Table II. RDSon is increased by a factor of 2.5 as temperature rises from 25°C ambient to 225°C. JFET can be used in reverse conduction, at zero Gate voltage behaviour is almost symmetrical to forward conduction, it is a low value resistor. At high negative Gate bias, the JFET is fully depleted and canal is not conducting. A structural junction between source and drain, such as in a MOSFET, is present see figure 7. This internal diode is characterized, see figure 2, it has a forward voltage drop of around 3V. Because the JFET channel is able to conduct current in both directions, the internal diode is active during the dead-time of the inverter leg only, therefore expected conduction losses are very low.

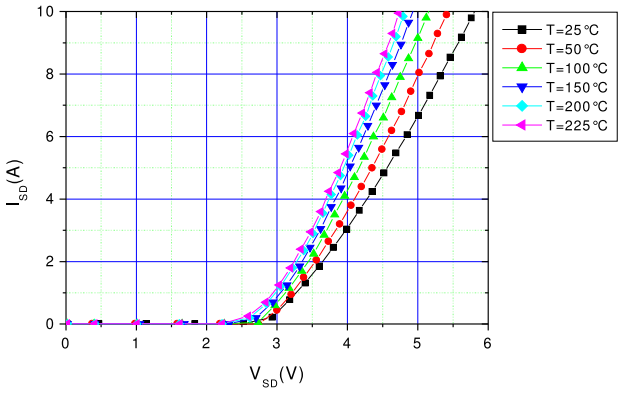


Fig. 2. Measured characteristic of the internal diode of the JFET. The JFET channel is turned off by a negative bias on the gate.

*2) JFET dynamic characterization:* In this part, the switching losses are experimentally measured at fixed operating points : DC bus voltage, switched current and temperature. The dynamic model of the JFET, briefly presented below, has not been validated at the time of writing, but data collected will be used for the experimental verification.

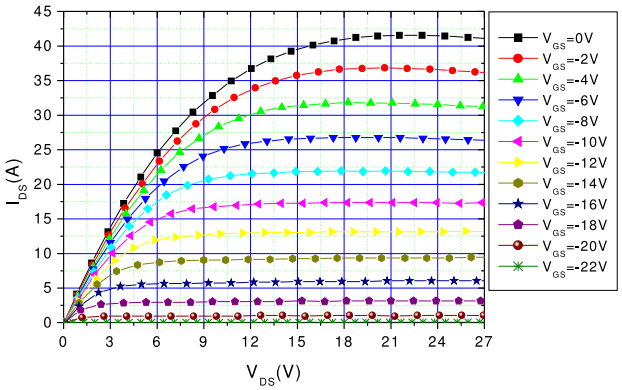


Fig. 3. Measured Kellog diagram of 15A JFET at room temperature

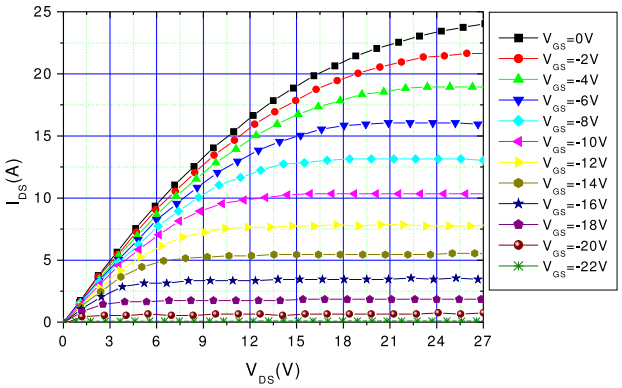


Fig. 4. Measured Kellog diagram of 15A JFET at 225°C

The switching losses are due to the simultaneous presence of voltage and current in the JFET during transients. The highest losses occurs at turn-On when the oposite JFET provoques a peak current. This peak is partly caused by a recovery mechanism, linked to the value of the current. The temperature dependency indicates a saturation limitation. The peak current is also dependant on voltage, which suggests a capacitive behaviour, see table III.

*3) JFET gate charge characterization:* The gate charge is measured using the same technique as for power losses.

TABLE II
RDSon versus temperature

| Temperature [°C] | RDSon [Ω] |
|---|---|
| 25 | 0,2 |
| 225 | 0.5 |

The complete diagram of resistance versus temperature can be found in [9]

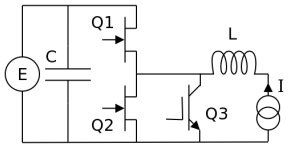


Fig. 5. Test circuit to measure switching losses and dynamic behaviour. Q1 and Q2 and JFETs under test. Voltage 'E' and Current 'I' are independent and also, are not the consequence of any conduction duration. The auxiliary power switch, Q3, by-passes the current source to avoid self heating of Q1 or Q2.

TABLE III
MEASURED TURN-ON AND TURN-OFF LOSSES

*25°C ambient temperature*

| E [V] | I [A] | Eon [uJ] | Eoff [uJ] | Ipeak [A] |
|---|---|---|---|---|
| 270 | 1 | | 17 | |
| 270 | 3 | 198 | 56 | 22,5 |
| 270 | 8 | 306 | 142 | 27,5 |
| 570 | 1 | 817 | 54 | 27 |
| 570 | 3 | 898 | 170 | 27,5 |
| 570 | 8 | 924 | 298 | 28 |

*200°C case temperature*

| E [V] | I [A] | Eon [uJ] | Eoff [uJ] | Ipeak [A] |
|---|---|---|---|---|
| 270 | 1 | 90 | 12 | 10,5 |
| 270 | 3 | 114 | 38 | 12,5 |
| 270 | 8 | 400 | 142 | 25,5 |
| 570 | 1 | 420 | 38 | 13 |
| 570 | 3 | 477 | 101 | 15 |
| 570 | 8 | 498 | 215 | 17,5 |

From table IV it can be observed that the gate charging requirements are almost not affected by temperature.

### *B. Capacitor characterization*

The variation of capacitance and series resistance of the capacitor is plotted against temperature up to 260°C. At 260°C, capacitance drops by 65%. The series resistance increases with temperature almost as much as capacitance as dropped, a times 3 factor. This measurement is based on a Hewlett-Packard impedance analyser, the capacitor is heated up by a hot air furnace, connecting high temperature wires are compensated for.

## III. JFET MODELLING

The JFET modelling approach is as much as possible based on physical parameters, mainly geometrical and material related. The model is writen using 'elements'. The conducting path is split in two :

TABLE IV
MEASURED GATE ENERGY

| E [V] | I [A] | Egoff [uJ] *25°C* | Egoff [uJ] *200°C* | Egon [uJ] *25°C* | Egon [uJ] *200°C* |
|---|---|---|---|---|---|
| 270 | 1 | 0,9 | 0,9 | | 0,4 |
| 270 | 3 | 0,8 | 0,8 | 0,4 | 0,4 |
| 270 | 8 | 0,7 | 0,7 | 0,4 | 0,4 |
| 570 | 1 | 1 | 1,1 | 0,5 | 0,5 |
| 570 | 3 | 0,9 | 1 | 0,5 | 0,5 |
| 570 | 8 | 0,8 | 0,9 | 0,5 | 0,5 |

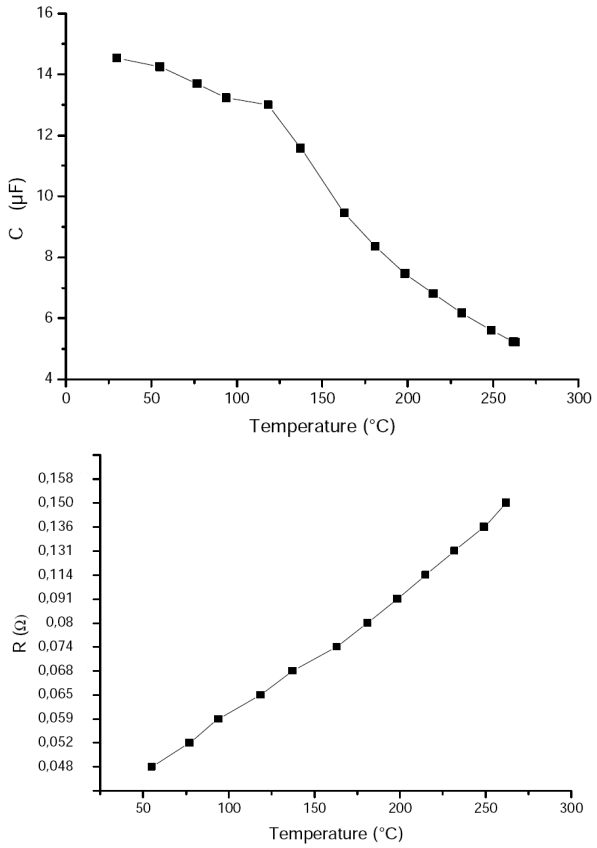


Fig. 6. Measured capacitor variation of capacitance and series resistance versus temperature

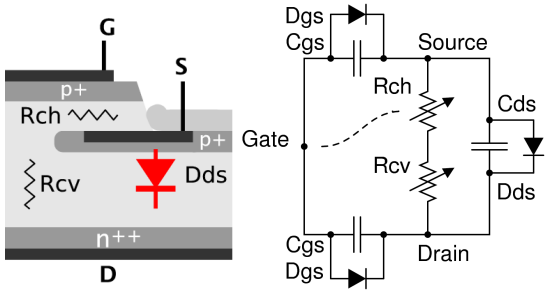


Fig. 7. SiC JFET simplified cross section and proposed model

1- a JFET channel directely controlled by the gate voltage named Rch, the horizontal part on the path.
2- a modulated resistor Rcv, to take into account the vertical section. At the time of writing the model parameters are 'guesses' of geometrical and physical properties of the SiCED JFET. The behaviour of the model is correct on a static point of view and needs further work for dynamic response. Nevertheless, the peak current at turn-On is modelled. Identification is now the next step to get a good matching of the model in order to compute switching losses and Electro-Magnetic-Compatibility spectrums. An experimental verification is shown on figure 9, the peak current presents no oscillations as does the simulated circuit, the shape is also

narrower. The simulation doesn't include circuit parasitics and inductance coupling, the voltage source is ideal in the modelled circuit.

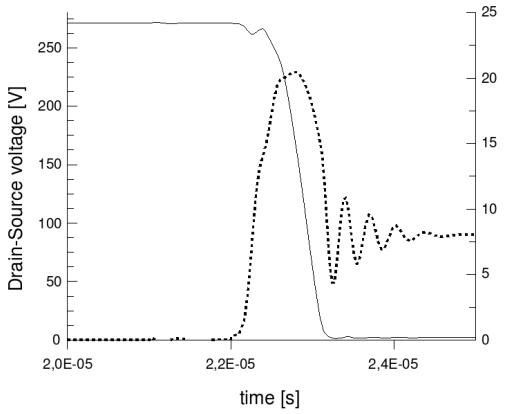


Fig. 8. Simulation of Turn-On voltage and current using the proposed model. V=270V, I=8A. Peak drain current phenomenom is visible

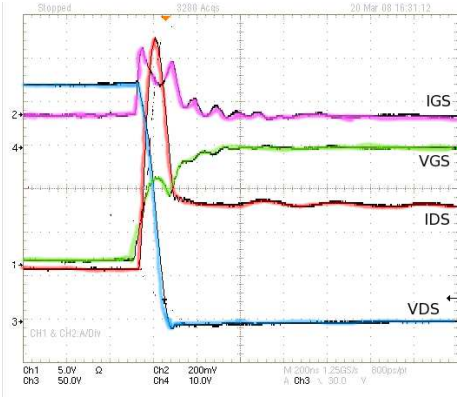


Fig. 9. Measurement at Turn-On. U=270V, I=8A. The experimental test bench is described in figure 5.

## IV. Converter expected performance

Using data from measured dynamic losses of table III and knowing RDSon temperature dependency, table II, it is possible plot the total losses per JFET chip, see figure 10. Cooling effort is estimated as a power density. It ranges from 300W/cm2 to 1500W/cm2 at 100W. Even with a common thermal resistance value such as 2K/W, the JFET chip temperature remains below maximun permissible temperature which is arround 600°C. Ambient maximum is 200°C, temperature rise is 200°C giving a maximum of 400°C. The principal limitation of performance is the package and the associated cooling system.

## V. Driver

Specific JFET Drivers are designed. They may be based on SOI integrated circuit to convert control logic signals into voltage gate signal, with adapted gate current. Each JFET should be driven by a separate SOI integrated circuit. A

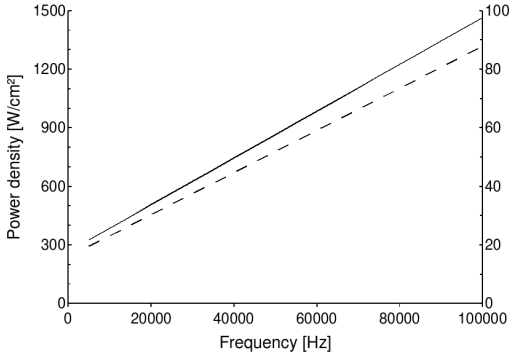


Fig. 10. Estimated total losses per JFET chip.
*Solid line : Required cooling power density [W/cm2], left axis.*
*Dotted line : Power losses, right axis [W]*

leg driver module includes two SOI ICs (upper and lower switches) and associated passive components.

*a) Specific Gate driver:* Specific JFET Drivers

Normally-On power switches are controlled using a gate driver. This subsystem receives a control signal to set the switches's state. The control signal is provided by the converter's controller. Figure 11 represents a gate driver including some kind of protection circuit sensing the Drain voltage. A logic core processes control and protection information. The Gate of a power JFET is biased by the output stage. It can be noted that a negative voltage is needed to set the JFET in the Off-state. Insulation is needed as power switches are connected to different high voltage sources. The Source reference is connected to the highest potential of output stage.

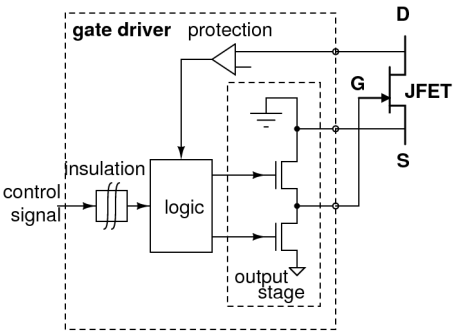


Fig. 11. JFET driver prototype bloc diagram

On a functional point of view, the same driver structure can drive both normally-On JFETs and normally-Off MOSFETs : a change of connection for the Source reference will suffice. Even the resistors used to adjust the turn-On and the turn-Off transients are placed in the same current loop. The difference will appear in the supply voltage of the output stage as gate threshold voltages differ between JFET and MOSFET. An extra positive voltage supply could be needed for sensing Drain voltage in the JFET driver.

*b) SOI for high temperature driver:* For high temperature operation, the use of transformers to insulate signal and supplies is a solution. For the semiconductors, Silicon-On-

Insulator technology enables operation of integrated circuit at 200°C. A SOI gate driver is proposed in figure 12, it uses two separate transformers, one for signal transmission, another for the power supply.

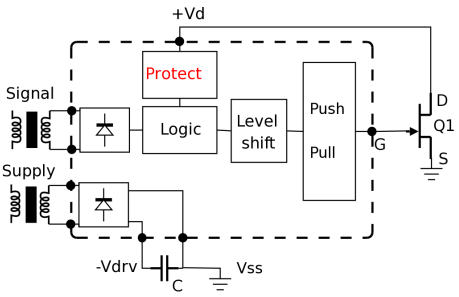


Fig. 12. Proposed SOI JFET gate driver bloc diagram

### A. Drivers requirements

*1) Requirements set by the JFET:* Static characterisation indicates a required voltage of -28V to turn the JFETs Off Dynamic measurements tell that a peak gate current of 0.5A is needed to switch the JFET with reduced losses; and that a measured 0.16W will be wasted for gate driving at 100kHz if the gate driver was loss-less. A value close to 0.18W, the charging/discharging power for the equivalent gate-source capacitor of 5nF under 27V at 100kHz. In this paper, the efficiency of the gate driver is not dealt with, but experimental knowledge indicates a power consumption of the gate driver in the 1 to 3W range. Most of the energy is lost in heavily-biased circuits for very fast switching operation.

*2) Requirements set by the environment:* Gate drivers provide specific added properties to power switches. In our case standard functions plus protection and safety circuits must be implemented as follow :

- Input signals level : 3.3 or 5 Volts.
- 600V or 1200 V DC bus rating.
- Galvanic Insulation for each leg power supply.
- Galvanic insulation between command and driver output signal.
- Interlock generation.
- Short pulse suppression.
- Overtemperature protection monitoring.
- Monitoring and protection of drivers supply voltage.
- DC bus monitoring.
- Saturation monitoring (Overcurrent and short-circuit).
- Off-state for all power components in the event of a default.
- Independent fault monitoring and independent inhibition for each leg.

## VI. Prototype

### A. Power side

A prototype is built using an hermetic Si3N4 module housing six JFET and a ceramic capacitor, assembled on a high temperature printed circuit board as presented on figure 13.


Fig. 13. Latest prototype. A 540VDC 15A three phase inverter operating at 200°C

## VII. Experimental verification

Experimental verification is needed at each step as reliable models are not available on the full operational range of the converter. The three phase inverter is tested at power levels exceeding required ratings (15A in stead-of 6A) in burst mode to reduce the cooling effort required at such levels of total losses. The RDSon on the samples we have used is still high 0.2Ω but much lower values are obtainable according to [10].

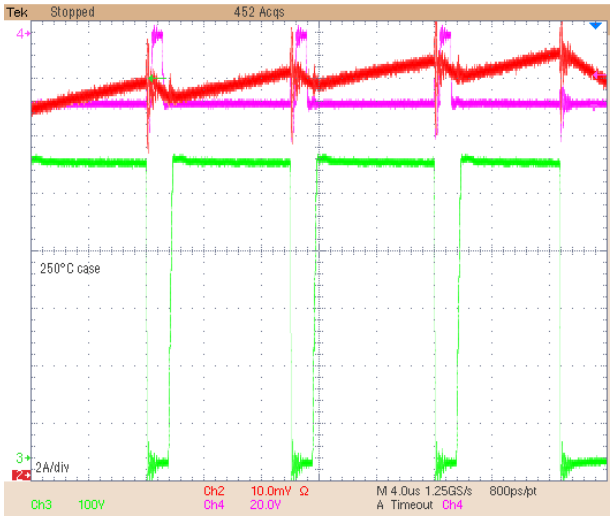


Fig. 14. Experimental verification of the inverter operation at 540VDC bus voltage, 15A peak output current, 250°C case temperature
Top purple trace : Gate voltage, Top red trace : Load current reaching 15A, Bottom green trace : JFET Drain-Source voltage. PWM frequency is 100 kHz.

## VIII. Conclusion

A three phase power module including inter-connections and capacitor is built and tested at 200°C, switching 15A under 540V. The limiting factor is the maximum obtainable cooling effort. Gate drivers for normally-On JFET are developped with standard techniques and a high temperature gate driver is under developement using either Silicon-On-Insulator integrated circuit or a discrete solution. Packaging and cooling are a main issue to be dealt with now.

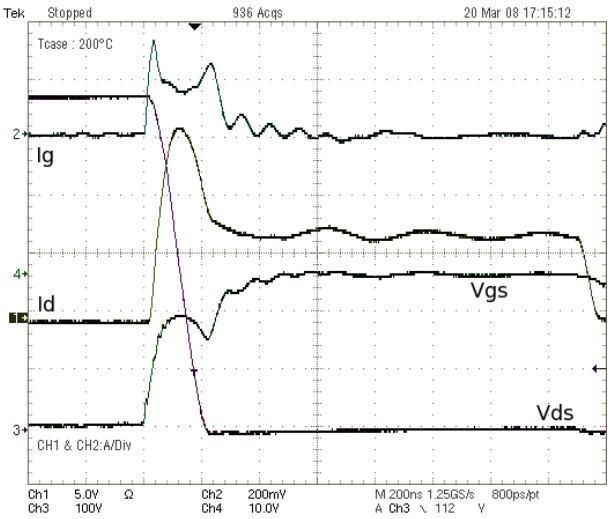


Fig. 15. Experimental verification. Zoom on the turn-On at 570VDC bus voltage, 8A switched current. Case temperature is 250°C
Labels show trace names at reference level (0V). Id : Drain current, Vds : Drain-Source voltage, Ig : Gate current, Vgs : Gate-Source voltage

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