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# Material and electrical characterization of TMS-based silicidation of the Cu-dielectric barrier interface for electromigration improvement of 65 nm interconnects

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The formation of a copper silicide interfacial layer by surface reaction in a plasma enhanced chemical vapour deposition (PECVD) system has been studied. Tri-methyl silane (TMS,  $\text{SiH}(\text{CH}_3)_3$ ) has been employed as the Si source as an alternative to more conventional silane ( $\text{SiH}_4$ ) approach. TMS precursor has been chosen due to improved control of Si penetration into the copper [S. Chhun, L.G. Gosset, N. Casanova, J.F. Guillaumond, P. Dumont-Girard, X. Fedespiel, R. Pantel, V. Arnal, L. Arnaud, J. Torres, *Microelectronic Engineering* 76 (2004) 106–112]. AFM, SIMS, light scattering, FT-IR spectroscopy and dielectric constant measurements were performed on various stacks to evaluate  $\text{CuSiN}$  formation. Resistance, leakage, and electromigration (EM) reliability characterization were performed on test structures based on 65 nm design rules. Nitridation step in silicidation process was shown to have positive impact on EM reliability, minimizing the line resistance increase.

*Keywords:*  $\text{CuSiN}$ ; Silicide; Electromigration; TMS

## 1. Introduction

The continuous dimensional scaling of interconnect technologies is associated with an increase of the signal propagation delay in the interconnects and a loss of intrinsic reliability. Indeed, for the latter, keeping the same current leads to higher current density through lines thus increasing electromigration phenomenon. The interface between copper and its overlying dielectric barrier becomes the primary contributor to EM degraded performances [2–4]. Cu interconnect reliability can be improved by engineering interface composition to reduce surface diffusion of Cu.

Surface treatments have been employed to modify interfaces in an effort to increase electromigration performances [5,6]. Copper silicide formation, obtained by means of a self-aligned process done prior to dielectric barrier deposition, has been demonstrated to enhance the EM lifetime [1]. In previous studies, silane has commonly been used as the silicon source for such a reaction. In this study, tri-methyl silane (TMS) based copper silicidation is evaluated as an alternative to the silane process [1]. Indeed, as TMS dissociation is more difficult to achieve due to the high energy of the carbon–silicon bond, less silicide is formed, limiting the resistance increase associated with the process [1].

In the current integrations, ultra low  $k$  (ULK) films are capped with a  $\text{SiO}_2$  layer to protect the ULK film from the

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patterning steps and to prevent the plasma damage that can occur during the treatment prior to SiCN dielectric barrier deposition [7]. Removal of this layer could provide further capacitance reduction, since the capacitance of interconnects increases in the presence of the SiO<sub>2</sub> layer. In this study, the impact of the silicidation process on the ULK surface has been characterized.

## 2. Experimental details

Silicide formation was considered as a pre-treatment to dielectric barrier deposition. All the process steps were performed in a standard PECVD chamber using 300 mm silicon substrates. The silicide formation was accomplished using a three-step approach [1], as illustrated in Fig. 1. After copper surface cleaning by CuO<sub>x</sub> reduction in a NH<sub>3</sub> based plasma, the silicide phase is formed by adsorption of the Si-based precursor, TMS (SiH(CH<sub>3</sub>)<sub>3</sub>) at the Cu grain surface and boundaries. A subsequent plasma-based nitridation step may follow to stabilize the compound by forming a CuSiN-like phase. Dilution conditions of the

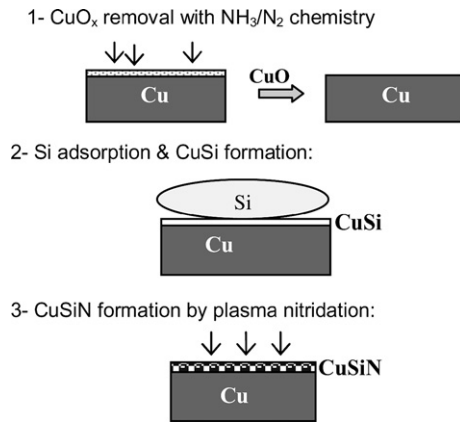


Fig. 1. CuSiN formation process [1].

Table 1  
Nitride dilution applied to the two tested process conditions

Nitridation process	NH <sub>3</sub> /N <sub>2</sub> proportion (%)
Pure NH <sub>3</sub>	100/0
NH <sub>3</sub> /N <sub>2</sub>	3/97

nitridation step were varied according to the values listed in Table 1. The process temperature was kept constant at 335 °C.

The film stacks used for the unpatterned Cu and ULK (porous SiOC:H  $k = 2.5$ ) substrates and C065 patterned wafers are shown in Fig. 2. The patterned stack has a typical 65 nm integration scheme with a SiOCH ( $k = 3.0$ ) interlayer dielectric. SIMS, AFM and light scattering measurements were performed following the CuSiN formation. Some of the samples were then capped with 30 nm of SiCN, for adhesion measurements using the four-point bending technique. FT-IR spectroscopy and dielectric constant measurements were performed following the silicidation process on the ULK surface. Patterned wafers with copper silicided interfaces were evaluated and compared to standard processed samples by means of electrical characterization and electromigration performance assessment at the package level under down-stream applied stress current.

## 3. Results and discussion

### 3.1. Unpatterned wafer characterization

Surface roughness was seen to increase during the silicidation process using both AFM and optical microscopy. These techniques illustrate the differences within wafer process uniformity. Light scattering effects or “haze” mapping provide a complete map of the relative surface roughness, as seen in Fig. 3. A correlation with local AFM measurements (10 × 10 μm box) was established. One AFM example of central roughness measurement is given in Fig. 3a, additional measurements have been done correlated to difference of roughness between center and edge as seen with light scattering technique. The main advantage of light scattering in this study was the quick information regarding the overall relative roughness of the wafer surface.

Results show that the silicidation obtained with TMS-based chemistry followed by pure NH<sub>3</sub> nitridation is non-uniform, with a rough surface in the center of the wafer. TMS chemistry followed by NH<sub>3</sub>/N<sub>2</sub> nitridation shows a more uniform surface, with lower global roughness.

Nevertheless, the SIMS depth profile in Fig. 4 shows the formation of a Cu<sub>x</sub>Si<sub>y</sub>C<sub>z</sub> O–N like layer at the copper’s top surface. The carbon-contamination originates from the use

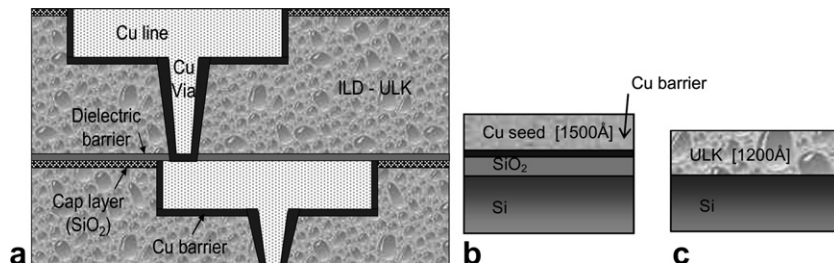


Fig. 2. Stack descriptions for (a) patterned and unpatterned wafers generated for experiment, (b) with Cu substrate and (c) ULK substrate.

of a TMS precursor. The relative thickness of the layer was observed to vary by a factor of 3 from the edge to the center with a lack of Cu detection at the wafer edge. The 3 nm thick layer observed in the center is believed to be sufficient to achieve EM enhancements with minimal copper consumption and therefore limited resistance impact.

Adhesion measurements were performed using a four-point bend technique, on samples with Si/TaN-Ta/Cu/SiCN stacks such as the one described in Fig. 5. Strain energy release rate ( $G$ ) results of several samples are presented in Table 2.

When silicidation is performed without any nitridation step, the adherence matches the reference value of strain energy release rate.

For the TMS process, whatever the silicide nitridation performed, results show a 30–50% lower adhesion compare to the reference process of a Cu-silicide treated interface without silicidation. However, when silicidation without the subsequent nitridation step is performed, the adhesion matches the reference value of strain energy release rate. The adhesion degradation with nitridation is likely associated with nitrogen and hydrogen penetration to the Cu/CuSi<sub>x</sub> interface. Follow-up analysis will be used to study potential SiN formation at the interface and process optimization to control the N penetration. Although previous studies [8] indicate adhesion improvement with CuSi<sub>x</sub> formation, no such improvement was seen here relative to the reference. However, it is important to note that the reference include an NH<sub>3</sub>-based plasma treatment already optimized for adhesion.

The dielectric constant ( $k$ ) measurements of the ULK substrate (Fig. 2c), including a standard reference, were performed using a mercury probe (see Table 3). Measurements were performed directly on ULK surface as capping SiO<sub>2</sub> layer removal is consider to provide global ILD capacitance reduction. All the processes strongly degrade  $k$ , especially the NH<sub>3</sub>/N<sub>2</sub> nitridation process. In this latter case, the surface leakage is so high that capacitance measurement is not able to provide any values. When the CuSiN pure NH<sub>3</sub> nitridation process is used, helium pre-

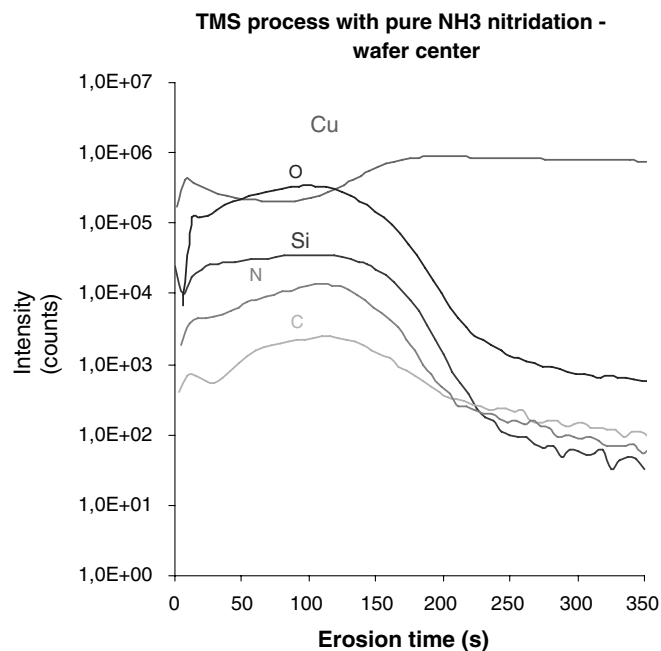


Fig. 4. SIMS profile of blanket wafer (Cu/CuSiN/SiO<sub>2</sub>).

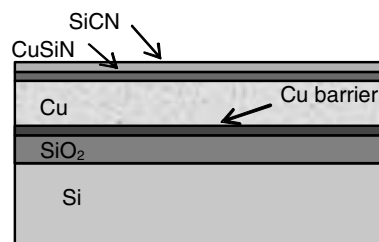


Fig. 5. Stack used for adhesion measurements.

treatment seems to limit the nitridation’s impact on the ULK surface.

Chemical bonding information was provided by FT-IR spectroscopy. The main change was observed for the 3000–3500 cm<sup>-1</sup> wavelength region as shown in Fig. 6. Indeed, intensity of Si–OH and H–OH links increases when

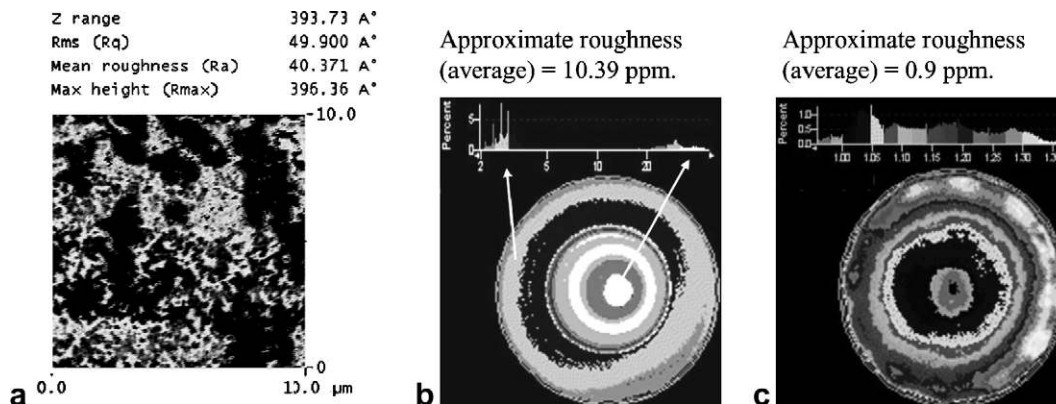


Fig. 3. (a) AFM surface roughness, (b) light scattering mapping, for TMS with pure NH<sub>3</sub> nitridation process and (c) light scattering mapping, for TMS with NH<sub>3</sub>/N<sub>2</sub> nitridation process.

Table 2  
Values of strain energy release rate  $G$  ( $J/m^2$ ) at Cu/cap interface; average wafer values

Treatment	TMS pure $NH_3$ nitridation + SiCN	TMS $NH_3/N_2$ nitridation + SiCN	(No CuSiN) standard $NH_3/N_2$ treatment + SiCN	TMS silicidation only + SiCN
$G$ ( $J/m^2$ )	17	13	26	23
Avg				
$G$ st. dev.	7	4	13	12

Table 3  
Treatments were applied on a ULK substrate

After treatment on ULK substrate	No treat.	CuSiN process with $NH_3/N_2$ nitridation	CuSiN process with pure $NH_3$ nitridation	He + CuSiN process with pure $NH_3$ nitridation
$k$ value at the center	2.44	Non-measurable (excessive surface leakage)	4.57	4.01

$k$  values were obtained using a Hg probe ( $S = 0.0214 \text{ cm}^2$ ).

CuSiN processes are applied. Nevertheless, there is a difference between CuSiN process with pure  $NH_3$  and with  $NH_3/N_2$  nitridation. After both processes, there is a transformation from a hydrophobic surface (standard ULK) to a hydrophilic one but with a higher susceptibility to moisture absorption in the case of CuSiN process with  $NH_3/N_2$  nitridation. He pre-treatment decreases the hydrophilic nature of the surface but is not sufficient to prevent a dielectric constant shift. The difference of peak intensity could be related to the nitridation plasma used during CuSiN formation.  $NH_3$  partial pressure is higher for pure  $NH_3$  nitridation. The content of  $NH_3$  (3%) provided during the  $NH_3/N_2$  nitridation might not be sufficient to inhibit the hydrophilic nature of the surface.

### 3.2. Electrical characterization of patterned wafers

Line resistance and current leakage values were evaluated (Fig. 7). The TMS process with pure  $NH_3$  nitridation considerably degrades the electrical performance of the circuit, by the formation of a leakage path along the upper

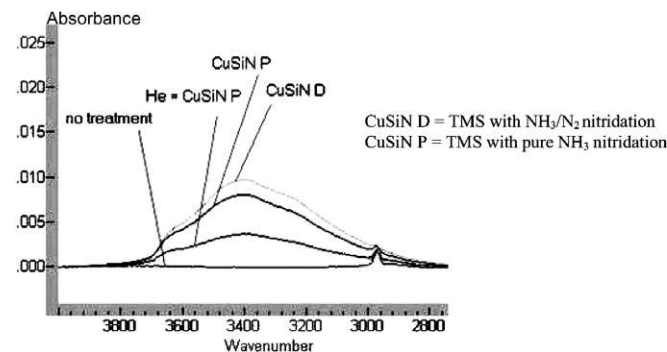


Fig. 6. FT-IR spectrum of all the conditions tested. Si-OH Peak [9].

dielectric surface. An example can be seen in TEM image of Fig. 8 in which a clear residue is observed on the dielectric surface at metal level where CuSiN has been formed. This effect is not visible at the other standard metal levels. Moreover, the edge-center effect observed on unpatterned physical characterizations has been confirmed by a wafer mapping of the chips, showing high leakage results in the center compared to the acceptable leakage results for the edge chips.

The TMS process with  $NH_3/N_2$  nitridation conserves the electrical properties of the interconnects. No improvements of these properties were expected as the CuSiN formed has higher resistivity compared to copper. Indeed, EM reliability demonstrates the potential improvement brought by the TMS-based silicidation plus  $NH_3/N_2$  nitridation compared to the standard SiCN deposition process: 40% longer failure times are observed, if one takes into account the late failures of each distribution only (standard, TMS-based, see Fig. 9). Other reports [10] have indicated MTF increase of two times with silicidation treatments. The more modest improvements described in this report may be attributable to a combination of the following: (a) structures using 65 nm node design rules have increased via sensitivity as compared to previously published results on 90 nm based structures thereby diminishing the surface treatment impact, and (b) silicidation treatment process designed to minimize resistance increase with tradeoffs to interface improvement.

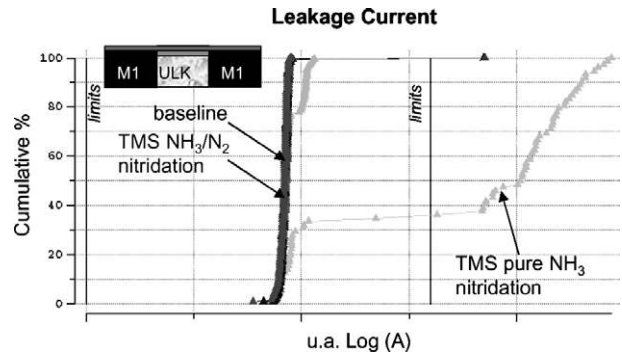


Fig. 7. Leakage current results. Y-axis is cumulative percentage.

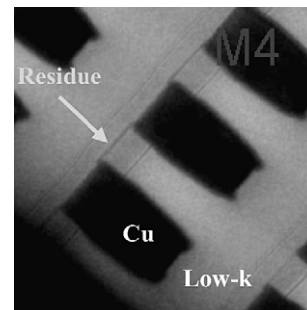


Fig. 8. TEM cross-section (Cu + CuSiN with pure  $NH_3$  nitridation) capped with 30 nm SiCN at metal 4.

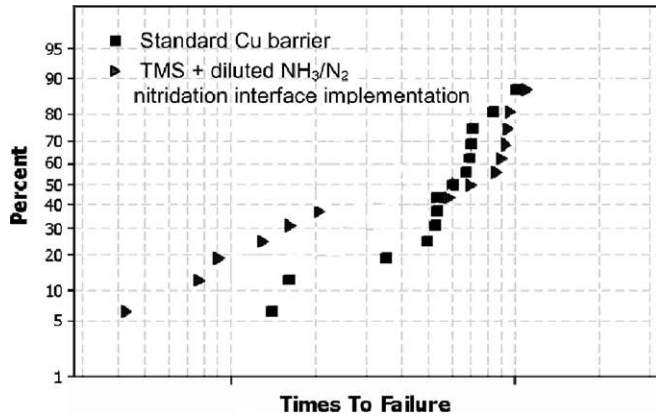


Fig. 9. EM cumulative time to failure distribution for wafers processed with silicidation and standard process.

The EM data points were collected for 0.10  $\mu\text{m}$  wide lines tested at package level under accelerated conditions corresponding to a temperature of 300  $^{\circ}\text{C}$  and a current density of 1.5  $\text{MA}/\text{cm}^2$ . The failure criterion was set to 10% of the resistance increase. The early failures were associated with void excursions in the Cu metallization. It is important to note that although comparable adhesion was observed for the two splits, MTF showed a difference. This calls into question the proposed correlation between MTF and adhesion put forth by Lloyd [6]. However it is important to note that the accuracy of the four-point bend test is limited in the extreme of “good” adhesion ( $>20 \text{ J}/\text{m}^2$ ) due to a mixture of interfacial failure modes and fracture in the epoxy.

#### 4. Conclusion

A process optimization has been completed to improve the copper dielectric interface by forming of a CuSiN layer

between copper and dielectric. This layer is a TMS-based copper silicidation providing the advantages of improved process control and Si depth penetration as compared to standard silane sources [1]. The nitridation step was identified as a key predictor of electrical performance, since pure  $\text{NH}_3$ -based nitridation leads to leakage pathways on the dielectric surface. Furthermore, an optimized regime was identified on patterned structures to minimize the impact on line resistance and current leakage while achieving the first improvement in terms of electromigration robustness. However, plasma treatment studies performed on ULK films have shown deterioration of the material integrity. Multi-step plasma treatments are required to create a protective skin on the ULK prior to the CuSiN treatment, in order to achieve the electromigration benefits without a capacitance increase.

#### References

- [1] S. Chhun, L.G. Gosset, N. Casanova, J.F. Guillaumond, P. Dumont-Girard, X. Fedespiel, R. Pantel, V. Arnal, L. Arnaud, J. Torres, *Microelectron. Eng.* 76 (2004) 106–112.
- [2] X. Lu, J.W. Pyun, B. Li, N. Henis, K. Neuman, K. Pfeifer, P.S. Ho, *Proceedings of the IITC (2005)* 33–35.
- [3] B. Li, T.D. Sullivan, T.C. Lee, D. Badami, *Microelectron. Reliab.* 44 (2004) 365–380.
- [4] K.N. Tu, *J. Appl. Phys.* 94–99 (2003) 5451–5473.
- [5] M. Hatano, T. Usui, Y. Shimooka, H. Kaneko, *Proceedings of the IITC (2002)* 212–214.
- [6] J. Lloyd, *Proceeding of the 2002 International Integrated Reliability Workshop, October 21–24, 2002.*
- [7] A. Humbert, L. Mage, C. Golberg, K. Junker, L. Proenca, J.B. Lhuillier, *Microelectron. Eng.* 82 (2005) 399–404.
- [8] D.S. Armbrust et al., *IBM United States Patent no. US 6, 818, 992 B1*, November 16, 2004.
- [9] C. Rau, W. Kulisch, *Thin solid Films* 249 (1994) 28–37.
- [10] P. Dumont-Girard, L.G. Gosset, S. Chhun, M. Juhel, V. Girault, *Proceedings of the IITC (2005)* 132–134.