

Automatic extraction methodology for accurate measurement of effective channel length on 65nm MOSFET technology and below

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Outline

- ◆ Problematic of accurate L_{eff} extraction
- ◆ State-of-the-art
- ◆ Methodology for automatic extraction
- ◆ Test structure design for automatic extraction
- ◆ Results and validation
- ◆ Conclusion

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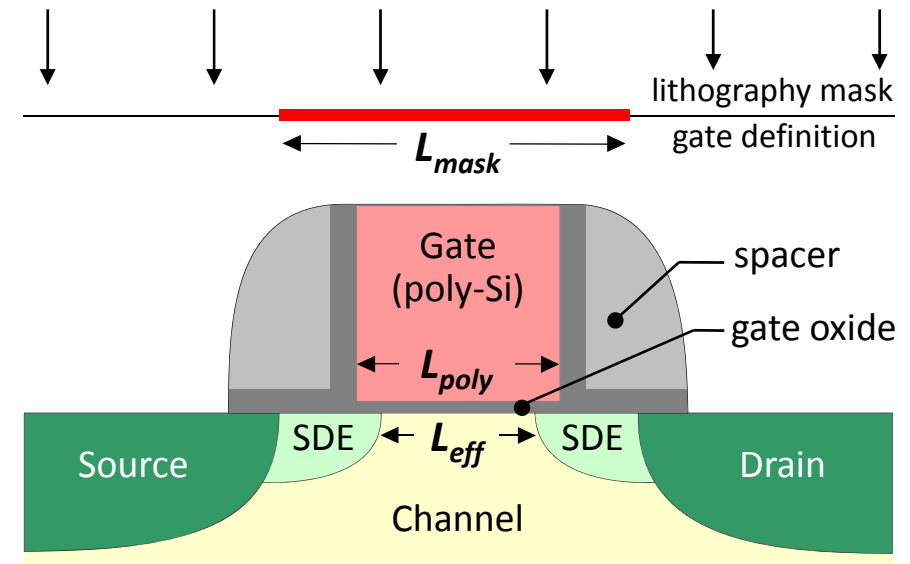
Problematic of accurate L_{eff} extraction

- ◆ The mask length (L_{mask}): gate definition from lithography mask
- ◆ The effective channel length (L_{eff}): defined by the inversion layer length
- ◆ $\Delta L = L_{mask} - L_{eff}$ is the channel length reduction

Nowadays, L_{eff} hardly reaches 50% of L_{mask}



A few nanometer change can induce bad results interpretation !



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State-of-the-art

- ◆ Most of $I_D(V_G)$ -based methods assume invariance of the mobility with the length of transistors.

Mistaken approach due to low field mobility degradation observed on short devices [1], [2]

- ◆ Capacitive method provides L_{eff} extraction without any assumption towards the mobility.



Solution avoiding a mistaken extraction

[1] K.Romanjek, Solid State Elec., vol. 49, pp. 721-726, 2005

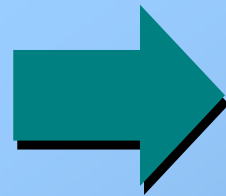
[2] A.Cros, IEDM'06, San Francisco USA, dec. 2006, pp. 663-666

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Methodology: experimental setup

- ◆ Capacitance measurements are performed:
 - On fully automatic prober with probecard (Accretech UF3000)
 - Using high precision LCR-meter (HP4984 LCR-meter)
 - Using a connection matrix (Agilent 4073B)
- ◆ Extractions are performed thanks to a home-developed software (Scilab™)



- Test of several pad combinations
- Large samplings (>20 dice/wafer)
- Batch extractions

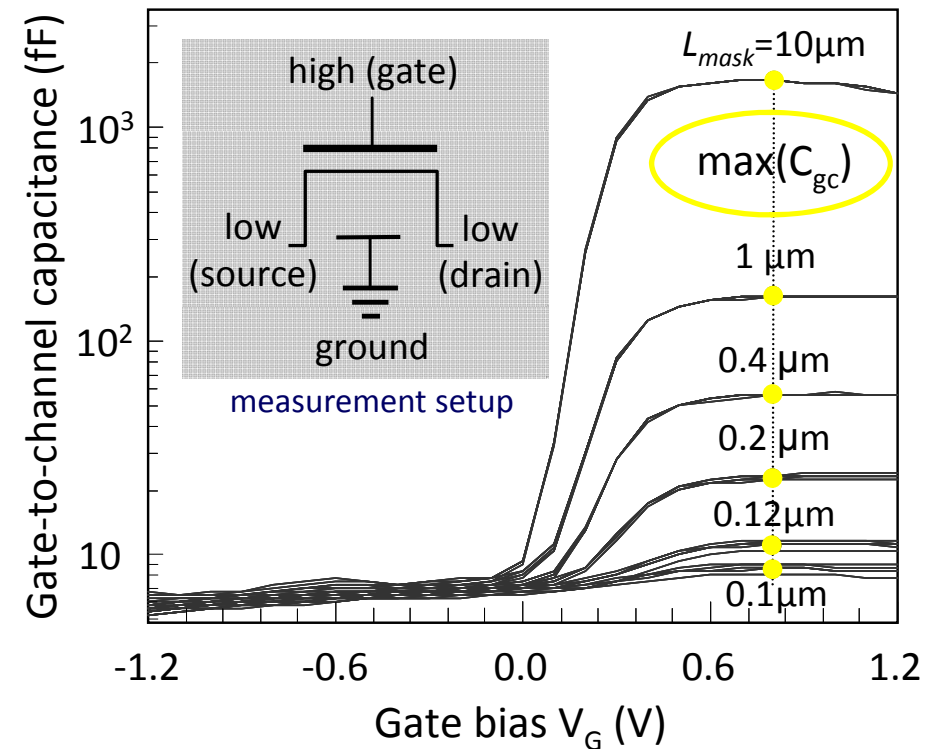
Methodology: capacitive method

- ◆ L_{eff} is extracted from gate-to-channel measurements $C_{gc}(V_G)$
 - Proportional to the channel area

$$C_{gc} \propto W \times L_{eff}$$

- $\max(C_{gc})$ is set as a reference point for each curve.

No de-embedding structure needed to get rid of parasitic capacitances



Methodology: L_{eff} extractions

- ◆ Two ways of extraction are possible:

L_{eff} extraction

Assume ΔL
constant

ΔL extracted from an
axis intercept

Extract
 $\Delta L(L_{mask})$

ΔL extracted from a
cross product

Recall : $\Delta L = L_{mask} - L_{eff}$

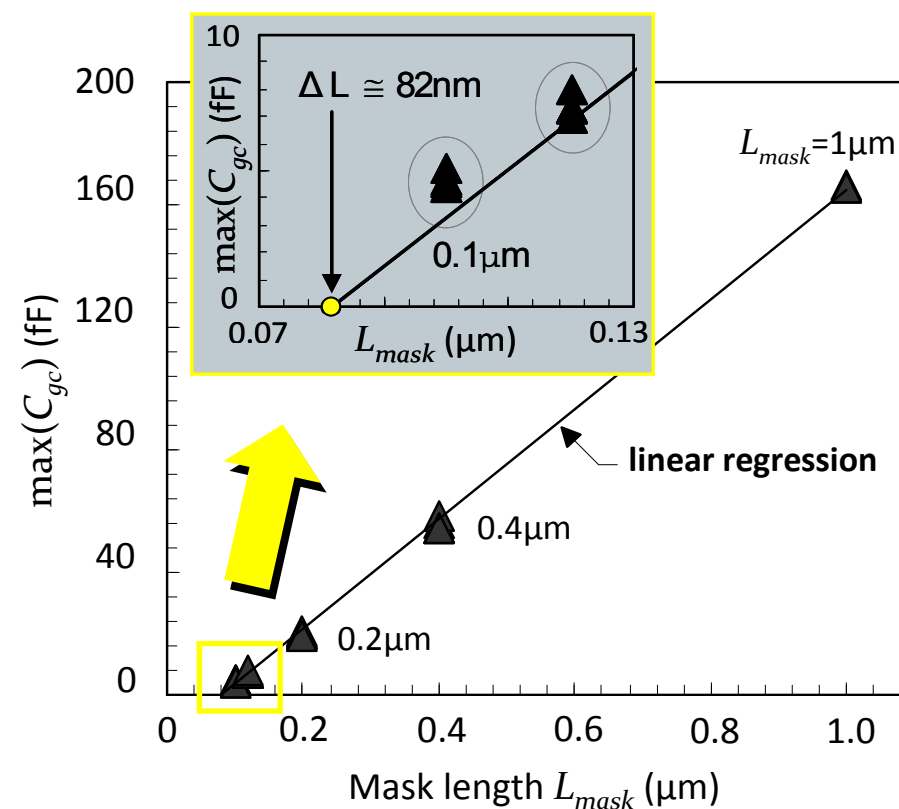
Methodology: constant ΔL method

- ◆ ΔL is assumed invariant with L_{mask} , thus:

- $C_{gc} = W \cdot C_{ox} (L_{mask} - \Delta L)$

- ΔL is extracted from the linear regression: $\max(C_{gc}) = f(L_{mask})$

L_{eff} error strongly depends on ΔL linearity assumption. (lithography and gate etch processes optimization) ⚠



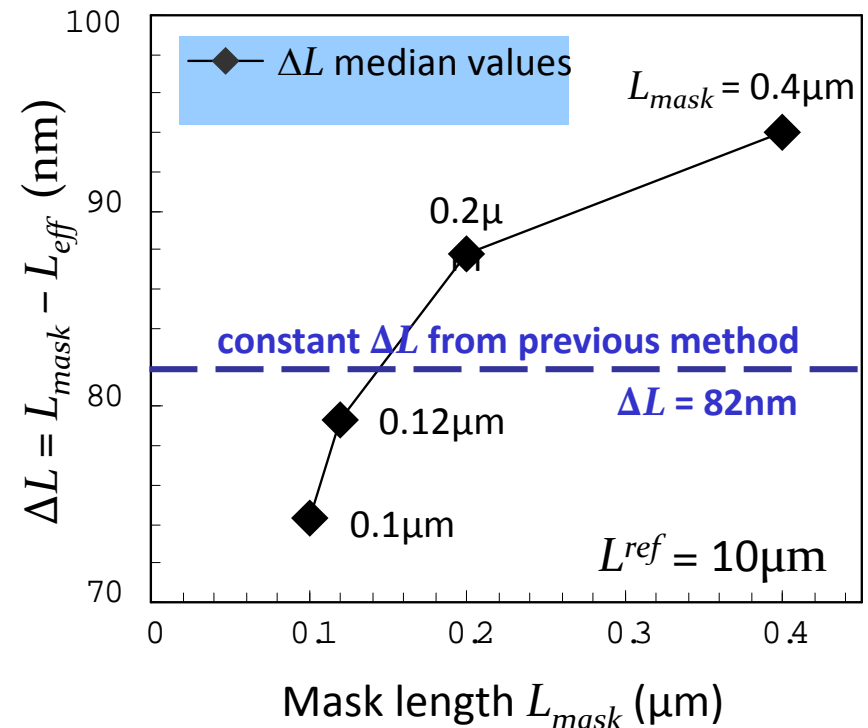
Methodology: individual ΔL method

◆ Extraction of individual ΔL^* (for each transistor)

- ΔL are extracted from a proportionality rule:

$$\Delta L^* = L_{mask}^* \underbrace{\left(\frac{L_{eff}^{ref}}{\max(C_{gc}^{ref})} \times \frac{\max(C_{gc}^*)}{\max(C_{gc}^{ref})} \right)}_{=L_{eff}^*}$$

- The longest transistor is set as the reference ($L_{eff} \cong L_{mask}$)
- The constant ΔL is almost the average value of $\Delta L(L_{mask})$



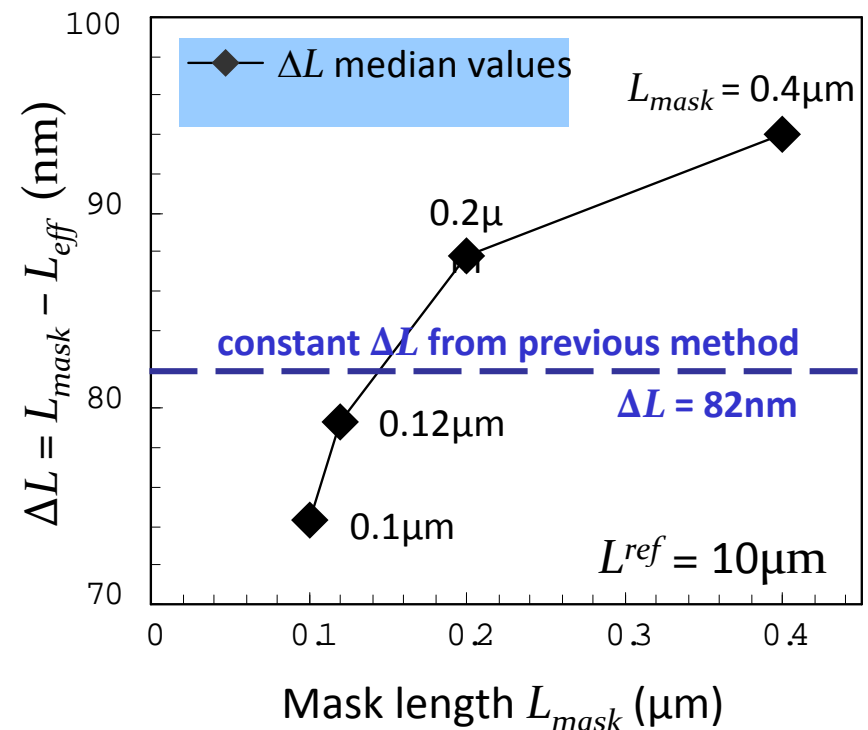
Methodology: individual ΔL method

- ◆ Extraction of individual ΔL^* (for each transistor)
 - ΔL are extracted from a proportionality rule:

$$\Delta L^* = L_{mask}^* - \underbrace{L_{eff}^{ref} \times \frac{\max(C_{gc}^*)}{\max(C_{gc}^{ref})}}_{=L_{eff}^*}$$

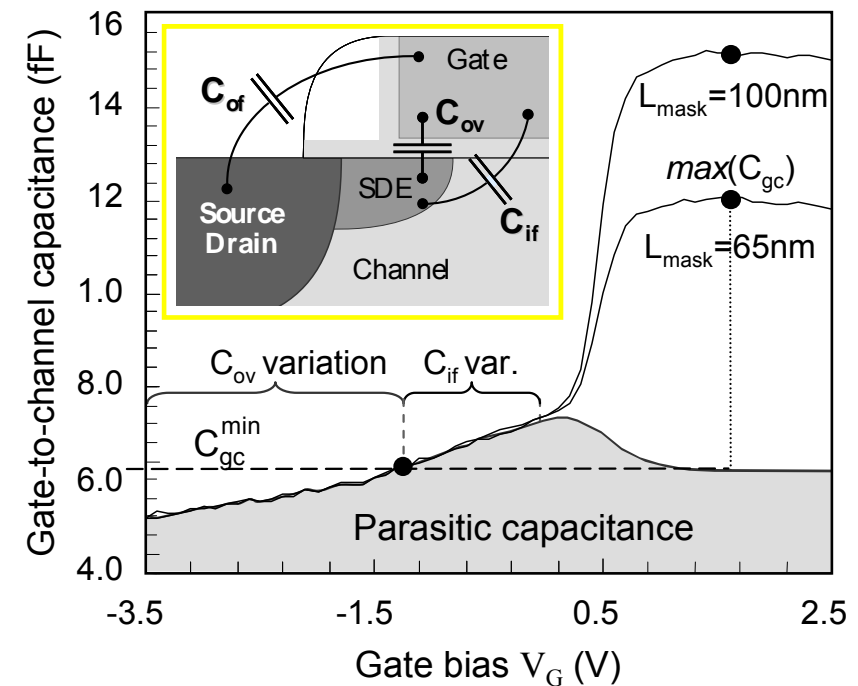
Allows studying $\Delta L(L_{mask})$ behavior

Needs a long transistor as reference



Methodology: parasitic capacitance

- ◆ C_{gc} measurements are impacted by parasitic capacitance
 - From cabling, probes and connection pads (constant term)
 - Inherent to the MOSFET architecture
 - Overlap capacitance C_{ov} (V_G -dependent)
 - Inner fringe capacitance C_{if} (V_G -dependent)
 - Outer fringe capacitance C_{of}
 - C_{gc}^{min} is chosen to have the same value than parasitic capacitances include into $\max(C_{gc})$ [3].

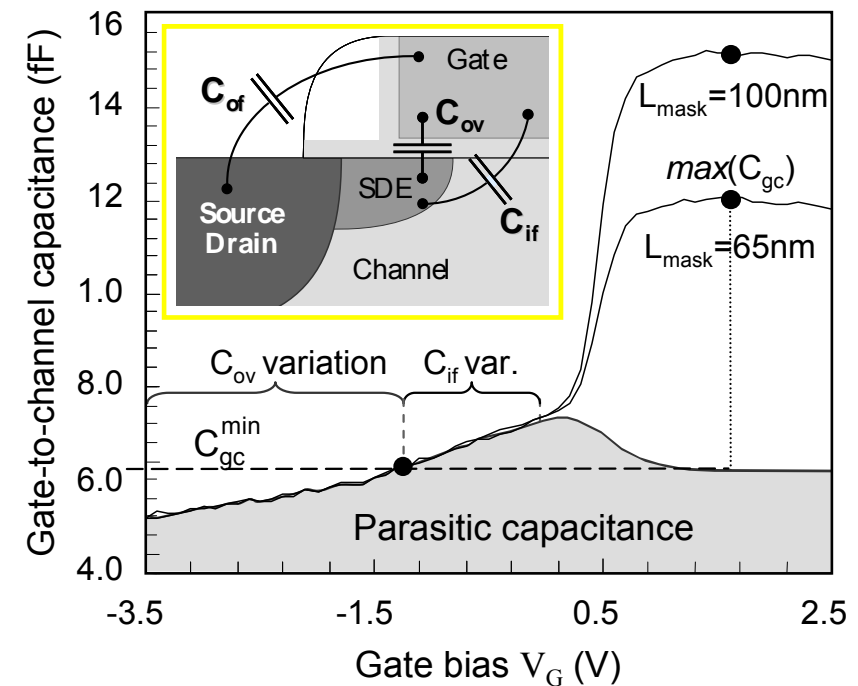


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Use of $\Delta C = \max(C_{gc}) - C^{min}$
instead of $\max(C_{gc})$
⇒ cancel parasitic capacitances

approximation on C^{min}
⇒ error less than 3% on L_{eff}

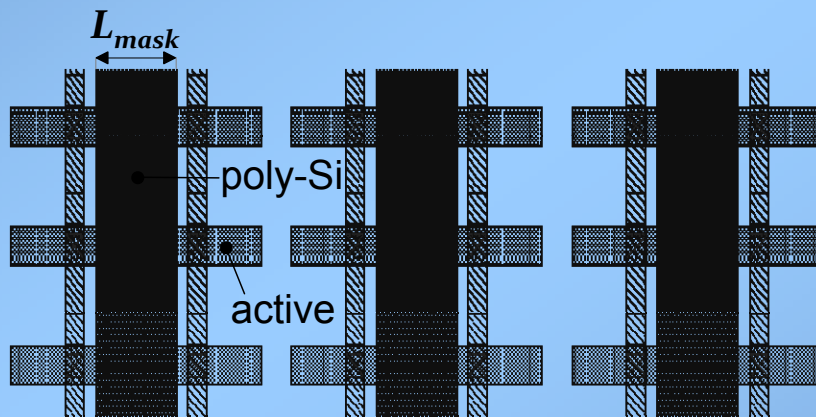


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Test structures

- ◆ Requirements of the measurement setup
 - Connection matrix: areas above $50\mu\text{m}^2$ to provide enough signal-to-noise ratio
- ↓
- **Use of array test structures** composed by N identical transistors wired together (area $\approx 100\mu\text{m}^2$)



Such large areas can not be measured on leaky devices ($T_{ox} < 15\text{\AA}$) !

Test structures: leaky devices

$$T_{ox} > 15\text{\AA}$$

array test structures
 $A \approx 100\mu\text{m}^2$



matrix connection
between LCR-meter
and devices
2-3min/curve

$$T_{ox} < 15\text{\AA}$$

isolated test structures
 $A = L \times W < 10\mu\text{m}^2$



direct connection of
LCR-meter to devices
20min/curve

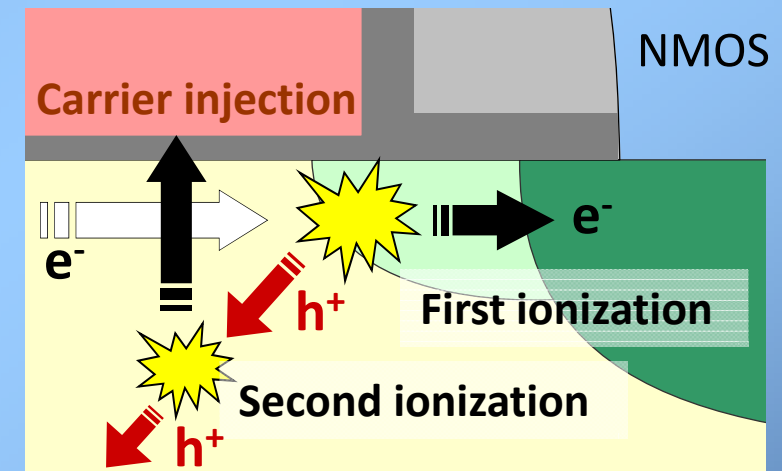
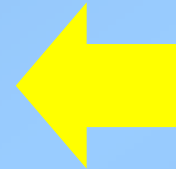
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Results and validation: HCI lifetime

◆ Hot Carrier Injection mechanism:

Bulk current
 I_b and I_b/I_d ratio
are increased



◆ HCI strongly depends on L_{eff} :

- When L_{eff} decreases the lateral electric field increases ($E \propto 1/L_{eff}$)
- Carriers get high kinetic energy thanks to the high field \Rightarrow **hot carriers**

L_{eff} must be measured with accuracy to identify the origin of HCI lifetime degradation

Results and validation: HCI lifetime

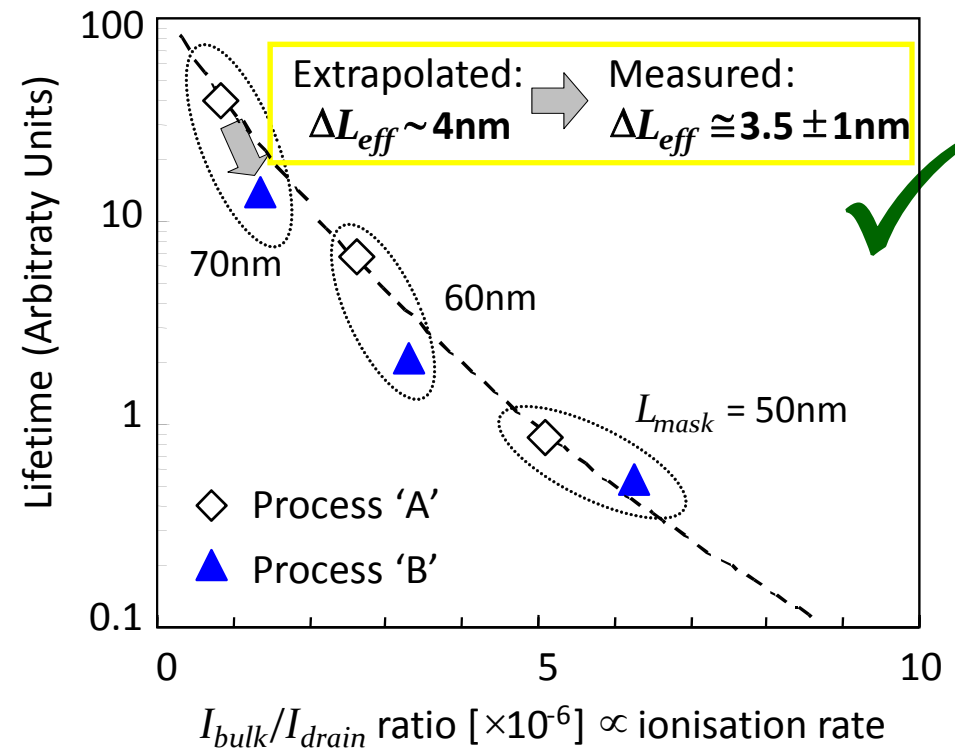
- ◆ L_{eff} measurements to understand HCI lifetime results:

Thick oxide ($T_{ox} \cong 18.5\text{\AA}$)
 \Rightarrow array test structures

Statistical measurements
 20 dies

HCI-lifetime study predicts 4nm-
 shift on L_{eff} between 'A' and 'B'

L_{eff} measurements give 3.5 ± 1 nm



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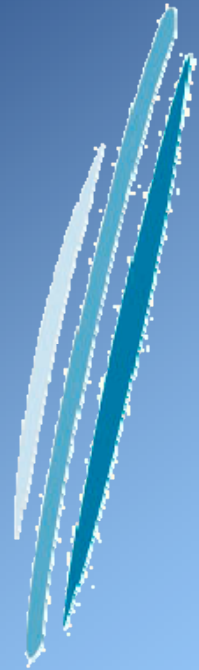
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Conclusion

- ◆ High capabilities of our industrially-adapted L_{eff} extraction
 - Outstanding accuracy ($\pm 1\text{nm}$)
 - Unequal benefits toward HCI lifetime and mobility studies
- ◆ Test structure improvement
 - Systematic measurements thanks to new array test structures
 - Reduction of the measurement time (20min \Rightarrow 2min)

Expected method improvements:

- Extend L_{eff} meas. to in line monitoring
- In-depth study of parasitic capacitances



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