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# Reliable Self-Stabilizing Communication for Quasi Rendezvous

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## Abstract

The paper presents three self-stabilizing protocols for basic fair and reliable link communication primitives. We assume a link-register communication model under read/write atomicity, where every process can read from but cannot write into its neighbours' registers. The first primitive guarantees that any process writes a new value in its register(s) only after all its neighbours have read the previous value, whatever the initial scheduling of processes' actions. The second primitive implements a “weak rendezvous” communication mechanism by using an alternating bit protocol: whenever a process consecutively writes  $n$  values (possibly the same ones) in a register, each neighbour is guaranteed to read each value from the register at least once. On the basis of the previous protocol, the third primitive implements a “quasi rendezvous”: in words, this primitive ensures furthermore that there exists exactly one reading between two writing operations

All protocols are self-stabilizing and run in asynchronous arbitrary networks. The goal of the paper is in handling each primitive by a separate procedure, which can be used as a “black box” in more involved self-stabilizing protocols.

*Keywords:* Self-stabilization, communication primitive, rendezvous, read/write atomicity, liveness

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# 1 Introduction

A *self-stabilizing* system which is started from an arbitrary initial configuration, regains its consistency and demonstrates legal behaviour by itself, without any outside intervention. Consequently, a self-stabilizing system needs not be initiated to any configuration, and can recover from *transient faults*. More precisely, it can recover from *memory corruptions* and copes with processors or channels crashes and recoverings (i.e., dynamic networks).

## 1.1 The Communication primitives

In the paper, we present fair and reliable self-stabilizing communication primitives in the link-register model. The communication between two neighbours ( $A$  and  $B$ ) is carried out by the use of two sets of *communication registers* called *registers*:  $r_{AB}$  and  $r_{BA}$ . Process  $A$  can write in the registers of  $r_{AB}$  and each process  $A$  and  $B$  can read from the registers of  $r_{AB}$ . The registers support *read* and *write* atomic operations. For example, let  $\Sigma = \{a, b, c, \epsilon\}$  be an alphabet and  $w = aaabbbbcc = a^3b^4c^2$  a sequence of values written by  $A$  into  $r_{AB}$ . The communication primitives in their very first basic form *do not ensure more* than e.g.:  $a^*b^*c^*$  is eventually read by  $B$ .

The first presented primitive guarantees that any process  $A$  writes a new value in its register(s)  $Write_{AB}$  only after its neighbour  $B$  has read the previous value. Notice that when  $A$  writes  $n$  times the same value consecutively in the register  $Write_{AB}$ , the primitive ensures that  $B$  eventually copies this value at least once. For example, given  $\Sigma$  and  $w$  as above, the first primitive *only guarantees* that e.g.,  $aa^*bb^*cc^*$  is eventually read by each neighbour: each symbol in  $w$ , ( $a$ ,  $b$  and  $c$ ) is read at least once, whatever the number of occurrences. This primitive simulates self-stabilizing reliable message-passing communication in the link-register asynchronous model. It guarantees that a message, that is the value of the register  $Write$ , is eventually received: the value is eventually known from the neighbours' process.

The *rendezvous* mechanism (as defined in [16]) synchronizes communications, i.e., the *write* and *read* operations are performed in and from the same register. When Process  $A$  writes a value in its register  $Write_{AB}$ , it cannot perform any other action until process  $B$  has completed a *read* operation from the register  $Write_{AB}$ .

The second communication primitive is a self-stabilizing “weak rendezvous”. After performing a *write* operation in its register  $Write_{AB}$ , the process  $A$  cannot perform but some specific actions, as long as process  $B$  has not completed a *read* operation from  $Write_{AB}$ . Therefore, if  $A$  consecutively writes  $n$  values (possibly the same ones) in the register  $Write_{AB}$ , the primitive guarantees that  $B$  eventually

copies each value at least once. If  $A$  writes  $n$  times the same value in  $Write_{AB}$ , the value will be read at least  $n$  times. As an example, given  $\Sigma$  and  $w$  as above, the second primitive *at least guarantees* that e.g.,  $a^3a^*b^4b^*c^2c^*$  is eventually read by each neighbour: each symbol in  $w$  ( $a$ ,  $b$  and  $c$ ) is read at least the number of times the symbol occurs in  $w$  (but any symbol may be read strictly more than its number of occurrences).

The third self-stabilizing communication primitive performs a quasi synchronization. It is a “quasi rendezvous” mechanism and requires that between two *write* operations performed by the process  $A$  in  $Write_{AB}$ , the process  $B$  cannot perform but one and only one *read* operation from  $Write_{AB}$ . Therefore, if  $A$  writes  $n$  consecutive times the same value (possibly the same one in each row) in the register  $Write_{AB}$ , the primitive guarantees that  $B$  will copie each of the  $n$  values exactly one time, once the system is stabilized. For example, given again  $\Sigma$  and  $w$  as above, the third primitive *does ensures* that *exactly*  $a^3b^4c^2$  is eventually read by each neighbour: each symbol in  $w$  ( $a$ ,  $b$  and  $c$ ) is read exactly the number of times it occurs in  $w$ .

Each such primitive may prove useful as a communication “black box” in designing more involved distributed self-stabilizing protocols.

## 1.2 Related Works and Results

A deterministic self-stabilizing “balance-unbalance” mechanism on two processes systems under read/write atomicity is presented in [12] and in [13]. The two processes are not executing the same code. The one executes the balance code: when both processes have the same color, it changes color. The other executes the unbalance code: when both processes have not the same color, it changes color. In [12], this mechanism is used to guarantee that each process has a mutual exclusion access to a critical section, and in [13], it is used to ensure synchronization of the processes. In both cases, this mechanism provides strong synchronization: between two “actions” of a process, the other process cannot perform but only one “action”. In [12, 13], the two processes protocol is used to design a mutual exclusion algorithm (global synchronization) on tree networks. As claimed in [12, 13], the balance-unbalance mechanism cannot be extended to any network topology, since there exist no deterministic self-stabilizing synchronization protocols in uniform arbitrary networks. On the other hand, a self-stabilizing synchronization on unidirectional rings is provided in [10] through the deterministic token circulation mechanism: between two actions of a process its neighbours cannot perform but only one action.

Any self-stabilizing reset protocol [5, 2, 8] can be combined with the protocol in [6] to design a self-stabilizing synchronizer. General self-stabilizing synchroniz-

ers are presented e.g. in [9, 7, 19]. Global self-stabilizing synchronizers for tree networks are also proposed in [13, 3, 11]. A self-stabilizing local synchronizer, that synchronizes each node in a tree network with its neighbours is presented in [18]. In the recent literature, several communication problems in the message-passing model have been addressed. A self-stabilizing communication protocol for two-way handshake is presented in [15], and a self-stabilizing version of the alternating-bit protocol is given in [1]. In [4], Anagnostou and Hadzilacos present a self-stabilizing data link protocol under the read/write atomicity model such that, between two *write* operations in the register, only one *read* operation from that register is performed. However, no proof of the protocol is given in their paper. By contrast, our last two primitives use the alternating-bit mechanism, and since the two bits values must begin with the same value 0, our algorithm in section 7 is twice as fast as in [4].

Section 2 describes our model with the basic assumptions. In Section 3, we present the general principle of our solution for a two processes system. The generalization to  $n$  processes in arbitrary networks yields the *Read Checking* self-stabilizing protocol, which is presented in Section 4. Section 5 is devoted to the proof of liveness and correctness of the Read Checking protocol. Section 6 presents the weak rendezvous protocol and Section 7 describes our quasi rendezvous protocol. Finally, the paper ends with few concluding remarks.

## 2 Model and Requirements

Although distinct from the one described in [12], our model relies on close requirements and assumptions, especially in terms of communication (e.g., link registers, read/write atomicity, etc.). A distributed system consists of  $n$  processes denoted  $A$ ,  $B$ , etc. Each process resides on a node of the system's *communication graph* (or *network*). Two processes which reside on two adjacent nodes of the network are called *neighbours*. We model distributed self-stabilizing systems as a set of (possibly infinite) state machines called processes. Each process can only communicate with the subset of processes consisting of its neighbours. We assume a *link-register* communication model under read/write atomicity [12]. Each link between any two neighbours  $A$  and  $B$  is composed of two pairs of registers<sup>1</sup>, denoted  $(Write_{AB}, Read_{AB})$  and  $(Write_{BA}, Read_{BA})$ , and belonging to  $A$  and  $B$ , respectively. Process  $A$  can read from the two registers of  $B$ ,  $Write_{BA}$  and  $Read_{BA}$ , but cannot write into them. Similarly, process  $A$  cannot write but in its own registers,  $Write_{AB}$  and  $Read_{AB}$ , to communicate with  $B$ .

---

<sup>1</sup>In our model, the registers are physical (hardware) devices. Reading from or writing in *one* register is an atomic action according to the design of the microprocessor.

A *configuration* of the system is the vector of states of all processes. The state of a process is the value of its internal variables and the contents of its registers.

## 2.1 Schedulers, Demons and Computation

An *atomic step* is the “largest” step which is guaranteed to be executed uninterruptedly. A process uses *read/write* atomicity if each atomic step contains either a single read operation or a single write operation but not both. The system behaviour is modelled by the interleaving model in which processes are activated by a scheduler. The scheduler is regarded as a *fair* adversary: in a self-stabilizing system, all possible fair executions are required to converge to a correct behaviour. A fair scheduler shall eventually activate any process which may continuously perform an action. A common scheduler activates either processes one by one (central demon) or subsets of processes (distributed demon). Under read/write atomicity, both central and distributed schedulers/demons are “equivalent”, in the sense that any execution performed under a distributed scheduler may be simulated by a central one. A process which can perform an atomic step into a configuration  $c$ , is said to be *enabled* at  $c$ . During a *computation step*, one or more processes execute an atomic step. A *computation* of a protocol  $\mathcal{P}$  is a sequence of configurations  $c_1, c_2, \dots$  such that, for  $i = 1, 2, \dots$ , the configuration  $c_{i+1}$  is reached from  $c_i$  by one computation step. A computation is said to be *maximal* either if the sequence is infinite, or if it is finite and no process is enabled in the final configuration. A *problem* is a predicate defined on computations.

## 2.2 Self-Stabilization

The protocol  $\mathcal{P}$  is *self-stabilizing* for the problem  $\Pi$  if and only if there exists a predicate  $\mathcal{L}$  defined on configurations such that:

- all computations reach a configuration that satisfies  $\mathcal{L}$  (**convergence**);
- all computations, from  $\mathcal{L}$ , satisfy problem  $\Pi$  (**correctness**).

Notice that the maximal computations of a self-stabilizing protocol may be finite; in that case the algorithm is said to be *silent* [14]. Most self-stabilizing algorithms which build spanning tree or elect a leader are silent [17]. Self-stabilizing protocols offers full and automatic protection against all transient process failures, no matter how much the data have been corrupted: e.g., all registers values may be fully corrupted.

So, whatever the registers values, our protocols secure the transfer of information between any two pair of neighbours after a “certain delay time”.

### 3 Principle of the Solution

Let a two processes system, consisting in two neighbouring processes  $A$  and  $B$  equipped with their two pairs of registers (see Section 2). The principle of the solution for  $A$  relies on the following basic idea. Under read/write atomicity,  $A$  systematically keeps reading the value from  $Write_{BA}$  and copies out this value in  $Read_{AB}$  (i.e.,  $A$  reads the message sent by  $B$  and copies out the message in  $Read_{AB}$  to inform  $B$  that its message is received). Besides,  $A$  systematically keeps reading the value from  $Read_{BA}$  and compares it to the value of  $Write_{AB}$ . When both values are equal,  $A$  finds out that  $B$  somehow read that value (i.e., the information has been transmitted), So it can stop reading and can write again in  $Write_{AB}$ .

---

```
while true do
     $A$  writes in  $Write_{AB}$ 
repeat
     $A$  reads from  $Write_{BA}$  ;
     $A$  writes out the value of  $Write_{BA}$  into  $Read_{AB}$  ;
     $A$  reads from  $Read_{BA}$ 
until  $Read_{BA} = Write_{AB}$ 
endwhile
```

**Fig. 1.** *The basic 2-processes protocol for A.*

---

After  $A$  has written a new value in  $Write_{AB}$ ,  $A$  becomes “weakly locked” until  $B$  receives the message ( $Read_{BA} = Write_{AB}$ ). When  $A$  is inside the **repeat** loop, it can only perform some actions, for instance,  $A$  cannot write in its register  $Write_{AB}$ .

In a self-stabilizing setting,  $A$  may then proceed with the execution of its own code, since the protocol makes it sure that  $B$  did read the value from  $Write_{AB}$  (at least, it results from the protocol that  $A$  knows for sure that the values in  $Read_{BA}$  and  $Write_{AB}$  are identical). The corresponding code sequence for  $B$  is of course fully symmetrical to the basic protocol for  $A$ : the roles of  $A$  and  $B$  (i.e. the registers’ names) have simply to be inverted within the above protocol in Fig. 1. Thus, a two-way communication is established between  $A$  and  $B$ .

### 4 The Protocol in Arbitrary Networks

The generalization of the above protocol to a system of  $n > 2$  processes constituting an arbitrary network is now easy. We still assume each pair of neighbouring

processes in the network to be equipped with its two pairs of registers on their common link. In order to simplify the use of variables, we call “*message*” the “information” exchanged between neighbours during the execution of the protocol.

A protocol which stabilizes on a single link may not generalize to a protocol which stabilizes on all links of a (finite) network, e.g. by having each process execute the “link-protocol” in a round robin manner on each individual link adjacent to it. Taking the  $n$ -processes system pair by pair may cause a deadlock: for all  $i \in \{0, \dots, n-1\}$ ,  $A_i$  may be waiting for  $A_{i+1}$  to read from  $Write_{A_i A_{i+1}}$ , with  $A_n = A_0$ .

## 4.1 Notation

**Write register for A:**  $Read_{AB_i}$  is the register in which  $A$  writes the value of the last message read by  $A$  and sent by  $B_i$ .

**Read register for A:**  $Write_{B_i A}$  is the register in which  $B_i$  writes the message to be transmitted to  $A$ , and  $Read_{B_i A}$  is the register in which  $B_i$  writes the value of the last message read by  $B_i$  and sent by  $A$ .

**Write and read register for A:**  $Write_{AB_i}$  is the register in which  $A$  writes the value of the message which is to be sent to its  $i$ th neighbour  $B_i$ .

**Function  $get_i$  for A:**  $get_i$  takes no argument and returns the next message to be sent to the  $i$ th neighbour of  $A$  ( $get_i$  is a helper function added to  $A$ ).

## 4.2 The Read Checking Protocol

On the same assumptions for the model (read/write atomicity) and for the scheduler’s actions (rules of activations of processes and fairness) as given in Section 2, the specification of the self-stabilizing Read Checking protocol in arbitrary networks for a process  $A$ , with neighbours  $B_i$ ’s ( $1 \leq i \leq N_A$ ), is as follows.

---

```

constant  $N_A$       : the number of neighbours of  $A$  ;
var  $s_i$           : message to be sent to the  $i$ th neighbour of  $A$  ;
       $r_i$           : message sent from the  $i$ th neighbour of  $A$  ;
       $val_i$         : value of the last message sent from  $A$  and read by the  $i$ th
neighbour of  $A$  ;

while true do
  for  $i = 1$  to  $N_A$  do
    write( $Write_{AB_i}, get_i$ ) ;
  endfor
repeat

```

```

for  $i = 1$  to  $N_A$  do
   $r_i \leftarrow \mathbf{read}(Write_{B_iA})$  ;
   $\mathbf{write}(Read_{AB_i}, r_i)$  ;
   $val_i \leftarrow \mathbf{read}(Read_{B_iA})$  ;
   $s_i \leftarrow \mathbf{read}(Write_{AB_i})$  ;
endfor
until ( $\forall i \in [1, N_A] \ val_i = s_i$ )
endwhile

```

**Fig. 2.** *The Read Checking protocol for A.*

---

## 5 Proof of the Read Checking Protocol

### 5.1 Proof of Liveness

**Lemma 5.1** *Whatever the execution, every process performs an infinite number of actions.*

**Proof.** Read/write atomicity ensure that each process is always enabled. Therefore, every execution is infinite (every configuration is deadlock-free), and in each configuration that is reached every process can perform an action (fair scheduler). The scheduling of processes' actions is fair: if a process can always execute an action, then the process finally performs an action. Thus, by fairness, every process is performing an infinite number of actions, whatever the execution.  $\square$

**Lemma 5.2** *Let A be a process with its program counter in the **repeat** loop and let B be a neighbour of A. Whatever the current configuration and the execution, the processes system executing the protocol either eventually reaches a configuration in which B allows A to write, or A exits the **repeat** loop.*

**Proof.** Suppose B never allows A to write and A never exits the **repeat** loop. Then A never changes the value in its register  $Write_{AB}$ . Under these conditions, updating its register  $Read_{BA}$  is a writing permission given to A by B (since between the reading of the value from the register  $Write_{AB}$  and the writing of that value in  $Read_{BA}$ , the register  $Write_{AB}$  does not change value).

Whatever the current configuration and the execution, if the program counter of B is not within the **repeat** loop, it takes B less than  $N_B$  actions to enter the **repeat** loop. Once B enters the loop, after  $4N_B$  actions, it updates all its *Read* registers, and thus allows A to write.

Whatever the current configuration and the execution, if the program counter of  $B$  is within the **repeat** loop, it takes  $B$  at least  $4N_B$  actions either to exit the loop, or to update its register  $Read_{AB}$ .

Whatever the execution,  $B$  performs an infinite number of actions (by Lemma 5.2) and eventually, either  $B$  allows  $A$  to write, or  $A$  exits the **repeat** loop.  $\square$

**Definition 5.1** *Let  $A$  and  $B$  be two neighbouring processes.  $A$  is said to allow  $B$  to write iff  $Read_{BA} = Write_{AB}$ . Let  $A$  be a process and let  $N_A$  denote the number of neighbours of  $A$  ( $N_A$  is the degree of  $A$  in the network).*

**Definition 5.2** *Let  $A$  and  $B$  be two neighbouring processes. The update of the register  $Read_{AB}$  is the sequence of the two following actions performed by  $B$ :  $r_i \leftarrow \mathbf{read}(Write_{AB})$  ;  $\mathbf{write}(Read_{BA}, r_i)$ .*

*A wrong writing is a write action in the register  $Read_{BA}$  which is not performed within the context of an update. (The correct writing into the register  $Read_{BA}$  is a write action executed within the context of an update.)*

**Lemma 5.3** *After executing its first action, no process can perform a wrong writing.*

**Proof.** Process  $A$  can perform at most one *wrong* writing, and it may only happen when initially its program counter is set up after reading from the *Write* register and before writing in the *Read* register. Once this write action is executed, each write action of  $A$  in a *Read* register is performed within the context of an update.  $\square$

**Lemma 5.4** *Let  $A$  and  $B$  be two neighbouring processes. After  $B$  executes its first action, if  $B$  allows  $A$  to write, then only the writing of  $A$  in its register  $Write_{AB}$  may be able to cancel that permission.*

**Proof.** Nothing but writing into the register  $Read_{BA}$  or into the register  $Write_{AB}$  can cancel the writing permission. After  $B$  executes its first action, from Lemma 5.3 there is no *wrong* writing anymore. Hence, any writing into the register  $Read_{BA}$  is executed within the context of a register's update. This update is such that the permission remains given to  $A$ , unless  $A$  writes into its register  $Read_{BA}$  during the updating process or after the last update.  $\square$

**Theorem 5.1** *Let  $A$  be a process. Whatever the execution, the system of processes which performs the protocol reaches a configuration in which  $A$  is not within the **repeat** loop anymore.*

**Proof.** Suppose  $A$  remains within the **repeat** loop forever; then  $A$  never writes into its *Write* registers. Every  $4N_A$  actions,  $A$  is checking out the loop exiting condition. Whatever the execution, process  $A$  performs an infinite number of actions. Hence,  $A$  checks out the **repeat** loop exiting condition an infinite number of times. In particular,  $A$  tests the exit condition an infinite number of times after all its neighbours have already executed an action.

If at some test all neighbours of  $A$  allow its writing, then, at the next test, all its neighbours keep on giving  $A$  permission to write (by Lemma 5.4). In the meanwhile,  $A$  has updated its variables  $r_i$  and  $s_i$ , and when the test happens, the loop exiting condition is satisfied:  $A$  exits the loop.

Process  $A$  stays within the loop infinitely long in the case when, at each test, at least one neighbour does not allow its writing. Once a neighbour has allowed  $A$  to write, this neighbour cannot withdraw permission from  $A$ . Therefore, there exists at least one neighbour of  $A$  which never allows  $A$  to write. Now from Lemma 5.2, this is impossible, and the theorem follows. Therefore, the protocol is deadlock-free.  $\square$

**Corollary 5.1** *Let  $A$  be a process. Whatever the execution,  $A$  writes an infinite number of times into all its *Write* registers.*

**Proof.** If  $A$  is out of the loop, then it takes  $A$  less than  $N_A$  actions to enter the loop. When it is within the **repeat** loop, then by Theorem 5.1,  $A$  cannot stay infinitely long.  $N_A$  actions after exiting the loop,  $A$  writes into all its *Write* registers and reenters the **repeat** loop.  $\square$

## 5.2 Correctness Proof of the Read Checking Protocol

**Theorem 5.2** *Let  $A$  and  $B$  be two neighbouring processes. After  $B$  executes its first action and after any writing in the register  $Write_{AB}$ ,  $A$  can write in the register  $Write_{AB}$  only if  $B$  allows it, i.e.  $Read_{BA} = Write_{AB}$  (see Definition 5.1).*

**Proof.** Process  $B$  is the  $i$ th neighbour of  $A$ . Between each of its two writings,  $A$  enters the **repeat** loop and exits the loop. Once  $A$  is within the loop, the register  $Write_{AB}$  does not change value. The **repeat** loop's code is such that when the loop is exited, the value of the local variable  $s_i$  of  $A$  and the value of the register  $Write_{AB}$  are equal. In the loop, the local variable  $r_i$  of  $A$  takes the value of the register  $Read_{AB}$ . The value of the register  $Read_{BA}$  may change after this assignment and before the loop is exited. Thus, when the loop is exited two distinct cases have to be considered:

- No update of the register  $Read_{BA}$  happens between the reading from that register and the loop exit. Then,  $s_i = Write_{AB} = val_i = Read_{BA}$ , and  $B$  allows the writing of  $A$ .

- Writings into the register  $Read_{BA}$  happen between the reading from that register and the loop exit. However, the latter writings are performed within the context of updating. Hence, each time the value has changed, we have that  $Read_{BA} = Write_{AB}$  and, by Lemma 5.4, the equality holds while  $A$  does not rewrite into the register  $Write_{AB}$ .  $\square$

After the writing of a value in the register  $Write_{AB}$ , the first primitive guarantees that  $A$  will only write in the register  $Write_{AB}$  if  $B$  allows it. In the case when the value is new,  $B$  must perform the action  $\mathbf{read}(Write_{AB})$  to allow the writing.

## Summing up of the Results

1. **The protocol is live:** every process is updating all its  $Write$  registers an infinite number of times.
2. **The protocol is correct:** no process can write distinct values twice in a row in its  $Write$  register without any previous reading from that register.

## 6 The Weak Rendezvous Protocol

In this section, we present a self-stabilizing *weak rendezvous* communication primitive.

Recall that The *rendezvous* mechanism (as defined in [16]) synchronizes communication in the link-register asynchronous model of distributed system: each *write* or *read* operation is performed in and from the same register. When Process  $A$  writes a value in its register  $Write_{AB}$ , it cannot perform *any other action* until process  $B$  has completed a *read* operation from the register  $Write_{AB}$ .

The *weak rendezvous* mechanism only requires that between two *write* operations performed by a process  $A$  in  $Write_{AB}$ , process  $B$  performs at least one *read* operation from  $Write_{AB}$ . Therefore, if  $A$  writes a value  $n$  consecutive times (even the same ones in each row) in the register  $Write_{AB}$ , the primitive guarantees that  $B$  copies each of the  $n$  values at least one time, once the system is stabilized.

The weak rendezvous mechanism is based upon the alternating bit technique. After writing in its register  $Write_{AB}$ , process  $A$  changes the value of the bit-register  $Control_{AB}$ .  $A$  can write again in the register  $Write_{AB}$  only after  $B$  has copied the new value of  $Control_{AB}$  into the register  $CheckControl_{BA}$ . And  $B$  copies the value only after reading in the register  $Write_{AB}$ .

The liveness proof of the weak rendezvous protocol is similar to the proof of the read checking protocol. The following Theorem 6.1 proves the correctness of the weak rendezvous protocol.

**Theorem 6.1** *Let  $A$  and  $B$  be two neighbouring processes. After  $B$  executes its first action and after the  $x$ th ( $\geq 2$ ) writing in the register  $Write_{AB}$ ,  $B$  reads the value from  $Write_{AB}$  before the next writing in  $Write_{AB}$ .*

**Proof.** As shown in Theorem 5.2, we can establish that before the  $x$ th writing in the register  $Write_{AB}$ ,  $Control_{AB} = CheckControl_{BA}$ . After the writing in the register  $Write_{AB}$ ,  $A$  changes the value in  $Control_{AB}$  and enters the **repeat** loop ( $Control_{AB} \neq CheckControl_{BA}$ ).  $A$  stays within the loop as long as  $B$  does not copy the value of  $Control_{AB}$  into the register  $CheckControl_{BA}$ . Finally,  $B$  copies the value only after reading in the register  $Write_{AB}$ .  $\square$

The weak rendezvous protocol maintains a weak scheduling of the communication between processes in the following sense. We call a *weak scheduling* of the communication between process  $A$  and all its  $N_A$  neighbours the property that  $A$  can write twice into its registers  $Write_{AB_i}$ , only whenever all the  $B_i$ 's did read from the register  $Write_{AB_i}$  in the meantime ( $1 \leq i \leq N_A$ ).

---

**constant**  $N_A$  : the number of neighbours of  $A$  ;  
**var**  $r_i$  : message sent from the  $i$ th neighbour of  $A$  ;  
 $b_i$  : alternate bit sent from the  $i$ th neighbour of  $A$  ;  
 $c_i$  : alternate bit sent from  $A$  to the  $i$ th neighbour of  $A$  ;  
 $l_i$  : value of the last alternate bit sent from  $A$  and read by the  $i$ th neighbour of  $A$  ;

```

while true do
  for  $i = 1$  to  $N_A$  do
    write( $Write_{AB_i}, get_i$ ) ;
     $c_i \leftarrow$  read( $Control_{AB_i}$ ) ;
    write( $Control_{AB_i}, (c_i + 1) \bmod 2$ ) ;
  endfor
  repeat
    for  $i = 1$  to  $N_A$  do
       $r_i \leftarrow$  read( $Write_{B_iA}$ ) ;
       $b_i \leftarrow$  read( $Control_{B_iA}$ ) ;
      write( $CheckControl_{AB_i}, b_i$ ) ;
       $c_i \leftarrow$  read( $Control_{AB_i}$ ) ;
       $l_i \leftarrow$  read( $CheckControl_{B_iA}$ ) ;
    endfor
    until ( $\forall i \in [1, N_A] \ c_i = l_i$ )
  endwhile

```

**Fig. 3.** *The weak rendezvous protocol for A.*

---

## 7 The Quasi Rendezvous Protocol

In this section, we present a self-stabilizing *quasi rendezvous* communication primitive. A close idea may be found in [4], where the authors also present a self-stabilizing data link protocol under read/write atomicity such that, between two *write* operations in the register, there is only one *read* operation from that register. (See our remarks in section 1.2.)

The *quasi rendezvous* mechanism requires that between two *write* operations performed by the process  $A$  in  $Write_{AB}$ , the process  $B$  cannot perform but one and only one *read* operation from  $Write_{AB}$ . Therefore, if  $A$  writes  $n$  consecutive times the same value (possibly the same one in each row) in the register  $Write_{AB}$ , the primitive guarantees that  $B$  will copie each of the  $n$  values *exactly one time*, once the system is stabilized.

The quasi rendezvous mechanism is based upon the alternating bit technique. After reading from the register  $Write_{AB}$ , the process  $B$  copies the value of the bit-register  $Control_{AB}$  into  $CheckControl_{BA}$ . Now,  $B$  can read again from the register  $Write_{AB}$  only after  $A$  has changed the value of  $Control_{AB}$ . And  $A$  changes that value only after writing in the register  $Write_{AB}$ .

---

```

constant  $N_A$  : the number of neighbours of  $A$  ;
var  $r_i$  : message sent from the  $i$ th neighbour of  $A$  ;
 $b_i$  : alternate bit sent from the  $i$ th neighbour of  $A$  ;
 $c_i$  : alternate bit sent from  $A$  to the  $i$ th neighbour of  $A$  ;
 $l_i$  : value of the last alternate bit sent from  $A$  and read by the  $i$ th
neighbour of  $A$ ;
 $d_i$  : value of the last alternate bit sent from the  $i$ th neighbour of  $A$ 
and read by  $A$ 

while true do
  for  $i = 1$  to  $N_A$  do
    write( $Write_{AB_i}, get_i$ ) ;
     $c_i \leftarrow$  read( $Control_{AB_i}$ ) ;
    write( $Control_{AB_i}, (c_i + 1) \bmod 2$ ) ;
  endfor
  repeat
    for  $i = 1$  to  $N_A$  do
       $b_i \leftarrow$  read( $Control_{B_iA}$ ) ;
       $d_i \leftarrow$  read( $CheckControl_{AB_i}$ ) ;
      if  $b_i \neq d_i$  then
         $r_i \leftarrow$  read( $Write_{B_iA}$ ) ;
        write( $CheckControl_{AB_i}, b_i$ ) ;
      endif
       $c_i \leftarrow$  read( $Control_{AB_i}$ ) ;
       $l_i \leftarrow$  read( $CheckControl_{B_iA}$ ) ;
    endfor
  until ( $\forall i \in [1, N_A] \ c_i = l_i$ )
endwhile

```

**Fig. 4-** *The quasi rendezvous protocol for  $A$ .*

---

The liveness proof of the quasi rendezvous protocol is similar to the proof of the read checking protocol.

**Definition 7.1** *Let  $A$  and  $B$  be two neighbouring processes.  $B$  is said to allow  $A$  to write iff  $CheckControl_{BA} = Control_{AB}$ .*

**Definition 7.2** *Let  $A$  and  $B$  be two neighbouring processes. The full reading of register  $Write_{AB}$  is completed by the sequence of the four following actions performed by  $B$ :*

$b \leftarrow$  **read**( $Control_{BA}$ ) ;  $d \leftarrow$  **read**( $CheckControl_{AB}$ ) ; **if**  $b \neq d$  **then**  $\{r \leftarrow$  **read**( $Write_{BA}$ ) ; **write**( $CheckControl_{AB}, b$ ) ;  $\}$ .

**Definition 7.3** Let  $A$  and  $B$  be two neighbouring processes. The full writing of register  $Write_{AB}$  is completed the sequence of the three following actions performed by  $A$ :

**write**( $Write_{AB}, get$ ) ;  $c \leftarrow$  **read**( $Control_{AB}$ ) ; **write**( $Control_{AB}, (c + 1) \bmod 2$ ) ;

**Lemma 7.1** Let  $A$  be a process with its program counter in the **repeat** loop and let  $B$  be a neighbour of  $A$ . Whatever the current configuration and the execution, the system of processes executing the protocol either eventually reaches a configuration in which  $B$  allows  $A$  to write, or  $A$  exits the **repeat** loop.

**Lemma 7.2** After executing its first three actions, no process can perform an incomplete reading or writing.

**Lemma 7.3** Let  $A$  and  $B$  be two neighbouring processes. After  $B$  and  $A$  execute their first three actions, if  $B$  allows  $A$  to write, then only the complete writing of  $A$  in its register  $Write_{AB}$  may be able to cancel that permission.

**Proof.** The proof of the three above lemmas (7.1, 7.2 and 7.3) is similar to the proof of Lemma 5.2, Lemma 5.3 and Lemma 5.4, respectively.  $\square$

**Theorem 7.1** Let  $A$  be a process. Whatever the execution, the system of processes which performs the protocol reaches a configuration in which  $A$  is not within the **repeat** loop anymore.

**Sketchproof.** The proof is by contradiction and it is similar to the proof of theorem 5.1.  $\square$

**Corollary 7.1** Let  $A$  be a process. Whatever the execution,  $A$  writes an infinite number of times into all its  $Write$  registers.

The following Theorems 7.2 and 7.3 prove the correctness of the quasi rendezvous protocol.

**Theorem 7.2** Let  $A$  and  $B$  be two neighbouring processes. After  $A$  and  $B$  execute their first three actions and after the  $x$ th ( $\geq 2$ ) writing in the register  $Write_{AB}$ ,  $B$  reads the value from  $Write_{AB}$  before the next writing in  $Write_{AB}$  can take place.

**Proof.** We can establish that before the  $x$ th writing in the register  $Write_{AB}$ ,  $Control_{AB} = CheckControl_{BA}$ . After writing into the register  $Write_{AB}$ ,  $A$  changes the value in  $Control_{AB}$  and enters the **repeat** loop ( $Control_{AB} \neq CheckControl_{BA}$ ).  $A$  stays within the loop as long as  $B$  does not copy the value of  $Control_{AB}$  into the register  $CheckControl_{BA}$ . Finally,  $B$  copies the value only after reading from the register  $Write_{AB}$ .  $\square$

**Theorem 7.3** *Let  $A$  and  $B$  be two neighbouring processes. After  $A$  and  $B$  execute their first three actions and after  $B$  reads from  $Write_{AB}$ ,  $A$  performs a complete writing in  $Write_{AB}$  before the next reading from  $Write_{AB}$ .*

**Proof.** Before the reading from  $Write_{AB}$ ,  $Control_{AB} \neq CheckControl_{BA}$ . After the reading from the register  $Write_{AB}$ ,  $B$  changes the value in  $CheckControl_{BA}$ . Now,  $B$  does not change the value in  $CheckControl_{BA}$  ( $B$  does not read from the register  $Write_{AB}$ ) as long as  $A$  does not change the value in  $Control_{AB}$ . After the first three actions of  $A$ , changing the value in  $Control_{AB}$  is made after  $A$ 's writing in  $Write_{AB}$ .  $\square$

The quasi rendezvous protocol maintains a scheduling of the communications between processes in the following sense. We call a *scheduling* of communications between process  $A$  and all its  $N_A$  neighbours the property that  $A$  can write twice into its registers  $Write_{AB_i}$ , only whenever each of the  $B_i$ 's performed *one unique* reading from the register  $Write_{AB_i}$  in the meantime ( $1 \leq i \leq N_A$ ).

## 8 Concluding Remarks

The paper presents three very basic general protocols for the design of fair and reliable self-stabilizing communication primitives. Both protocols work in arbitrary networks and also ensure minimal scheduling properties, whatever the initial configuration of the system of processes and the activations by the scheduler. In particular, the last protocol entails the mechanism of a “quasi rendezvous”, which proves useful in more involved self-stabilizing protocols.

Each primitive can actually be used as a “black box” by a separate protocol, handling the procedures in more involved self-stabilizing algorithms. Thus, the protocols may be modified according to the designer’s will and needs: e.g., in specific topologies of networks a weak scheduling of communications may impose fewer neighbours to read from the registers. For example, with only one neighbour, a point to point self-stabilizing quasi rendezvous mechanism may also be completed. Along the same lines, the protocols also simulate reliable self-stabilizing message-passing in asynchronous distributed systems.

Although the paper does not concern itself with complexity measures, it is worth mentioning that when time is measured by some appropriately defined round complexity, the stabilization time of the read checking protocol is  $O(1)$ .

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