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A Passive Mixer for 60 GHz Applications in CMOS 65nm Technology

Mariano Ercoli [#*], Michael Kraemer[#*], Daniela Dragomirescu[#*], Robert Plana[#*]

[#]CNRS; LAAS; 7 avenue du colonel Roche, F-31077 Toulouse, France
* University of Toulouse ; UPS, INSA, INP ISAE; LAAS; F-31077 Toulouse, France

mercoli@laas.fr; mkraemer@laas.fr; daniela@laas.fr; plana@laas.fr

***Abstract* — A study of the feasibility of a wide band double balanced resistive mixer in the 60 GHz band is done. The device is implemented in a 65nm CMOS technology process. In this paper an approach to design an optimized version of the mixer in terms of the principal figures of merit: conversion loss, port to port isolation and noise figure is shown. The mixer will be a part of an homodyne down-conversion system. The conversion loss is 6.9±0.2dB around 60GHz with a − 5dBm of LO drive. The port-to-port isolation for the LO feed through is better than 41dB. The noise figure is 8.39dB. The power dissipation for the mixer depends on the LO buffer that increases the input LO power. Its power consumption is 15mW.**

***Keywords* — Passive Mixer, Homodyne receivers, 60GHz Band, Low Power, CMOS, Direct Conversion.**

I. Introduction

The unlicensed frequency band around 60GHz is today at the center of the research community interest. There are many applications proposed in this band and the request for cheap circuit is rising. Silicon-based technologies, with their inexpensive production cost and a continuous reduction of channel dimension, become an attractive alternative for the realization of millimeter-wave integrated circuits. This technological process moreover offers a high-level integration capability for high-frequency front-end circuitry with the chance to integrate analog and digital blocks on a single chip.

The optimization of the basic building blocks is an important objective. In particular, it is important to take into account the parasitic phenomena that occur at millimeter waves. For the receiver circuitry the choice of the mixer's architecture is very important, because it influences the entire down-conversion chain. Heterodyne systems employ two consecutive stages of down-conversion, while the homodyne system requires only one mixer. In the second case the complexity of the system is lower. The direct down-conversion however has drawbacks. The typical issues are the DC voltage offset and strong flicker noise. These phenomena are particularly remarkable on a classical active architecture: the Gilbert cell mixer. Another problem of the active mixer configuration is the linearity. This aspect is accentuated by the low voltage supply for sub-micrometer devices [1]. An alternative approach can be the use of a passive mixer. This architecture allows a very good linearity, suitable for high dynamic range receiver design, [2] and a very limited flicker noise effect, due to the absence of channel DC bias current. Moreover, the passive mixer has a simple architecture and zero power dissipation. The disadvantage of this class of frequency converter is their conversion loss.

This paper analyses a lot of the factors that determine the passive mixer behavior. The design of the mixer was done with the concurrent evaluation of the conversion gain, linearity, noise figure, and power dissipation.

The presence of a local oscillator (LO) buffer stage is justified by the requirement for large LO amplitudes to drive the switch system. This is done to avoid the increase of the conversion loss.

II. Consideration Concerning The Behavior Of The Switches

An ideal configuration for a double balanced passive mixer is shown in Figure 1. Intermediate Frequency (IF), Radio Frequency (RF) and LO ports are indicated.

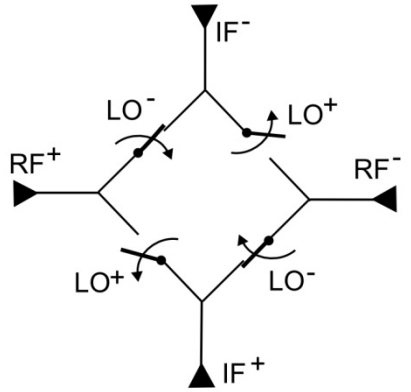

Figure 1: Ideal passive mixer composed by four switches driven by a balanced local oscillator

In the ideal case, the switches are controlled by a LO square wave signal. The transfer function of the ideal

system, based on the down-conversion voltage gain, is [1] then

$$G_C = \frac{Output\ Signal\ Level(IF)}{Input\ Signal\ Level\ (RF)} = \frac{2}{\pi} \qquad (1)$$

Therefore, for an ideal dual balanced passive mixer the minimum conversion loss is around 4 dB.

This value, however, neglects many parasitic effects that affect the real transistor and the interconnection networks. The problem of the different behavior between an ideal switching device and a real MOS switch is discussed in [2]. In that paper it is shown that the voltage-gain of a mixer is in strict relation with the allowed minimum R_{ON} and the allowed maximum Z_{OFF}:

$$G_C = 20log_{10}\left[\frac{2}{\pi}\left(\frac{Z_L}{Z_L+R_{ON}||Z_{OFF}}\right) - \frac{2}{\pi}\left(\frac{Z_L}{Z_L+Z_{OFF}}\right)\right] \qquad (2)$$

An important variable in the R_{ON} and Z_{OFF} definition is the geometrical parameter "W_t". The minimum gate resistance

$$R_{ON} = \frac{L_g}{\mu_n C_{OX} W\left(\left(V_g - g_c v_{RF}\right) - V_{th} - V_{ds}\right) Z_L} \qquad (3)$$

is inversely proportional to the gate width (Wt). So, for a low channel resistance, the value of Wt has to be very high. Note that the gate length (L_g) is set to the minimum value allowed by the technology (here 65nm) in order to maximize f_{MAX} and f_T.

Regarding the Z_{OFF} impedance, W_t determines the amount of parasitic capacitance that causes a drop of the total off-impedance. The estimation of an optimum value of W_t is critical to establish the best trade-off between R_{ON} and Z_{OFF}. For the off-state of the MOS, the impedance is represented by a high channel resistance and a set of parasitic capacitances, as shown in Figure 2.

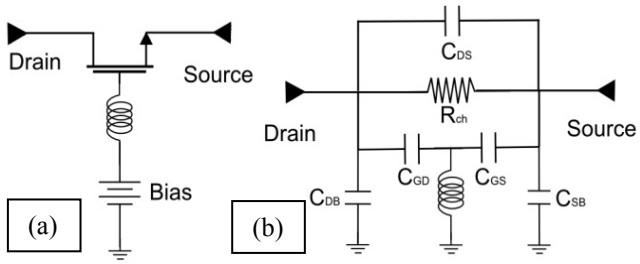

Figure 2: Equivalent circuit for a switch in off-state. A negative value (-0.5V) of bias voltage is imposed to well simulate the off-state of the switch.

In off-state, R_{ch} shows a high value due to the depletion of the channel. The drop of the total Z_{OFF} impedance is caused by the connection of the capacitance C_{DS} and the influence of the parasitics C_{GD}, C_{GS}, C_{DB} and C_{GB}. This parasitic effect is linearly proportional to the transistor's width W_t. Figure 3 shows the fitting curves of the equivalent circuit (named on Figure 3 *Eq-Circ*) versus the real CMOS device, (named on Figure 3 *Sim*) in terms of the S_{21} parameter. The data are represented for four different transistor dimensions (W_t = 35, 50, 80 and 96 um). For the real CMOS transistor the simulations were done using the complete model of the transistor, including the parasitic elements of the real device, Figure 2(a). The good matching of the curves demonstrates the validity of the equivalent circuit and its quality.

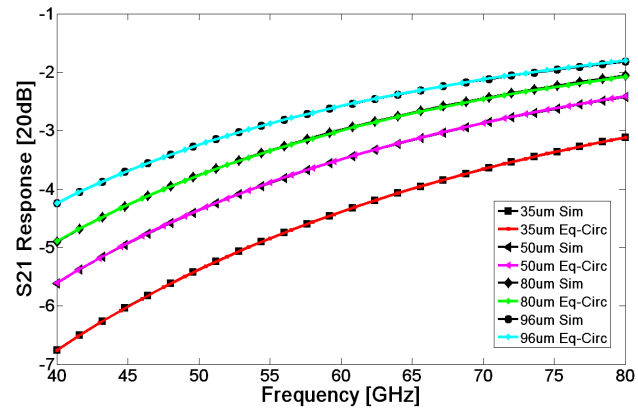

Figure 3: S_{21} values for the real transistor and equivalent circuit.

The graph on Figure 3 underlines the strong influence of the parasitic capacitance. The Drain-Source isolation falls with the rise of W_t. In the 60GHz band, the value of the capacitance builds a low impedance path for the RF signals. Figure 4 reports the variation of value for the principal parameters in the equivalent circuit versus the device size (W_t). The non-perfect linearity for the value is caused by different realizations, in terms of finger number (N_f), single finger width (W_f) and metal interconnection geometry. For the resistance, instead, the linearity is respected because it depends only on the dimension W_t.

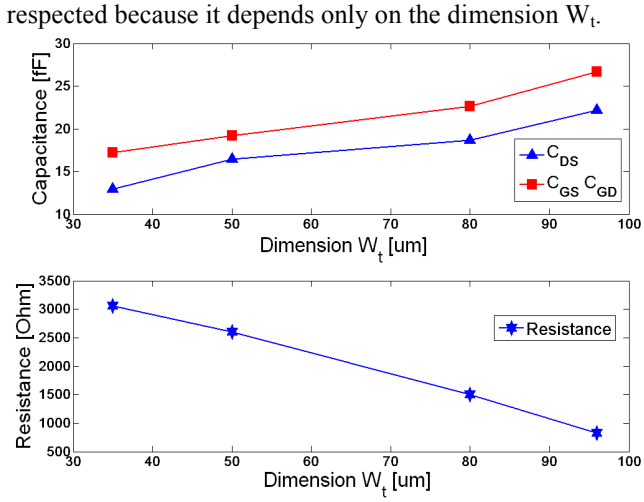

Figure 4: Capacitance and resistance variation versus device size.

To establish a consistent value for the capacitance on the equivalent circuit, the evaluation of C_{GS} and C_{GD} have been made following the guidelines proposed in [3]. The R_{ch}, C_{DS}, C_{DB} and C_{SB} are utilized like a variable parameter to fit the MOSFET's simulated curve. Thanks

TABLE I

State of the Art Passive Mixer					
Papers #	**Freq**	**Conv. Loss min**	**LO Power Drive**	**NF**	**Isolation**
[4]	900 MHz	4.7dB	+7dBm	6.5dB	NA
[10]	0.9÷1.8 GHz	5.8 dB	14 dBm	5.8	43dB
[12]	5÷6 GHz	6 dB	0 dBm	NA	45 dB
[6]	3GHz	6÷6,5 dB	+7dBm	NA	45dB
This work	**60GHz**	**6.9±0.2 dB**	**-5 dBm**	**8.39 dB**	**41 dB**
[7]	5 GHz	7 dB	0 dBm	8	45dB
[8]	19÷26.5GHz	7.6 dB	6 dBm	NA	28dB
[5]	11GHz	7±0.5 dB	+9dBm	7.5dB	37±1dB
[11]	2.4 GHz	7.8 dB	10 dBm	NA	48 dB
[9]	26.5÷30 GHz	10 dB	0 dBm	11.4	33dB

to this procedure it was possible to evaluate the effects that the capacitance variation has on the behavior of the MOSFET switch at 60GHz. In conclusion, a tradeoff has to be done between R_{ON} and Z_{OFF}. The realization of large devices allows to minimize the R_{ON} resistance but the parasitic capacitance lead nevertheless to a Z_{OFF} degradation. In this case the best compromise achieved to realize a 60GHz passive mixer, is to employ a 50um wide device. This value of Wt is a good trade-off between R_{ON} and Z_{OFF}.

III. Mixer Realization

The mixer design flow is thought to achieve the minimum conversion loss together with a limited LO drive. The literature shows that this compromise is not an easy target. Table 1 summarizes the state-of-the-art for the passive CMOS mixer design. A lot of this devices work at lower frequencies (0.9-5GHz) and only 2 configurations are employed in K band. Different technologies like SiGe or GaAs are used for this type of architecture, but these processes are more expensive in mass production. Moreover another significant aspect is that CMOS has a lower power requirement compared to the other technologies.

The layout's optimization has been made through the simulation of its conversion gain. The layout of the single transistor is done to minimize the phase difference of the signal at the gate.

This precaution has bound the transistor's finger width W_f to 2.5um and it guarantees the optimal signal distribution and a very compact device core. Thanks to this approach, the port-to-port isolation and the inductive degeneration due to connection lines are limited. A simulation of the transfer function of the device is shown in Figure 5.

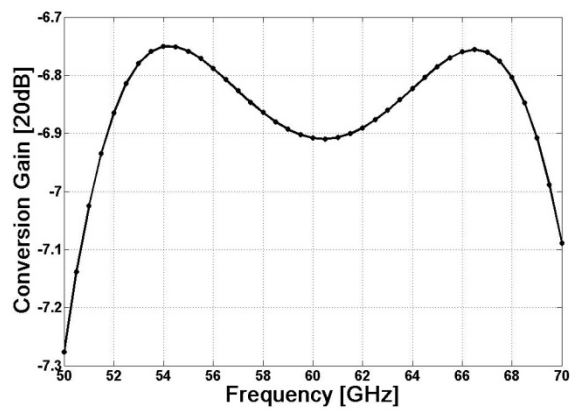

Figure. *5*: Mixer's Conversion Gain for a LO power level of −5dBm.

IV. Matching Network

The work on the matching networks component requires particular attention. The conversion loss of the mixer in fact is very susceptible to the parasitic resistance of the matching inductor. This phenomenon is particularly critical on the high frequency path (RF and LO shunt inductor).To decrease this effect, a combination of lumped elements and transmission lines were used to achieve an acceptable trade off for the matching elements. However the drop of the conversion loss is 1.8dB higher with respect to the ideal behavior. The return loss for the LO and the RF port is better than -13dB in the band of interest. The port-to-port isolation for the LO feed through is better than 40dB for the center frequency of 60GHz. The simulated noise figure (NF_{DSB}) for the structure is 8.39dB. In Figure 6 is shown the variation of NF_{DSB} for different values of LO power while Figure 7 shows the matching network employed on the circuit.

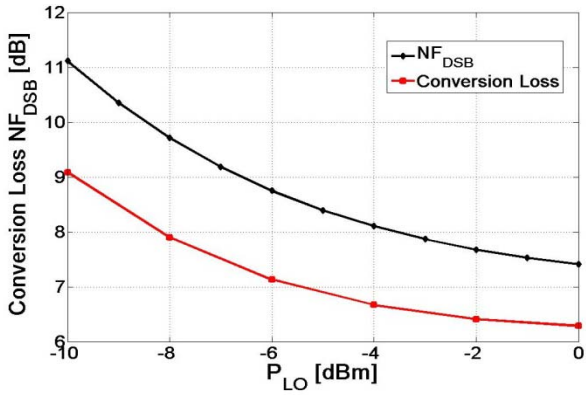

Figure. *6*: DSB Noise Figure in function of the Power level of the local oscillator (P_{LO})

IV. LO BUFFER

To realize a differential buffer stage for the LO signal, a Cascode configuration is chosen to guarantee good isolation, high gain, good stability and low power consumption. However, in the high frequency band the capacitance of the transistor becomes more dominant, so more caution is required when designing the transistor device. In this case a tradeoff is done to achieve 10 dB of Gain, and a -1dB compression point at 0dBm. The power dissipation for the differential buffer is 15 mW

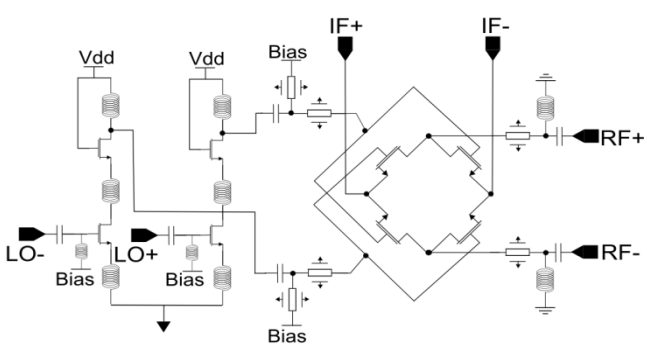

Figure 7: Schematic of the Mixer and LO Buffer with the matching network

V. CONCLUSION

A new wide-band dual balanced resistive mixer in silicon CMOS 65nm technology is presented here realized for the 60GHz unlicensed band. This mixer works with a very low LO drive of -5dBm. An equivalent circuit for the parasitic phenomena of the MOS switch is proposed to underline the strong effect of the MOS capacitance. The performed simulations of the mixer circuit show an excellent behavior. The circuit was sent to fabrication Nov 2009, using the CMP facilities (http://cmp.imag.fr/). Similar performance is expected for the fabricated mixer because all parasitics are modeled and accurate models are used for active and passive devices at 60GHz [13].

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