On the De-embedding of Small Value Millimeter-wave CMOS Inductor Measurements

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***Abstract*—In radio frequency integrated circuits using a low resistivity silicon substrate, spiral inductors show advantages in performance and size with respect to transmission lines, even at frequencies as high as 60 GHz. In order to verify simulation results and build accurate models, test inductors need to be fabricated and characterized very accurately. This implies the precise determination of the effective quality factor Q_{eff} and the measurement of the inductance L within a few pico-Henrys.**
This paper reviews suitable on-chip calibration and de-embedding techniques and proposes a technique that uses distributed *and* lumped elements to model the error two-ports. These elements also take into account the contact impedance.
The results obtained by this novel de-embedding approach are compared to results of the other discussed methods and to simulation results. The obtained agreement proves the suitability of the proposed method for characterization of millimeter-wave inductors.

I. Introduction

In the unlicensed frequency range around 60 GHz, the very first silicon RFIC designs used transmission lines for matching. They were followed by circuits based on spiral inductors that regularly exhibit superior performance and smaller size [1], [2]. In order to measure the performance of these inductors over a very broad frequency range (typically from around DC up to 67 GHz), inductor test structures are used. They consist of the inductor under test (IUT), which is surrounded by a structure allowing to properly place on-wafer probes (cf. section II-A) while respecting minimum distances recommended by the probe manufacturer.
The S-parameters of the IUT are obtained by measurements using a vector network analyzer (VNA). They are corrected by a two-step calibration procedure: The first calibration is done by the VNA, and uses an Impedance Standard Substrate (ISS) with high precision calibration standards, like **S**hort, **O**pen, **L**ine and **T**hru in the case of the SOLT calibration. By this first calibration, the reference plane is shifted to the probe tips. However, it has to be taken into account that the calibration is done on a substrate with gold metallization, while the pads on the CMOS chip are usually made of aluminum [3].
The second step of the correction is discussed in detail in this paper. It consists in moving the reference plane up to the IUT or rather removing the parasitics of the test structure and taking into account the difference in contact resistance.
Note that the accuracy requirements are extremely high, because the typical inductor values at 60 GHz lie between 50 pH and 350 pH and the quality factors on low resistivity silicon vary from around 15 to 20, so resistance values around one Ohm have to be determined precisely. If measurements and de-embedding are not done attentively, the tolerances (especially due to contact resistance repeatability) can exceed the series resistance value, yielding unphysical, even negative values.

II. A Typical Test-Structure for CMOS Inductors

A. Test Structure Geometry

The geometry of a typical test structure for inductor measurements is given in fig. 1. It is symmetrical around the IUT in order to facilitate layout and de-embedding. Each side contains one signal pad and two ground pads. While the signal pads are implemented only in the topmost metal layer and float on the inter-metal dielectric, the ground pads consist of a stack of via-connected metal polygons that descend down to the lowest two metal layers. They serve as ground plane and are well connected to the conductive substrate.
The terminals of the IUT are connected to the signal pads, while the IUT's grounding structure (for 60 GHz circuits usually a ground ring is recommended) is joined all along the reference plane.
The tips on the on-wafer probes are also indicated in fig. 1. The contact, whose resistance is particularly important for Q-accurate measurements (cf. section II-C), is illustrated by the shaded area around the tip. Note the two reference planes in fig. 1: The first one (at the probe tips) results from the calibration on ISS, the second one (at the IUT terminals) is obtained after applying the techniques detailed in this paper.

B. Test Structure Parasitics

The test-structure introduced in the previous subsection adds the following parasitics to the IUT:

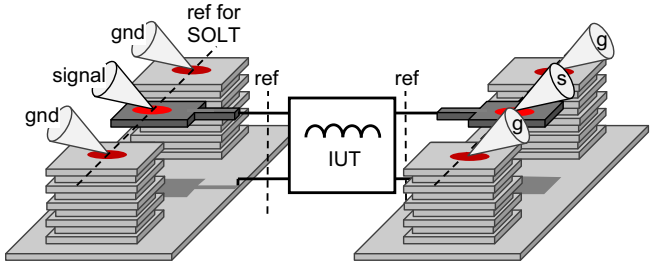

Fig. 1. Perspective view of the test structure (with probes sitting on ground and signal pads) and illustration of the contact area

- A pad capacitance between the signal pad and the ground, together with some (minor) associated dielectric loss
- The parasitics of the connection between signal pad and inductor. These parasitics include series inductance and loss as well as capacitance to ground
- The contact inductance, which depends on the distance between probe contact area and the boundary of the pad on the IUT side. It is negligible if this distance is very small.
- A contact resistance originating from the non-ideal contact between probe tip and aluminum pad

C. Contact Resistance on Aluminum Pads

The parasitic contact resistance R_{contact} plays a particular role for two reasons: First, R_{contact} depends on the pad material, which is usually *gold* for the ISS, but *aluminum* for the CMOS chip [3]. Thus after having done the first calibration (here: SOLT), the difference

$$R_{\text{contact,diff}} = R_{\text{contact,Al}} - R_{\text{contact,Au}} \tag{1}$$

still has to be taken into consideration for the second de-embedding step.

Fig. 2 shows a typical curve of $R_{\text{contact,diff}}$. Note that it is possible for $R_{\text{contact,diff}}$ to become negative (here at higher frequencies), due to the fact that for a particular measurement the aluminum contact is better than the gold contact.

The second point which proves Q-accurate inductor measurements particularly critical is the repeatability of the contact resistance [3]. To get a repeatable contact, a well defined, large force has to be applied to the on-wafer probes (unfortunately wearing them off rapidly), and the position of the probe tips has to be defined as accurately as possible. For the particular probes used for the measurements presented in this paper (GGB Inc.'s Picoprobes made of Beryllium-Copper, pitch 100 µm), a skate reaching from one rim of the signal pad to the other one, i.e. around 40 µm, assured a good repeatability. To affirm a proper contact, multiple measurements, between each of which the probes are lifted, are done for each structure.

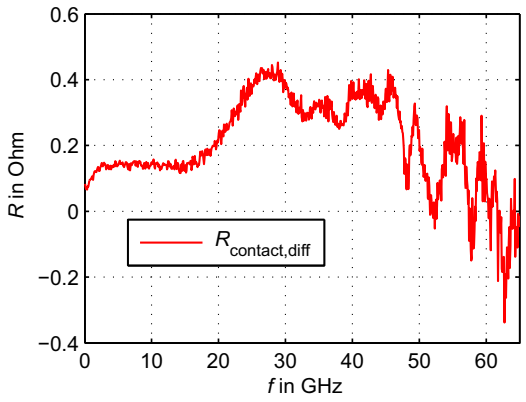

Fig. 2. Difference between contact resistance on aluminum and on gold obtained from the measurement of microstrip line test-structures

III. Calibration and De-embedding

Three different methods to remove the test structure parasitics in the second calibration step are discussed in this section.

Two of them make use of a technique to accurately obtain the transmission line parameters (characteristic impedance Z_0 and complex propagation constant γ) of a pair of microstrip lines, as introduced in [4]. This technique requires two microstrip line test structures of different length, and yields as by-product also the pad admittance of the test structure.

A. TRL-Calibration

If no further assumptions about the test structure parasitics are be made, two unknown error two-ports surround the device as illustrated in figure 3. The classical TRL calibration [5] can be used in this case. It requires three calibration standards: A **T**hru connecting both reference planes, a **R**eflect (e.g. short circuit) at each reference planes that provides no transmission, and a **L**ine between them.

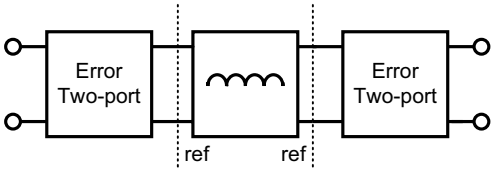

Fig. 3. Error two ports assumed during TRL calibration are considered to be black boxes, no assumptions are made concerning the inside

The line standard is the critical element, because it has to provide the reference impedance for the correction. As the characteristic impedance of a line in a CMOS technology cannot be precisely set to 50 Ω between near DC and 67 GHz, the TRL-corrected results have a generally frequency dependent, complex impedance $Z_0(f)$. To obtain $Z_0(f)$ from line measurements, the prior mentioned technique [4] is used by the authors. As one of the line standards for this extraction the thru can be used. Based on this extraction, the TRL results can be renormalized to 50 Ω.

In practice, the TRL calibration exhibits drawbacks if the used standards are small: Firstly, the line standard should have a certain electrical length (usually $> 20°$). Secondly, and more important in the present case, the thru standard should have negligible coupling between its input ports (i.e. the transmission from one port to the other one should be uniquely by a quasi TEM-wave on the microstrip line). If this is not the case, the effective port impedances for thru standard and line standard are different (even if their geometry is the same at the reference plane), and the calibration is not valid. The described behavior is observed in the present case at higher frequencies, because the pads of the thru test structure are very close.

B. Lumped-Element De-embedding

Lumped element de-embeding (e.g. [6]) assumes that the test structure parasitics can be approximated by a parallel

admittance and a series impedance as in fig. 4. The series element can be obtained by half of the series impedance of a through, while the parallel admittance can be obtained by the reflection measurement of an open standard.

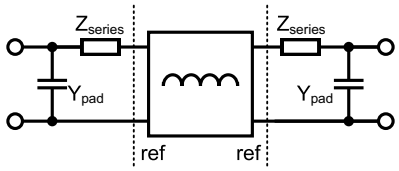

Fig. 4. Lumped element de-embedding assumes a parallel admittance and a series impedance as error two-port

The drawback of this technique is that the lumped element assumption becomes invalid at mm-waves, where the series element is accompanied by distributed capacitances. Furthermore, the contact resistance is not de-embedded at the right location. The consequences of these simplifications can be observed from measurement results (cf. section IV).

C. Newly Proposed Mixed-element De-embedding

In order to get a more accurate correction, the authors propose to de-embed the parasitics illustrated in the equivalent circuit in fig. 5. It resembles the one suggested in [7], however, a contact impedance Z_{contact} is added. To obtain all the required element values, only two line standards of different length are required. First, the difference of their series impedances is used to estimate the contact resistance $R_{\mathrm{contact,diff}}$. Then the two line measurements are corrected with respect to these contact impedances using ABCD - parameters.

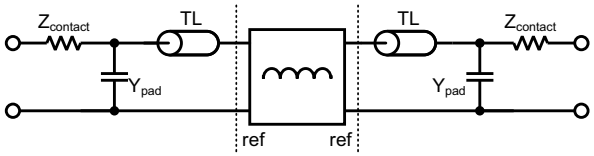

Fig. 5. proposed equivalent circuit model for error two ports surrounding the inductor under test

The line parameters of these $R_{\mathrm{contact,diff}}$-free microstrip lines are then extracted by the prior mentioned technique [4]. The ABCD matrix of the test structure's line element (the line lengths are known from layout) is subsequently found. A multiplication of the inverse matrix de-embeds the line segments. The pad admittances result also from the extraction according to [4], and can be de-embedded using Y-parameters. Compared to the TRL-calibration and the lumped de-embedding technique, the proposed mixed de-embedding technique avoids the use of a thru standard, whose drawback is unwanted coupling between its input ports. In addition, two standards are sufficient to characterize all the parasitics to de-embed. The distributed nature of the test structure is well taken into account, while at the same time the lumped contact impedance is correctly removed.

IV. Measurement Results

To assess the performance of the presented de-embedding and calibration techniques, they are compared to each other and to simulation results. Identical S-parameters, obtained by VNA measurements after applying the first SOLT calibration, are the basis for all of the presented results.

The measured test inductor is shown in fig. 6. It has a diameter of 30 µm, a conductor width of 3 µm and is implemented in the top-most copper metal layer of STMicroelectronics' 65 nm CMOS technology.

The importance of de-embedding the pad capacitance is illustrated in fig. 7. The return loss measured with and without de-embedding is very different, however, a difference between the presented de-embedding techniques is not observable.

The influence of the correction techniques on S_{21} is shown in fig. 8. The two techniques that are expected to correct the series parasitics more accurately, i.e. TRL and mixed-element de-embedding, show results very close to each other (note the scale on the abscissa, indicating measurements close to achievable tolerances).

In order to asses the influence of the de-embedding techniques on the differential inductance

$$L_{\mathrm{diff}} = \frac{\mathrm{Im}(Y_{21})}{2\pi f} \tag{2}$$

and the effective quality factor

$$Q_{\mathrm{eff}} = \frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \tag{3}$$

(where Y_{ij} are the Y-parameters), these quantities are compared to results obtained from HFSS simulations of the IUT in figures 9 and 10. The (very small) discrepancy of L_{diff} between the different measurement and simulation results can be explained by the use of a thru standard for TRL and lumped de-embedding: The series inductance between the ports of the thru is probably underestimated due to coupling effects.

Up to 40 GHz, the Q factor obtained using the discussed de-embedding techniques agrees exactly with simulations. Only the TRL method suffers somehow from the only 200 µm long line standard.

At higher frequencies, the VNA's measurement accuracy is

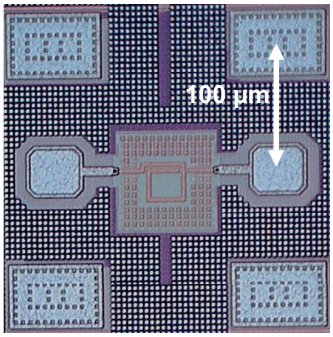

Fig. 6. Die photo of the measured test structure containing two error two-ports and the IUT

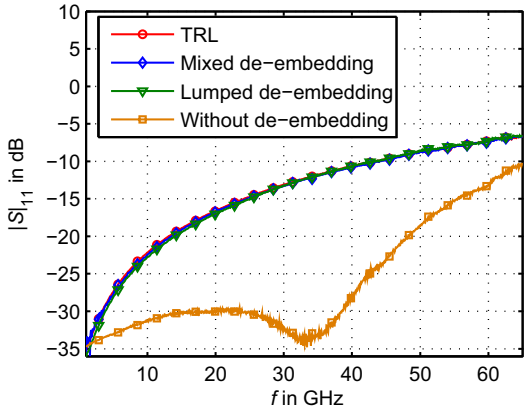

Fig. 7. Reflection coefficient at port one of the test inductor, with and without de-embedding of the test structure

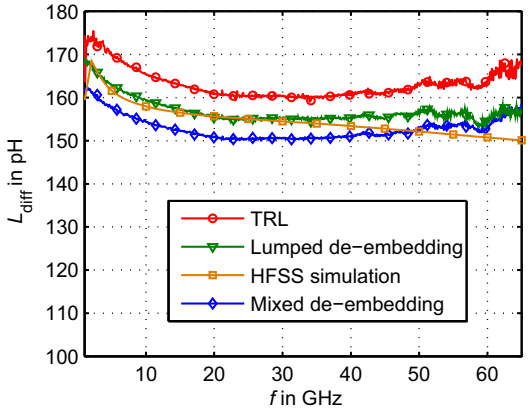

Fig. 9. Comparison of differential inductance obtained using different de-embedding techniques and HFSS simulation

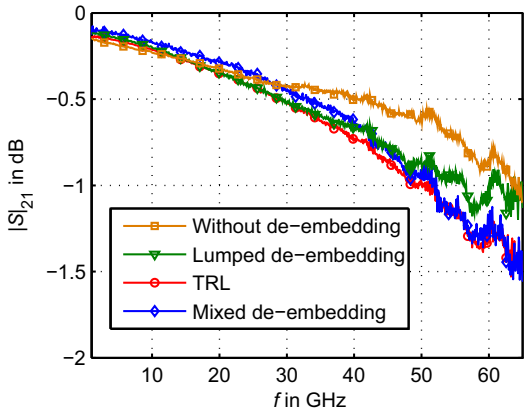

Fig. 8. Transmission coefficient of the test inductor, with and without de-embedding of the test structure parasitics

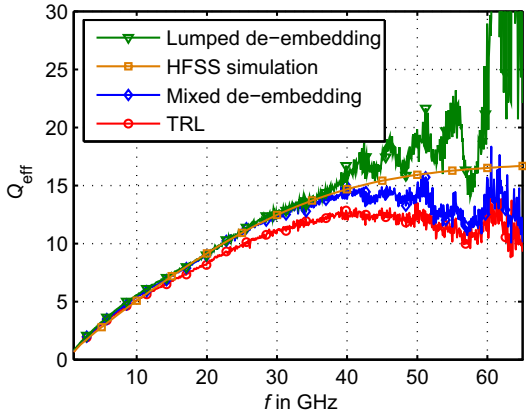

Fig. 10. Comparison of effective quality factor from different de-embedding techniques and HFSS simulations

the limiting factor, shown by the noisy, strong variation of the measured curve. The degree of accuracy already obtained becomes clear when noting that a change in series resistance of only one Ohms changes the Q factor from 12 to 18. Nevertheless, TRL and mixed de-embedding show a good proximity to the simulation results, while the mixed technique is slightly closer to simulations. Lumped-element de-embedding suffers from before-mentioned limitations.

Further comparison of the de-embedded measurement results to simulation results obtained with Sonnet, ASITIC and HFSS can be found in [8].

V. Conclusion

Techniques to remove the parasitics of typical test structures for RFIC spiral inductor measurements have been discussed and evaluated. A newly proposed mixed-element de-embedding technique that removes the contact resistance, the pad capacitance and a transmission line segment from the IUT yields better results than the classical lumped de-embedding technique. It requires only two transmission line test structures to obtain all parasitics.

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