



Emerging Nanotechnology for integration of Nanostructures in Nanoelectronic devices

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Emerging Nanotechnology for Integration of Nanostructures in Nanoelectronic Devices

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1. Introduction

Scaling down of semiconductor devices is the driving force for the development of new applications (mobile phone, memory cards, sensors, *etc.*). Up to now, device downscaling has been enabled by the top-down approach, combining lithography and etching technologies. However, we will soon reach the limitation of this approach to form nanostructures with uniform properties. In this context, the bottom-up approach, *i.e.* elaborating nanostructures in a self-ordered manner and integrating them directly into devices, seems to be a promising way to push towards miniaturization of microelectronics components and to create new functionalities.¹

In this chapter, we will focus our attention on two emerging nanotechnologies we have developed to fabricate, organize and integrate nanomaterials (nanodots, nanowires) in nanoelectronics devices.

The first one uses the natural properties of diblock copolymers² to create (i) a hexagonal lattice array of vertical PMMA cylinders in a polystyrene (PS) matrix, or (ii) an ordered array of horizontal PMMA cylinders in a PS matrix. These films are then used as deposition and/or etching masks to produce dense lattices of 20 nm diameter nanoparticles and nanowires with a density of around 10^{11} cm^{-2} . Examples of integration with an 8-inch wafer memory technology will be shown.

The second technology is based on chemical vapor deposition (CVD)³ of basic nanomaterial building blocks for future microelectronics. We focus on CVD growth of Si nanostructures using a fully compatible CMOS process. The resulting nanoobjects are integrated in test devices and measured electrically.

2. Diblock copolymer technology for nano-objects fabrication

In this chapter, we use an asymmetric polystyrene-block-methyl methacrylate (PS-b-PMMA) diblock copolymer having a PMMA weight fraction of 0.3 with a molecular weight (MW) of $67100 \text{ g}\cdot\text{mol}^{-1}$ and a polydispersity of 1.09. A thin $\sim 39 \text{ nm}$ film of PS-b-PMMA was deposited on the substrate by spin-coating a toluene-diluted solution, followed by annealing at 170°C for 24 hours. In order to employ this film as a template for nanodot or nanowire fabrication, the samples were exposed to ultraviolet (UV) light (HgXe with a $\sim 1.2 \text{ J}/\text{cm}^2$ fluence) for 15 minutes. The PMMA is degraded via a chain scission under UV irradiation whereas the PS is cross-linked and becomes insoluble. Rinsing with acetic acid then removes the PMMA phase, leaving an array of holes in the PS matrix. Then, a 5 nm thick layer of metal, Pt for example, was deposited onto the deposition mask by dc magnetron sputtering under an Ar pressure of 2.0 mT at ambient temperature. The formation of self-organized nanodots and nanowires is obtained by a lift-off process based mainly on O_2 plasma. The nanodots could for example be integrated in a capacitor or served as a hard mask to fabricate an ordered array of nanopillars.⁴

This technology was applied to form nanopillars in a multilayer made of a $\text{Si}/\text{Si}_{0.8}\text{Ge}_{0.2}$ $10/10 \text{ nm}$ superlattice epitaxially grown on a Si (100) substrate by reduced pressure CVD. Here, the Pt nanodots provided a hard mask and Cl_2/O_2 inductively coupled plasma (ICP) was used to anisotropically etch our Si/SiGe stacks. The entire processing sequence is schematically illustrated in Fig. 1.

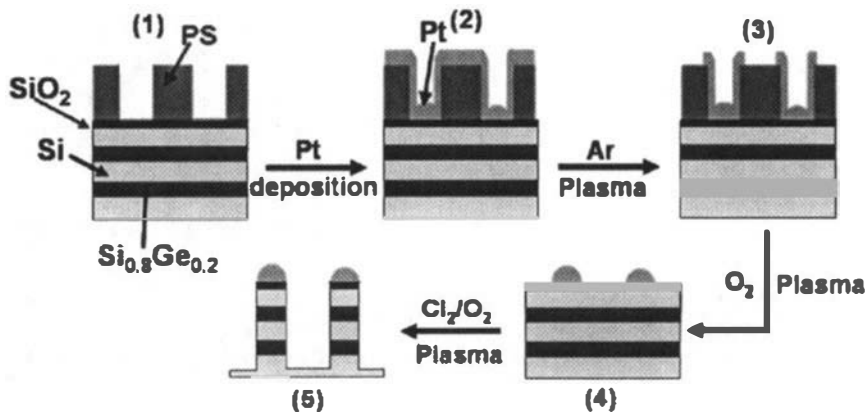


Figure 1. Schematic process flow for Pt dot fabrication by lift-off technique and realization of pillars by using Pt dots as a hard mask: (1) PS porous template on a $\text{SiO}_2/\text{Si}/\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}/\text{Si}_{0.8}\text{Ge}_{0.2}/\text{Si}$ multilayer; (2) Pt deposition onto the mask; (3) Ar plasma to selectively remove the metal in excess on top of the PS layer; (4) O_2 plasma to remove the residual polymer and side-walls metal-coated PS; and (5) etching the multilayer with a Cl_2/O_2 ICP plasma.

Figure 2 shows the nanopillars etched from a two-layer Si/Si_{0.8}Ge_{0.2} stack with a Cl₂/O₂ (180 sccm/25 sccm) ICP plasma during 15 s. The nanopillars have a cylindrical shape with the same height (~50 nm) and diameter (~20 nm). The Pt dots are still present after the etching step. This means that the increase of the O₂ flow rate in the etching gas limits the lateral etching of Si_{0.8}Ge_{0.2} quantum dots. Nevertheless, Fig. 2 shows that the diameter of the pillar is lower at the locations of the Si_{0.8}Ge_{0.2} layers. The significant decrease of the lateral etching of Si_{0.8}Ge_{0.2} layers with the increasing O₂ flow is due to sidewall passivation by an oxide layer.⁵ The thinner diameter of the Si_{0.8}Ge_{0.2} regions of the nanopillars is attributed to a thinner passivation layer than on the Si regions of the nanopillars. This effect was also observed by Monget *et al.*⁵ By analyzing the composition of the passivation layer by x-ray photoelectron spectroscopy (XPS), they determined that it contained Si, O, and Cl. As no Ge could be detected, they concluded that germanium etch products desorb into the gas phase without re-depositing on the sidewalls. This means that only silicon contributes to formation of the passivation layer, which is consequently thinner on the SiGe layers than on the Si layers.

In order to access to the physico-chemical nature of the nanopillars after the etching process, XPS measurements were performed on the samples (not shown). The Si spectrum shows two contributions at 99.6 eV and 104 eV, commonly attributed to Si-Si and Si-O bonds, respectively. The Ge 2p electronic level shows Ge-Ge and Ge-O contributions at 1218 eV and 1221.5 eV respectively.⁶ An interesting point to note here is that the 1221.5 eV peak corresponds to a completely oxidized Ge state⁷ with no significant sub-oxide. The presence of the Ge-Ge and Si-Si peaks shows that the Ge structure of the nanopillar is still present

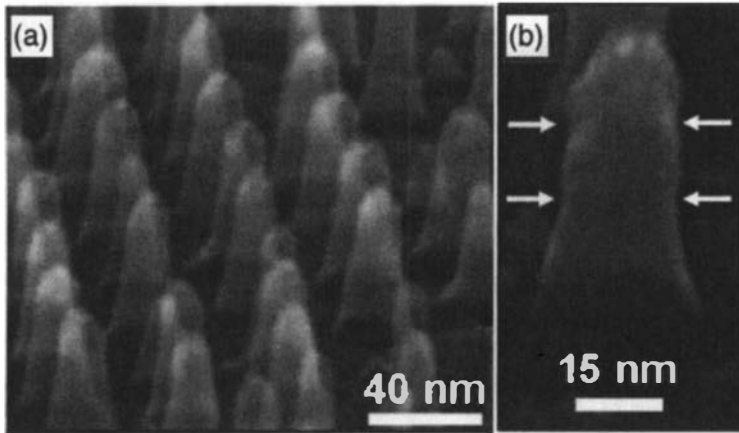


Figure 2. SEM images of pillars obtained by using the Pt dot array as an etch mask in a Cl₂/O₂ ICP etch process of Si/Si_{0.8}Ge_{0.2} 10/10 nm two-period superlattice on a Si substrate: (a) multiple pillars; (b) isolated ~50 nm tall pillar. The arrows in (b) indicate that the diameter of the SiGe layers is lower due to lateral etching.

after the etching, whereas the Ge-O and Si-O contributions are likely due to the sidewall passivation layers. The high reactivity of the oxygen radicals present in the gas phase during ICP explains the completely oxidized Ge state observed here.

3. Chemical vapor deposition of nanodots and nanowires

During the last few years, silicon quantum dots (Si-QDs) have been studied for nanoelectronics applications. Their unique physical properties, due to size confinement effects and Coulomb blockade phenomena, make Si-QDs suitable for use in new silicon based devices like single electron transistors⁸ or quantum dot floating gate memories.⁹ Low pressure CVD is a good way to obtain Si-QDs for industrial applications because of its MOSFET technology compatibility. By controlling the early stages of the Si film growth, silicon crystallites of nanometer size (5 nm) are obtained – a size that has proven of interest to nonvolatile memory devices.¹⁰ In order to obtain reliable devices, size, size uniformity and Si-QDs density must be controlled with a great precision and reproducibility. We have shown that a two-step CVD process makes it possible to control the QD size distribution while obtaining densities up to 10^{12} cm^{-2} – see Fig. 3.

Traditionally, Si nanowires (NWs) are grown using the vapor-liquid-solid (VLS) technique¹¹ where a metallic catalyst aids in the decomposition of a Si-containing gas. The metal and Si form a liquid eutectic droplet that moves along with the growing end of the wire as solid Si precipitates from the melt. Gold is the most frequently used catalyst because the Au-Si eutectic point occurs at a low temperature (363 °C).¹² We show that Si NWs can be grown with a solid-phase epitaxy process using fully CMOS-compatible catalysts: PtSi, NiSi, and PdSi.

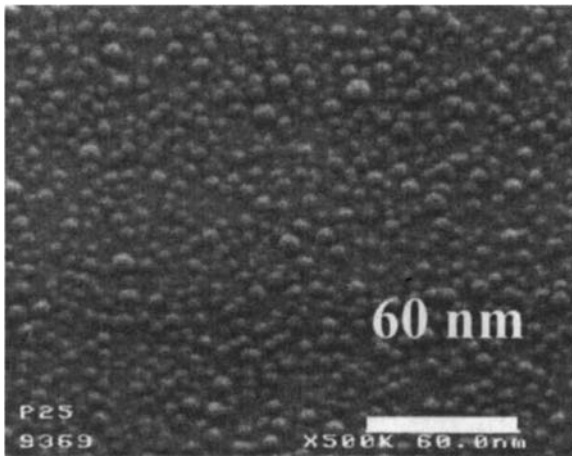


Figure 3. Typical SEM picture of Si nanocrystals after deposition on a SiO_2 surface: QD density is $\sim 10^{12} \text{ cm}^{-2}$, mean QD diameter is $\sim 8 \text{ nm}$.

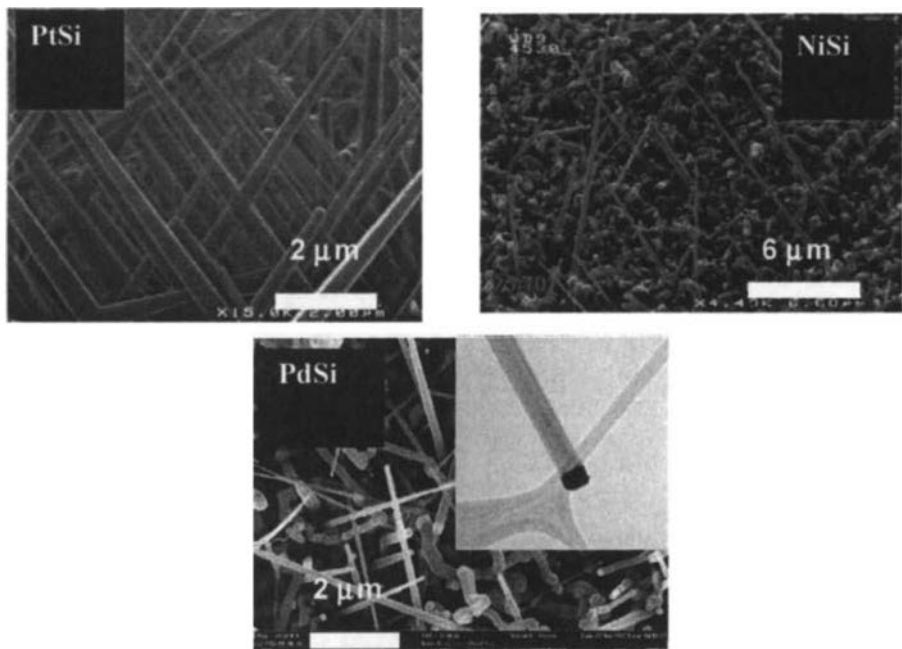


Figure 4. SEM picture of Si NWs obtained with different silicide catalysts: PtSi, NiSi and PdSi. The inset in the PdSi-catalyzed NW SEM shows a TEM analysis confirming the crystalline nature of the NWs.

Thus we have grown silicon nanowires by CVD using silicide catalysts and SiH_4 diluted in H_2 as the precursor gas. The resulting NWs are shown in Fig. 4. The growth temperature varied between 400 and 1000 °C, with silane fluxes in the 10–50 sccm range. Extra HCl gas could be added to favor catalytic growth.

4. Integration of nanoobjects

We have deposited Pt nanoparticles on *p*-type Si (100) substrate covered by a thin tunnel silicon dioxide (5 nm) via the diblock copolymer technology. This layer is integrated as a floating gate in a CMOS capacitor on an 8-inch pilot CMOS fab line. The density of nanoparticles was around 10^{11} cm^{-2} with the mean size centered around 20 nm. The Pt particles were covered by a 20 nm layer of SiO_2 deposited at low temperature. Aluminum was used as a metal gate. Figure 5 presents pictures representing the different steps of the process.

Capacitance-voltage characterization has been performed for devices with and without Pt nanodots. After a gate stress of 12 V during for 500 ms, a flatband voltage shift of about 1 V was only observed in devices with nanoparticles, indicating charge storage in the Pt nanocrystals.

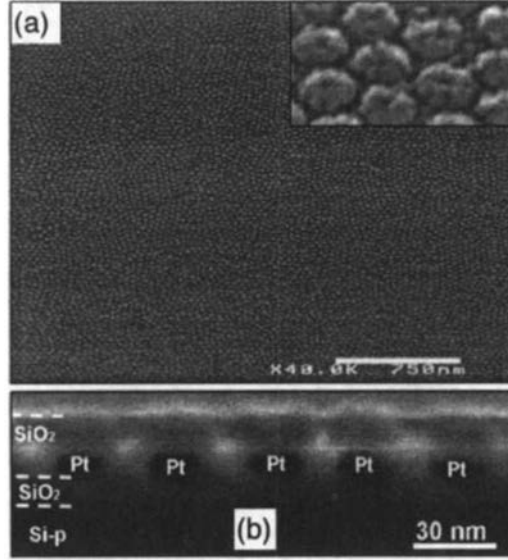


Figure 5. SEM pictures of the organized Pt nanocrystals: (a) top view; (b) cross-sectional view after the low temperature SiO₂ deposition.

Silicon NW field-effect transistors (FETs) were fabricated on thermal SiO₂ which is used as gate oxide and heavy *p*-doped Si substrate as back gate electrode – see Fig. 6. The source/drain electrodes were defined using photolithography, Ni/Al 120 nm/50nm metal deposition and lift-off. Through a controlled nickel silicide, the embedded parts of the undoped NWs are tuned into nickel silicide NWs, thus providing a direct metallic nanolead to the semiconducting nanowires and enhancing the device performance. The transistors obtained with NWs of ~100 nm diameter display *p*-type behavior, current densities around 2 kA/cm² and I_{ON}/I_{OFF} ratio up to 10⁷.

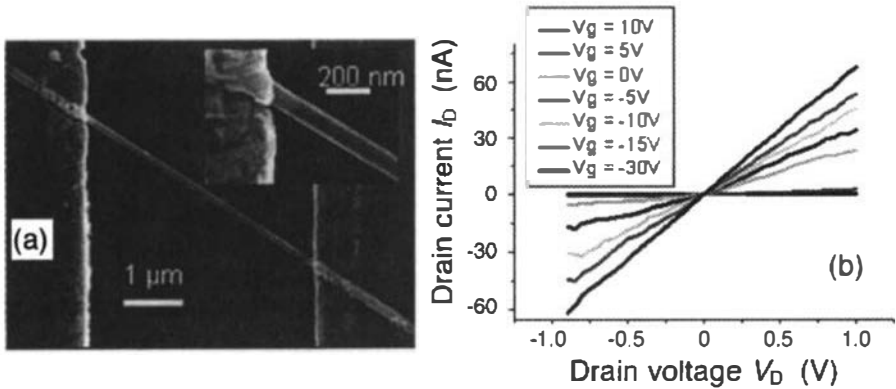


Figure 6. (a) SEM image of Si NW FET, the inset shows the axial silicidation of the Si NW; (b) output characteristics of the back-gated Si NW FET.

5. Conclusions

We believe that the fabrication technologies based on the bottom-up approach are promising to push forward the limits of conventional technology. Ordered arrays of dense nanostructures could be obtained and integrated in devices with CMOS process compatibility. Adding new functionalities to a CMOS integrated circuit via a 3D integration technology could enable new bottom-up applications.

Acknowledgments

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