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# Accurate Electromagnetic Simulation and Measurement of Millimeter-wave Inductors in Bulk CMOS Technology

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**Abstract**—In radio frequency integrated circuits (RFICs) that use a low resistivity silicon substrate, spiral inductors show advantages in performance and size with respect to transmission lines, even at millimeter-waves (mm-waves). Design guidelines to create mm-wave inductors and equivalent circuit models describing them exist in literature. However, these models need to be parametrized either from test-structure measurement or electromagnetic (EM) simulations. This paper complements previous work by discussing problems that arise when trying to accurately determine the spiral's parameters as inductance and quality factor. Firstly, it provides guidelines for obtaining accurate and consistent results using different kinds of EM simulators. Secondly, the issue of accurately measuring the fabricated inductors by de-embedding test structure parasitics is discussed. The results obtained from measurements are compared to the simulation results of an inductor test structure, confirming the validity of the considerations before.

**Index Terms**—mm-wave, inductor, spiral, on-chip

## I. INTRODUCTION

In the unlicensed frequency range around 60 GHz, the very first silicon RFIC designs used transmission lines for matching. They were followed by circuits based on spiral inductors that regularly exhibit superior performance and smaller size [1], [2], [3].

The design of mm-wave spiral inductors follows many of the guidelines developed for RFIC spirals at lower frequencies [4], [5]. Nevertheless, some modifications and extensions of these rules are necessary to get optimal spirals at mm-waves [6]. To characterize and improve the so-created inductors, EM simulations are essential [4]. They are more problematic at mm-wave frequencies, because skin depth  $\delta$  is much smaller compared to lower frequencies and substrate coupling is more pronounced. The first part of this paper deals with these simulation-related issues. After general considerations, it gives guidelines for the use of the inductance simulator ASITIC [7], the method-of-moment based planar EM software Sonnet V.12 (by Sonnet Software Inc.) and the finite element simulator HFSS V.12 (by Ansoft, LLC, a subsidiary of ANSYS, Inc.). The second part shows how to measure the inductors accurately, in order to confirm the EM simulation results.

## II. A TYPICAL MM-WAVE INDUCTOR

For the following considerations, the inductor test-structure of figure 1 is utilized. It is designed for the use in a 60 GHz CMOS low noise amplifier [3] and has a nominal value of 150 pH.

The spiral respects design guidelines for mm-wave spiral inductors found in literature:

- Only the topmost copper metal layer is used (thickness  $t=0.9\ \mu\text{m}$ )
- Narrow inductor width of  $w=3\ \mu\text{m}$  (upper limit is the horizontal skin effect, lower limit the electromigration rules or the partial quality factor  $Q_{\text{diff}}$  due to conductor loss [4],[6].)
- Inter-turn spacing is larger as required by design rules to reduce proximity effect ( $s=2\ \mu\text{m}$ )
- Small covered area (sidelength  $l=31\ \mu\text{m}$ ) to reduce substrate coupling
- Groundplane/Groundring around the inductor to reduce coupling between adjacent inductors in the final circuit [2], [6] and to provide a low loss, low inductance ground return path (cf. section III-B). A patterned ground shield is not used because it reduces the self-resonant frequency (SRF) due to increased capacitance to ground.

The inductor was fabricated in a 65 nm CMOS technology with seven copper layers and one aluminum pad layer. The substrate resistivity is  $15\ \Omega\text{-cm}$ .

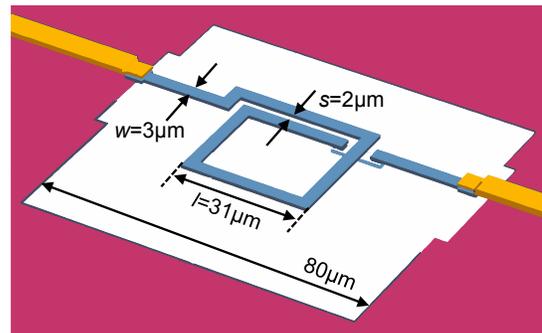


Fig. 1. 3D view of the inductor used for the following analyses

### III. INDUCTOR-SIMULATION

To accurately calculate the inductor's behavior, all kind of loss and coupling mechanisms have to be incorporated. Many of them are automatically taken into account, if the geometry and material properties are correctly entered to the EM software (like for example the magnetic and capacitive coupling between the turns of the spiral or the ohmic losses in silicon substrate). Depending on the solver type, some effects are neglected (ASITIC, for example, implements a quasi static solver and neglects substrate eddy currents. However, due to small inductor size ( $\ll \lambda/10$ ) and moderate substrate conductivity of 65 nm CMOS, these are negligible in the present case). The discussion in the following subsections concentrates on two important phenomena, namely the skin/proximity effect and currents in the grounding structure. They are essential for a correct simulation of the spiral inductors at mm-waves.

#### A. Skin and Proximity Effects

The skin effect in the conductor has always been an issue in RFIC inductor design [4]. However, the skin depth

$$\delta = \sqrt{\frac{2}{\mu\sigma\omega}} \quad (1)$$

in copper ( $\sigma = 5.8 \times 10^7 \text{ Sm}^{-1}$ ) at a lower frequency like 2 GHz is  $\delta_{2 \text{ GHz}} = 1.48 \text{ }\mu\text{m}$ , while at 60 GHz,  $\delta_{60 \text{ GHz}} = 0.27 \text{ }\mu\text{m}$  is obtained. Compared to the inductor thickness of  $t=1 \text{ }\mu\text{m}$ ,  $\delta_{60 \text{ GHz}}$  presents a worst case for simulation: at the one hand equivalent surface resistance models are not yet applicable because the inductor is not thick compared to the skin depth. At the other hand, a coarse mesh (or a two-metal model) inside the conductor, while sufficient at lower frequencies, is not fine enough to resolve the skin effect. Figures 2 and 3 illustrate the low skin depth inside the inductor.

In addition to that, a similar physical phenomenon leads to the proximity effect, if more than one inductor is implied. Its impact can also be observed in figures 2 and 3.

The extreme current distribution due to these effects needs to be respected by the EM simulation, otherwise conductor loss is not modeled correctly and even the inductance is slightly overestimated.

Accurate representation of these effects in the presented simulators is achieved in the following ways:

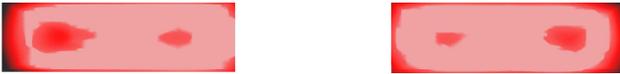


Fig. 2. Current displacement in the conductor cross section of the two turn side of the test inductor. Plot obtained by HFSS-simulation of the test-inductor, current density in logarithmic scale increasing to darker colors (see figure 3). The slightly higher current in the very inside of the metal is due to small simulation inaccuracies.

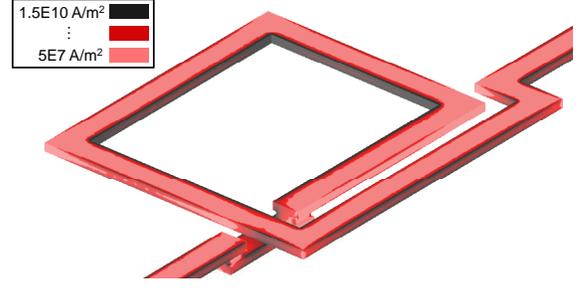


Fig. 3. Plot of the current densities on the conductor surface. Plot obtained by HFSS-simulation, current density in logarithmic scale increasing to darker colors.

1) *HFSS*: Meshing inside metals has to be activated. An iterative algorithm is used to refine the mesh. Besides the S-parameters' relative change  $\Delta S$ , other criteria like the effective quality factor  $Q_{\text{eff}}$  can be specified. In figure 4 convergence is illustrated in case of the test-inductor. An acceptable accuracy is achieved for about 120000 2nd order tetrahedra, showing the computational effort it takes to correctly simulate  $Q$ .

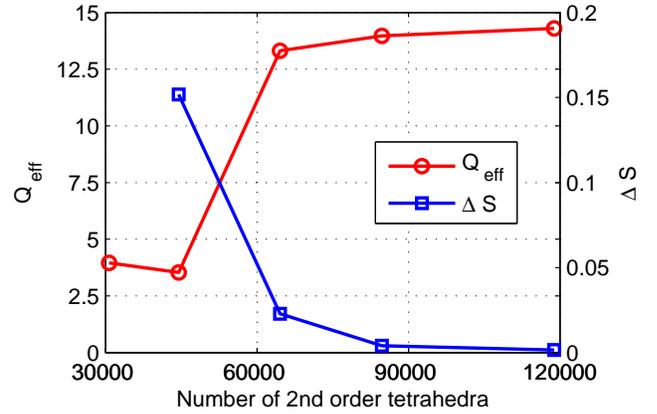


Fig. 4. Convergence of the adaptive mesh refinement process in HFSS

2) *Sonnet*: The thick metal model allows to discretize the inside of the metal by  $N$  layers, where  $N$  has to be chosen to obtain a resolution of several layers per skin depth. A convergence analysis helps to find out when  $Q$  factor accuracy is achieved (here  $N > 10$  in metal 7 for good accuracy).

3) *ASITIC*: The metal is modeled by the Partial Element Equivalent Circuits (PEEC) approach, where the metal is discretized in all dimensions. The above described effects are taken into account, if FFT size and the parameters  $\alpha$  and  $\beta$  (defined as  $t/\delta$ , set to  $\leq 0.3$ ) are correctly chosen.

In all solvers, meshing inside the conductor metal creates very large matrices. Their solution on personal

computers is a task that became possible only recently due to their increased computational power and memory.

### B. Ground Return Currents

A ground ring or even a ground-wall around the inductor is essential if coupling between the components in a circuit is to be avoided. To characterize the inductor in an environment close to the one encountered in the circuit, the grounding structure should be part of the simulation.

In figure 5 the currents in the grounding structure are

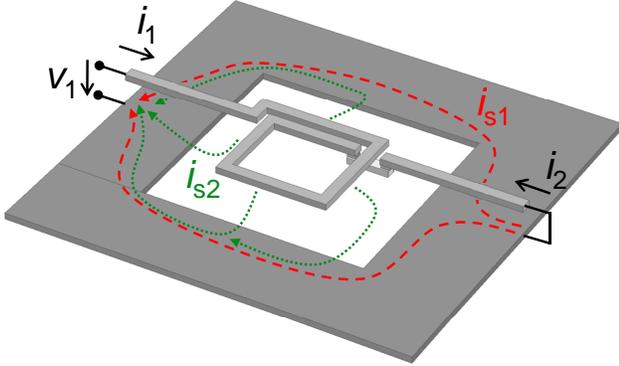


Fig. 5. Illustration of ground currents in a configuration used for the calculation of Y-parameters

illustrated. The short-circuit termination shown in this figure is the one for Y-parameter calculation, as inductance and effective quality factor are usually obtained from Y-parameters according to [6].

The return current  $i_{s1}$  takes the optimum path from the ground contact of port 2 to the ground contact of port 1. As the grounding structure has finite conductivity and non-zero dimensions, resistive loss  $R_{\text{gnd}}$  and inductance  $L_{\text{gnd}}$  is added to the inductor by this grounding structure. Approximations where these two grounds are at the same potential have to be carefully verified, especially at mm-wave frequencies. By optimizing the grounding structure,  $R_{\text{gnd}}$  and  $L_{\text{gnd}}$  can be greatly reduced.

Note that in circuits were many inductors and other devices are connected between the input and output port, the current  $i_{s1}$  is in general taking other ways as in the structure used to characterize the inductor. Thus in simulation of inductors it can be an option to remove  $L_{\text{gnd}}$  and  $R_{\text{gnd}}$  on device level and add these elements later on circuit level. The second current  $i_{s2}$  is created by capacitive coupling from the spiral to the grounded silicon substrate below. From the substrate it flows to the metal grounding structure and back to the exciting port. Note that the sooner this current reaches the grounding structure, the lower loss due to substrate resistivity is. However, approaching the ground ring too much reduces the inductor's SRF because of an increased capacitance to ground. Furthermore, eddy currents are induced in the ring structure, which increase

loss and thus lower Q. If loss and inductance created by  $i_{s1}$  and  $i_{s2}$  are taken into account depends mainly on the port excitation of the test structures:

1) *HFSS*: The excitation is done by wave ports. When no common, lumped ground reference is used, the ground conductors of port 1 and port 2 are distinct, and the loss and inductance of the grounding structure is taken into account according to its geometry and material properties.

2) *Sonnet*: Push-pull ports have to be used to achieve a differential excitation independent of the common ground. In this case, loss and inductance due to ground return currents are simulated according to geometry and conductivity. The grounding structure must not touch the sidewalls.

3) *ASITIC*: A grounding structure can be specified to fix a reference for capacitive substrate coupling, but its resistivity and inductance are not taken into account correctly. A differential excitation is not possible. Using ASITIC thus implies neglecting  $R_{\text{gnd}}$  and  $L_{\text{gnd}}$ .

## IV. INDUCTOR MEASUREMENTS

A die photo of the fabricated test-inductor is given in figure 6. The test-inductor plus parasitic access-structures are visible.

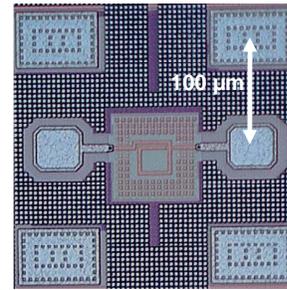


Fig. 6. Die photo of the inductor test structure

### A. Calibration and De-embedding

In order to obtain the intrinsic parameters of the inductor, first a short-open-line-thru (SOLT) calibration on a impedance standard substrate (ISS) is done using a vector network analyzer. It removes the error introduced by the measurement device up to the probe tips. Subsequently, a three step de-embedding procedure is applied to remove the access structure. The three elements to de-embed are the contact impedance  $Z_{\text{contact}}$ , the pad admittance  $Y_{\text{pad}}$  and the access line  $TL$ , as illustrated in figure 7. The de-embedding of  $Z_{\text{contact}}$  is necessary because of the difference in ohmic contact between the ISS and the aluminum pads of the CMOS chip [8].

The structures measured to obtain the elements of figure 7 are a  $147\mu\text{m}$  microstrip line and a  $246\mu\text{m}$  microstrip line including contact pads. First, the contact resistance is calculated by taking the difference of the two series

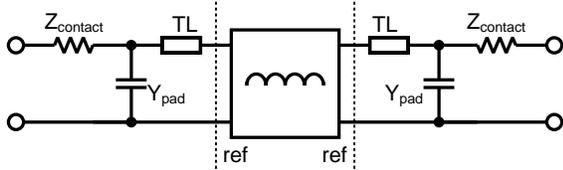


Fig. 7. Intrinsic inductor surrounded by elements to de-embed

impedances of the lines and scaling it to obtain the expected series resistance of the  $246\mu\text{m}$  line. The difference between expected value and measured value yields  $Z_{\text{contact}}$ . To obtain a good repeatability of the contact on aluminum pads, guidelines from [8] are respected.

The pad admittance and the parameters of the transmission line  $TL$  are obtained according to [9] using the above-mentioned microstrip lines. The parasitic elements  $Z_{\text{contact}}$ ,  $Y_{\text{pad}}$  and  $TL$  are removed from the inductor measurements using Y- and ABCD-representations of the inductor's two-port parameters.

## B. Results

In figure 8, both measurements and simulation of the effective quality factor  $Q_{\text{eff}}$  and differential inductance  $L$  of the test-inductor are shown. While the measured inductance value is reproduced with an accuracy of less than 5pH for Sonnet and HFSS, ASITIC's result lie slightly higher, probably because  $L_{\text{gnd}}$  is not taken into account.

The quite small discrepancy in  $Q_{\text{eff}}$  can be explained for one part by measurement tolerances, especially at high frequencies. The difference in corresponds to S-parameter differences of less than 0.1dB. At the other hand, the groundplane is considered to be homogeneous as shown in 1. However, due to design rules, a sophisticated pattern containing 2 metal layers is actually used. The equivalent thickness and conductivity of this groundplane is not known very well and can be decisive for accuracy at mm-waves.

## V. CONCLUSION

When designing spiral inductors for mm-wave RFICs, both simulation and measurements require special attention. This paper provides insight in two important phenomena, namely skin/proximity effect and ground return currents. Consequently, guidelines are given for the application of these insights to simulations of inductors in three popular EM solvers.

The accurate de-embedding of measurement results is also discussed. It allows to eliminate parasitic elements from the measured test structure and thus to obtain a good comparability to simulation results.

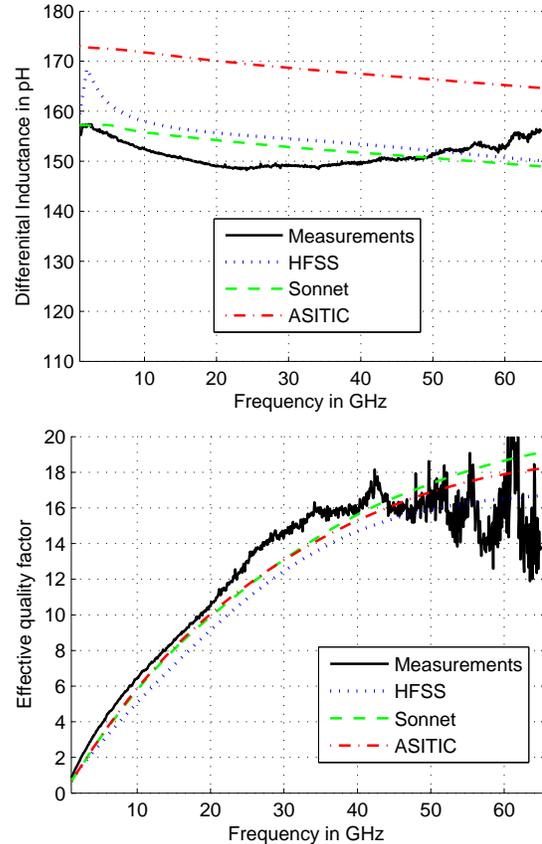


Fig. 8.  $L$  and  $Q_{\text{eff}}$  of the test-inductor

## ACKNOWLEDGMENTS

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## REFERENCES

- [1] D. Alldred, B. Cousins, and S. Voinigescu, "A 1.2V, 60-GHz radio receiver with on-chip transformers and inductors in 90-nm CMOS," in *IEEE CCSICS 2006*, Nov. 2006, pp. 51–54.
- [2] E. Cohen, S. Ravid, and D. Ritter, "An ultra low power LNA with 15dB gain and 4.4dB NF in 90nm CMOS process for 60 GHz phase array radio," *IEEE RFIC 2008*, pp. 61–64, April 2008.
- [3] M. Kraemer, D. Dragomirescu, and R. Plana, "A low-power high-gain LNA for the 60GHz band in a 65 nm CMOS technology," in *APMC 2009*, 2009.
- [4] J. Craninckx and M. Steyaert, "A 1.8-GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 5, pp. 736–744, May 1997.
- [5] A. Niknejad and R. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF ICs," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1470–1481, Oct. 1998.
- [6] T. Dickson, M.-A. LaCroix, S. Boret, D. Gloria, R. Beerkens, and S. Voinigescu, "30-100-GHz inductors and transformers for millimeter-wave (Bi)CMOS integrated circuits," *IEEE Trans. on MTT*, vol. 53, no. 1, pp. 123–133, Jan. 2005.
- [7] "http://rfic.eecs.berkeley.edu/niknejad/#asitic."
- [8] T. Kolding, "General accuracy considerations of microwave on-wafer silicon device measurements," in *IEEE IMS 2000*, vol. 3, 2000, pp. 1839–1842 vol.3.
- [9] A. Mangan, S. Voinigescu, M.-T. Yang, and M. Tazlauanu, "De-embedding transmission line measurements for accurate modeling of IC designs," vol. 53, no. 2, Feb. 2006, pp. 235–241.