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Václav VALENTA[1, 2], Martine VILLEGAS[2], Geneviève BAUDOIN[2]

[1] Dept. of Radio Electronics, Brno University of Technology, Purkyňova 118, 612 00 Brno, Czech Republic
[2] Université Paris-Est, ESYCOM, ESIEE, Cité Descartes, 93162 Noisy-le-Grand, France

valentav@esiee.fr, villegam@esiee.fr, baudoing@esiee.fr

Abstract. *This paper is focused on design aspects of a fractional-N PLL (Phase Locked Loop) based frequency synthesizer proposed for the Mobile WiMAX (Worldwide Interoperability for Mobile Access) standard. Requirements in terms of phase noise, settling time, frequency resolution and frequency of operation for WiMAX frequency synthesizer are presented. Furthermore, a high-speed CP (Charge Pump) PLL based synthesizer with a switched loop bandwidth is proposed and simulated. It has a 32 MHz reference frequency and a 50 kHz loop bandwidth with frequency raster of 125 kHz and 14 µs settling time.*

Keywords

Fractional-*N* frequency synthesizers, high-speed electronics, phase locked loops, phase noise.

1. Introduction

The IEEE 802.16 standard starts a real revolution in wireless communications, providing mobility and high-speed access to data, voice and video services. Throughput capabilities of wireless standards depend on the channel bandwidth. Unlike 2G and 3G wireless systems with a fixed channel bandwidth, the 802.16 WiMAX considers various channel bandwidths in a range from 1.25 MHz to 20 MHz, which offer very flexible deployment.

One of the most challenging blocks in a radio transceiver is the frequency synthesizer, which is generally a VCO phase-locked to a precise reference signal. This circuit is usually implemented with on-chip components like transistors, capacitors and resistors. Evaluation of the frequency synthesizer complexity relates to the WiMAX RF architecture. WiMAX considers three RF architectures, namely TDD, FDD and half FDD (HFDD). Since the TDD mode utilize one band for uplink and downlink direction, only one local oscillator is required. Contrary to the TDD, FDD mode requires two separate synthesizers for RX and TX due to the full duplex nature of the circuit and hence the switching requirements can be relaxed. Moreover, synchronization issues are alleviated compared to the TDD system. This fact results in simpler radio design, but on the other hand, it negatively affects the RFIC die area, cost of the circuit and the power consumption. This is one of the main reasons why the TDD is preferred for the mobile version of the WiMAX standard (802.16e). Moreover, TDD enables adjustment of the downlink and uplink ratio to efficiently support asymmetric traffic, while with FDD, the downlink and uplink always have fixed and generally equal channel bandwidths [2]. This article deals with design aspects of a synthesizer for the Mobile WiMAX standard, operating in a range of 3.4-3.8 GHz. We consider here initial certification profiles as defined by the WiMAX Forum, Release 1. Firstly, synthesizer requirements are presented. Furthermore, a fractional-*N* PLL based synthesizer with a switched loop bandwidth is proposed and simulated.

2. Synthesizer Requirements

A frequency synthesizer generates a local frequency that is mixed with the incoming RF signal to create a lower frequency signal that can be digitized and processed in the baseband IC. The frequency synthesizer has to provide all necessary frequencies for the down and up conversion with proper channel spacing that corresponds to the channel bandwidth or to the frequency raster. Frequency switching has to be performed agilely, with respect to settling time requirements of the standard. Moreover, the local frequency synthesizer has to fulfill the tightest signal purity requirements that can be expressed in terms of the integrated phase noise and the spurious output. These requirements given by the Mobile WiMAX standard are summarized in Tab. 1 [1]-[4].

Frequency Band [MHz]	Channel BW [MHz]	Settling Time[µs]	Phase Jitter [°rms]
2300-2400	5, 8.75, 10	< 50	< 1
2305-2320 2345-2360	5, 10		
2496-2690	5, 10		
3300-3400	5, 7, 10		
3400-3800	5, 7, 10		

Tab. 1. Mobile WiMAX Initial Certification Profiles.

It can be seen that the most critical synthesizer requirements are set in terms of the integrated phase noise and the settling time. The integrated phase noise is less than 1 deg rms with an integration frequency of 1/20 of the tone spacing (modulated carrier spacing) to ½ the channel bandwidth [4], [5]. Thus for smaller channel bandwidths the integration of the phase noise can start from as low as a few hundred Hertz. Moreover, the frequency synthesizer has to settle within less than 50 µs [6]. The minimum required frequency resolution is derived from the required channel raster, which is imposed by the Mobile WiMAX standard as 125 kHz. In order to settle and maintain this step size, fractional-*N* synthesizers must be considered. They can achieve very small frequency resolution equal to the fractional portion of the reference frequency and hence improve the phase noise performance by a factor of 20log (*N*) compared to the conventional integer-*N* PLL [7].

3. Frequency Synthesizer Architecture

Fractional-*N* synthesizers have become very popular and widely used in a range of RF applications due to the fact that they allow the reference frequency to be significantly higher than the required frequency resolution. Since the Mobile WiMAX standard defines the channel raster resolution as 125 kHz, the reference frequency of an integer-*N* synthesizer would have to be as low as 125 kHz and hence, the division *N* would reach up to 30400 in order to generate the highest frequency of 3.8 GHz. This would, in turn, deteriorate the reference phase noise contribution by a factor of 45 dB, compared to the fractional-*N* synthesizer with a reference frequency of 32 MHz.

In this paper, we consider a fractional-*N* CP frequency synthesizer. A simplified model is depicted in Fig.1. This model includes a tri-state PFD (Phase Frequency Detector) that produces output *up* and *down* signals, proportional to the phase and frequency difference between the reference and the feedback signal. PFD employs two positive edge-triggered resetable FF (Flip-Flops) to detect the phase and frequency difference and one AND gate to monitor the *up* and *down* signals. The upper FF is clocked by f_{ref}, the lower by f_{div}. Signals *up* and *down* are used to switch the current sources in the CP. These CP current pulses change the voltage drop on the loop impedance and tune the VCO with tuning gain of 125MHz/V and tuning range of 3.4-3.88 GHz.

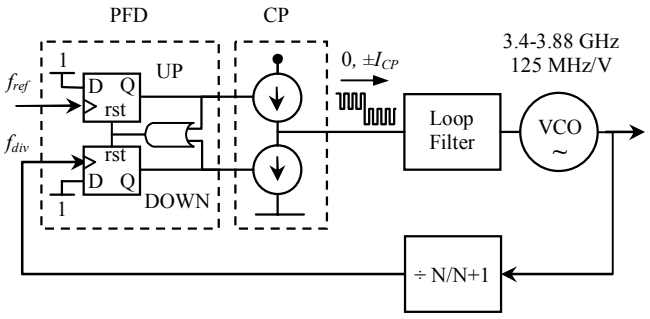


Fig. 1. A model of the fractional-*N* charge pump synthesizer.

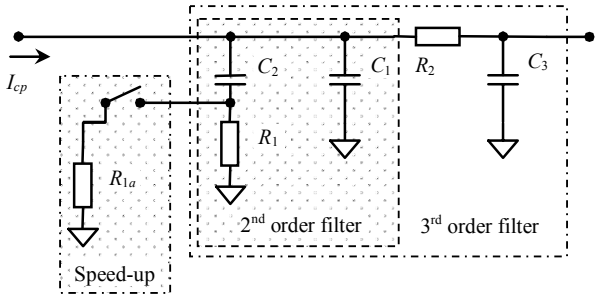


Fig. 2. A second and third order passive loop filter with the speed-up topology.

3.1 Speed-up Loop Filter Topology

Loop filter is the key component of the PLL that characterize the performance of the synthesizer. Loop filter design involves choosing the proper loop filter topology, loop filter order, phase margin and loop bandwidth. Due to the low phase noise requirements set by the Mobile WiMAX standard, a passive filter has been chosen. The tradeoff between the minimum loop bandwidth and the settling time has to be taken into account for optimal loop filter design. A simplified tradeoff presents [7] as $B_{PLL} = 4 / t_{lock}$, where t_{lock} is the settling time. Applied to WiMAX, the PLL would call for at least 200 kHz loop bandwidth in order to settle within 20 µs. However, such a wide PLL bandwidth would result in a higher in-band phase noise integration and phase jitter deterioration. Hence, a speed-up loop filter topology with a switched loop bandwidth has been proposed for the WiMAX transceiver.

The basic idea is to use a larger loop bandwidth during the frequency transition and then, after a certain programmable period, to shift the loop bandwidth to the normal value [7]. As depicted in Fig. 2, the speed-up mode is achieved when the CP current is increased by a factor of 16 ($I_{cp} \rightarrow 16 * I_{cp}$) while reducing the dumping resistance by a factor of 4 ($R_1 \rightarrow R_1/4$). So the PLL open-loop cross-zero frequency, the zero and pole frequency ($1/R_1C_2$ and $1/[R_1C_1C_2/(C_1+C_2)]$) are all increased by a factor of 4. The loop stability remains unaffected (see Fig. 3). The dumping resistance is reduced by a factor of 4 using an extra resistor R_{1a}. This resistor is chosen such that the parallel combination of the dumping resistor R_1 and the resistor R_{1a} equals to ¼ of the original value of the dumping resistor R_1.

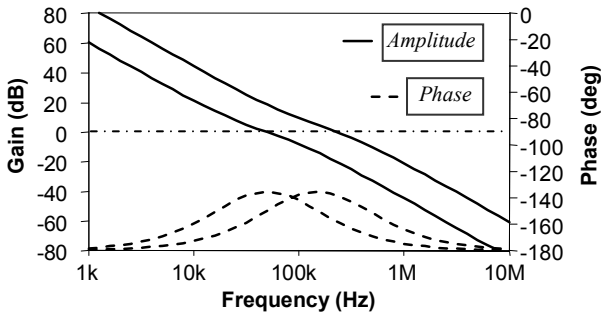
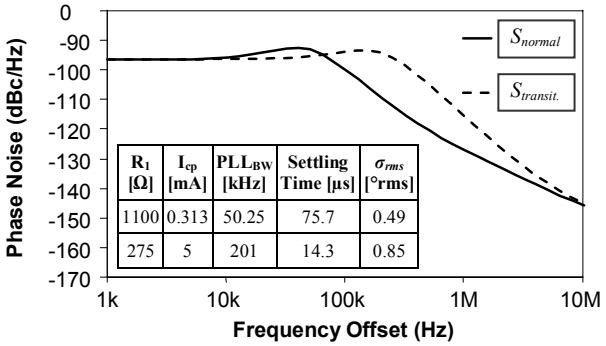


Fig. 3. Open loop gain for both PLL loop filters. Notice that the stability is unaffected (phase margin=constant=44.7°).



R_1 [Ω]	I_{cp} [mA]	PLL_{BW} [kHz]	Settling Time [µs]	σ_{rms} [°rms]
1100	0.313	50.25	75.7	0.49
275	5	201	14.3	0.85

Fig. 4. Phase noise performance at 3.59 GHz. Dashed line corresponds to the noise behavior at the PLL output during the frequency transition.

Figure 4 shows the phase noise performance at the central frequency of 3.59 GHz for two different loop filter adjustments. In this simulation, speed-up mode has not been enabled and the resistor R_{1a} has not been used. The inside table presents values of the dumping resistor R_1, charge pump current I_{cp} and the corresponding performance of the synthesizer in terms of the settling time and the integrated phase noise σ_{rms}. The integrated phase noise σ_{rms} has been calculated from 488 Hz to 5 MHz. This integration bandwidth corresponds to the channel bandwidth 10 MHz and FFT size 1024. Other passive loop components have not been changed.

It is evident that the integrated phase noise has risen in the second case due to the PLL bandwidth enlargement, but on the other hand, the settling time has dropped from 75.7 µs to 14.4 µs. This dual loop bandwidth constellation has been adopted in the speed-up mode, when the wideband loop is "switched on" during the frequency transition. The dumping resistance of 275 Ω has been replaced by the parallel combination of resistors R_1 and R_{1a} (1100 Ω and 365 Ω respectively). To determine the optimal moment to shift the loop bandwidth to the normal (narrow) value, following simulation has been carried out. Settling time has been monitored while changing the time spent in the wideband mode during the frequency transition. This time period has been calculated by the reference counter in terms of reference frequency cycles. One reference cycle equals to 31.25 ns ($1/32 \cdot 10^6$). This simulation has been carried out for second and third order filters. The result is presented in Fig. 5.

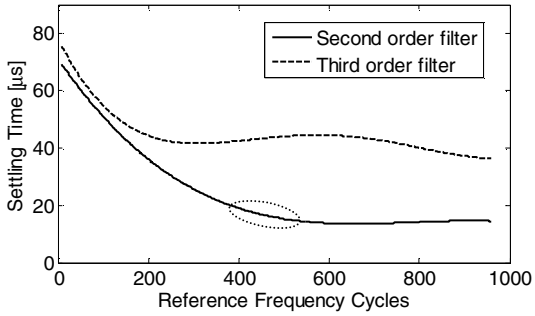
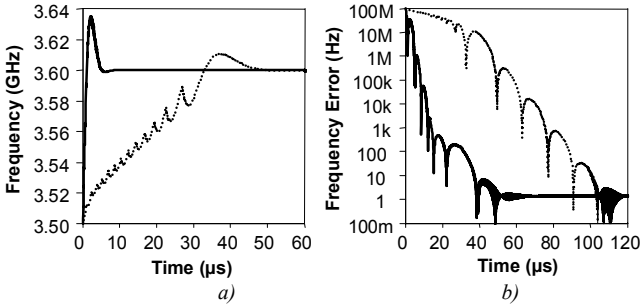


Fig. 5. Settling time as a function of time spent in the wideband mode. One cycle corresponds to one period of the reference frequency 32 MHz.



a) *b)*

Fig. 6. Transient responses of the PLL for two cases: speed-up mode enabled/disabled (solid/dotted line respectively). Plot *b)* displays the absolute frequency error in reference to the settling frequency of 3.6 GHz.

Let us have a look at the speed-up performance of the second order filter (solid line in Fig. 5), which exhibits better settling time compared to the third order filter. It can be seen that the major settling time improvement due to the speed-up mode occurs approximately within the first 425 reference cycles (ca. 13.3 µs). From this point onward, the settling time remains roughly constant and hence it is no more beneficial to stay in the wideband mode. This time period has been considered as the optimal time to switch the loop bandwidth to the normal value. Figure 6 shows the corresponding transient response of the PLL synthesizer that hops from 3.5 to 3.6 GHz. Moreover, the absolute frequency error in reference to 3.6 GHz is depicted in Fig. 6, plot *b)*. Notice that the PLL can settle with the maximal accuracy of 1 Hz. This error is caused by the leakage current that flows from the CP to the loop filter and causes undesired voltage drop that tunes the VCO. In this particular simulation, the 1-Hz uncertainty was caused by 1 nA leakage current. In addition to that, the leakage current contributes to reference and fractional spurs.

4. Loop Filter Phase Noise Analysis

Phase noise performance of a synthesizer is particularly important in OFDM based systems where it may easily break the orthogonality of sub-carriers. One consequence emerges from the self-mixing phenomenon, when the sub-carrier is mixed with the low frequency part of its own phase noise, resulting in sub-carrier rotation. This will affect all sub-carriers (so called common phase error). The second consequence results in an inter-carrier interference due to the mixing of the phase noise of all neighboring sub-carriers with the desired sub-channel. Inter-carrier interference becomes more important especially for high number of sub-carriers in the OFDM system and it results in BER degradation. The impact of the phase noise can be seen as a circular distortion of the signal point in the constellation diagram. Another negative impact of the phase noise emerges in receivers, during the reciprocal mixing [8]. There have been published several papers dealing with phase noise analysis of the PLL, considering noise contribution from all PLL elements (ref. oscillator, VCO, CP, PFD, divider) [7], [9]. This section deals with noise performance of the proposed loop filter.

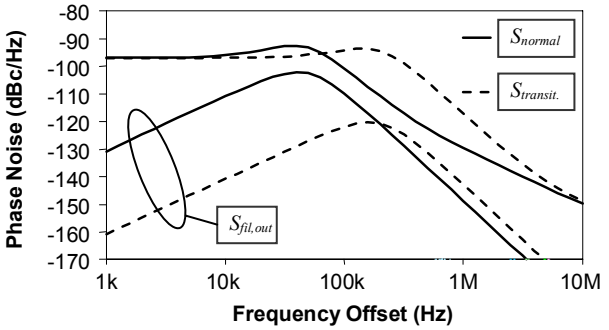


Fig. 7. Phase noise performance at 3.59 GHz in the speed-up mode. $S_{fil,out}$ is the phase noise contribution of the loop filter to the total phase noise at the output of the PLL.

A passive loop filter consists of only resistive and capacitive components. Hence, the output voltage noise is the result of the thermal noise present in the real part of the complex admittance of the loop filter. Two-sided PSD of current fluctuations is defined by the Nyquist equation as:

$$S_{fil}(f) \approx 2kT\,\mathrm{Re}(Y(f)), \tag{1}$$

where Y is the loop filter admittance that corresponds to the inverse filter transimpedance, k is the Boltzmann's constant $1.38 \cdot 10^{-23}$ J/K, T is the absolute temperature. Furthermore, this thermal noise is band pass filtered by the PLL [9]. The loop filter noise contribution $S_{fil,out}$ to the output of the PLL is depicted in Fig. 7 for both loop filter constellations. The PLL band pass filtering is noticeable.

Phase noise can also be expressed in the time domain as an integrated phase noise (rms phase jitter σ_{rms}) within the integration band defined by f_1, f_2.

$$\sigma_{rms}[^\circ] = \frac{180}{\pi}\sqrt{2\int_{f1}^{f2} S\ (f)df}\ , \tag{2}$$

where $S(f)$ corresponds to the total phase noise at the PLL output. Phase jitter has been calculated for all initial WiMAX channels within the band from 1/20 of the tone spacing to ½ the channel bandwidth (see Tab. 2). Moreover, the phase jitter was analyzed as a function of the phase margin (see Fig. 8). Notice, that the phase jitter exhibits a sharp rise in the third order filter. This is caused by the resistor R_2, which gets significantly higher and hence it contributes more noise to the PLL. Phase margin of 44.7° was chosen as the optimal value for this particular design as a compromise between the phase jitter, stability and the settling time.

Channel BW [MHz]	FFT Size	Integration Frequencies [kHz]	σ_{rms} [°rms] 2nd order filter	σ_{rms} [°rms] 3rd order filter
5	512	0.488 – 2500	< 0.49	< 0.56
7	512	0.684 – 3500		
8.75	1024	0.427 – 4375		
10	1024	0.488 – 5000		

Tab. 2. Phase Jitter Analysis for Mobile WiMAX channels.

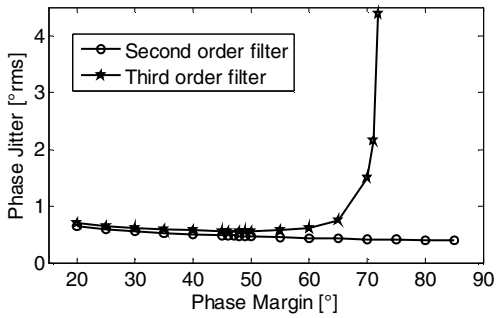


Fig. 8. Phase jitter as a function of the phase margin for the second and third order filter at 3.59 GHz.

5. Conclusion

A fractional-N frequency synthesizer for Mobile WiMAX has been proposed and simulated. It operates in the frequency band of 3.4-3.88 GHz and fulfills requirements imposed by Mobile WiMAX in terms of the settling time (14.4 μs), phase jitter (< 0.49°) and frequency step size (125 kHz). A significant enhancement of the settling time has been accomplished with help of the switched loop technique, which improved the settling time by 61 μs compared to the single narrowband loop.

Acknowledgements

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