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Study of a Modified Polar Sigma-Delta Transmitter Architecture for Multi-Radio Applications

Martha Liliana SUAREZ PENALOZA^{#1}, Václav VALENTA^{#*2}, Geneviève BAUDOIN^{#3}, Martine VILLEGAS^{#4}

[#]Université Paris-Est, ESYCOM, EA2552, ESIEE

2, Bd. Blaise Pascal - Cité Descartes BP99 - 93162 Noisy-le-Grand CEDEX, France

¹ suarezm@esiee.fr, ³ baudoing@esiee.fr, ⁴ villegam@esiee.fr

^{*}Dept. of Radio Electronics, Brno University of Technology

Purkyňova 118, 612 00 Brno, Czech Republic

²valentav@esiee.fr

Abstract— Polar Sigma Delta architecture has been previously proposed as a universal architecture able to offer multi-radio transmission for mobile systems. This paper describes polar sigma delta transmitter architecture and proposes modifications to it in terms of replacing analog mixing by digital mixing when recombining envelope and phase signals. Simulations of the modified architecture have been carried out for the mobile WiMAX standard. Impact of the frequency synthesizer on the performance of the architecture is also investigated considering the switched loop bandwidth topology. Results are presented and new architectures advantages and drawbacks are pointed out.

I. INTRODUCTION

Wireless communications systems including cellular communications, personal area networks (PANs), local area networks (LANs) and metropolitan area networks (MAN) have presented a considerable development in recent years and keep evolving constantly. Coexistence of different wireless standards on the same device is necessary to satisfy those users who expect mobility, ubiquitous connection and high data rates at the same time. This coexistence should not increase the size of the device or reduce the battery life.

Instead of including an independent architecture for each standard, universal transmitter architecture that is capable to generate all the different waveforms seems to be the best solution (namely in terms of consumed power and surface occupation). This concept is known as multi-radio transmitter.

At present, we envisage a cognitive multi-radio able to support existing wireless communications standards between 900 MHz and 6 GHz [1]. Multi-radio architecture should handle variations of all the considered standard parameters.

The next section will introduce the polar Sigma-Delta ($\Sigma\Delta$) transmitter architecture. Then, some possible modifications will be exposed and briefly analysed. Mobile WiMAX standard is introduced in Section IIIA, section IIIB presents the parameters chosen for the simulations and the digital mixing results. Finally, section IIIC briefly describes architecture of a frequency synthesizer and the impact on the modified polar $\Sigma\Delta$ transmitter.

II. POLAR SIGMA-DELTA ARCHITECTURES FOR MULTI-RADIO

Nowadays, different modulation types are proposed by wireless communication standards in order to reach high

throughput and mobility. Most of recent modulation techniques such as the orthogonal frequency division multiplexing (OFDM) and spread spectrum imply high envelope PAPR, increasing baseband and RF design complexity. Therefore, linearization methods or highly linear non-constant envelope architectures able to transmit high PAPR signals must be designed. In homodyne and heterodyne radio architectures linear backed-off power amplifier (PA) are typically used. However, transmitting variable envelope modulated signals by these common architectures results in reduction of the power efficiency. Linearity requirements increase with signal PAPR.

Architectures that use switched mode amplifiers are particularly interesting. 100% efficiency in switched power amplifiers is theoretically possible since the current and the voltage arises at different time intervals.

Some architectures that resort this principle have been previously proposed by different authors [1]. Two approaches have been proposed for polar $\Sigma\Delta$ transmitters, one by [2] and the other by [3]. In this paper we focus on the one proposed by [2], which uses a $\Sigma\Delta$ with variable output “-a” and “a”.

In the polar $\Sigma\Delta$ architecture, baseband signal is modulated according to the selected standard specifications (QPSK, m-QAM, OFDM, etc.). The resulting signal can be expressed by the complex envelope $z(t)$ as:

$$z(t) = z_I(t) + jz_Q(t) \quad (1)$$

$$\rho(t) = \sqrt{(z_I(t))^2 + (z_Q(t))^2} \quad (2)$$

$$\cos(\phi) = z_I(t)/\rho(t) \quad \text{and} \quad \sin(\phi) = z_Q(t)/\rho(t) \quad (3)$$

Then, the resulting envelope and phase signals are separated. The envelope signal (ρ) is modulated by a low-pass $\Sigma\Delta$ modulator and thereby transformed into a constant envelope signal as depicted in Fig. 1. Phase signals ($\cos(\phi)$ and $\sin(\phi)$) have constant envelope too. Envelope and phase signals are recombined and then RF modulated before the power amplification. Resulting signal has a constant envelope and hence amplifier linearity requirements are relaxed.

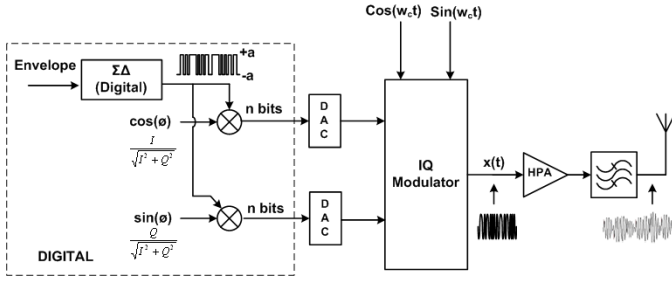


Fig. 1 Polar sigma delta architecture

Delay mismatch is not as severe issue as in the classical EER [1]. Amplified signal is finally filtered.

In this architecture, the output of the $\Sigma\Delta$ modulator is digital, as well as $Z_I(t)$ and $Z_Q(t)$ ($\rho\cos(\phi)$ and $\rho\sin(\phi)$). Therefore, two digital-to-analog converters (DAC) have to be employed before the IQ modulator as shown in Fig. 1. DACs sampling frequency is chosen relatively to the $\Sigma\Delta$ frequency. It has to be high enough in order to avoid the $\Sigma\Delta$ noise overlapping. Targeted communication standards in the multi-radio require high $\Sigma\Delta$ frequencies and therefore significant sampling frequency for DACs.

The polar $\Sigma\Delta$ transmitter could be used for multi-radio applications when the elements of the architecture are designed for the most restrictive communication standard parameters as suggested in [1].

A. Modified Polar Sigma Delta Architecture

Instead of decomposing the complex envelope signal into $\rho(t)$, $\sin(\phi)$ and $\cos(\phi)$, the second considered architecture (presented in Fig. 2) separates envelope and phase signals ($\rho(t)$ and $\phi(t)$) and processes them independently. In this case, the output of the low-pass $\Sigma\Delta$ modulator is analog. Digital phase signal is converted to analog and then modulated to the carrier frequency (f_c). Finally constant envelope and phase signals are recombined. The advantage of this approach compared to the first one is that only one DAC is required. Furthermore, DAC frequency requirements are mitigated.

In the polar $\Sigma\Delta$ architecture, the modulation to the carrier frequency is performed by the IQ modulator bloc with help of an analog mixer. Similarly, in the modified $\Sigma\Delta$ architecture an analog multiplier is used to recombine envelope and phase signals. The next architecture proposes to generate a digital carrier and then to change the analog mixer by a digital one, like an AND gate for example.

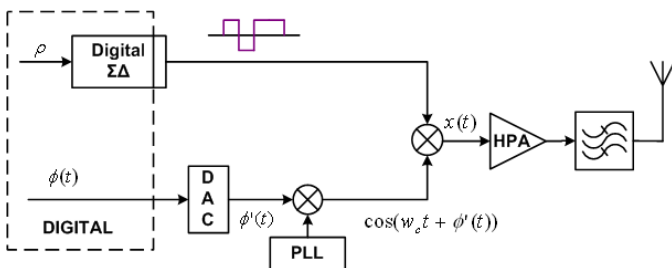


Fig. 2 Modified polar sigma delta architecture

B. Digital Mixing Polar $\Sigma\Delta$ Architecture

Fig. 3 presents the scheme of the digital mixing polar $\Sigma\Delta$ architecture. In this case, an All-Digital Phase Locked Loop (ADPLL) generates the carrier.

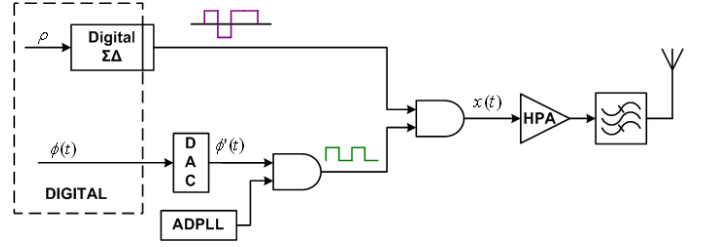


Fig. 3 Polar sigma delta architecture with digital mixing

The digital mixing approach in the $\Sigma\Delta$ architecture is very advantageous not only due to the nature of the digital signal processing, but it also offers better IC integration.

Synchronization between envelope and phase signals is a critical aspect in polar architectures. To overcome this problem, it is suggested in this third approach to use the same frequency generator for the ADPLL reference and for the $\Sigma\Delta$ modulator. This is a practical implementation because only one frequency generator is needed in the architecture. Modulated phase can be expressed as [4]:

$$\phi''(t) = \frac{1}{2} + \frac{2}{\pi} \cdot \sum_{n=1,3,\dots}^{\infty} \frac{1}{n} \sin(n(2\pi f_0 t + \phi(t))) \quad (4)$$

In the frequency domain, the multiplication of the $\Sigma\Delta$ modulated envelope and the modulated phase corresponds to the convolution operation. The output is centered on 0 , $3f_0$, $5f_0$... and the quantization noise introduced by the $\Sigma\Delta$ modulator is symmetrical around the carrier.

III. MODIFIED POLAR $\Sigma\Delta$ ARCHITECTURE SIMULATIONS

A. Mobile WiMAX technology

The IEEE 802.16e standard published in 2005 starts a real revolution in wireless communications, providing mobility and high-speed access to data, voice and video services. IEEE 802.16e considers various channel bandwidths in a range from 1.25 MHz to 20 MHz and offers throughput capabilities depending on channel bandwidth. This standard supports mapping according to the QPSK, 16-QAM or 64 QAM constellation scheme on the Orthogonal Frequency Division Multiplexing (OFDM) modulation. OFDMA air interface configuration is based on OFDM modulation and corresponds to the non line of sight operation in licensed frequency bands below 11 GHz. For this mode the possible FFT sizes are 2048, 1024, 512 and 128 [5]. Four primitive parameters characterize the OFDMA symbol: channel bandwidth (BW), number of used subcarriers including data and DC subcarriers (N_{used}), sampling factor (n) and cyclic prefix to useful time ratio (G) [5]. Channel bandwidths and the number of subcarriers are chosen depending on the targeted frequency band, channel conditions, capacity and the expected throughput. The n value

depends on BW. Supported values for the G are $1/32$, $1/16$, $1/8$ and $1/4$. The WiMAX Forum has published implementation profiles for the mobile WiMAX specifying frequency range, channel bandwidth and the FFT size [6].

B. Simulation of the Digital Mixing Polar $\Sigma\Delta$ Architecture

Simulations of a typical mobile WiMAX configuration have been conducted using Agilent Advanced Design Software (ADS).

Parameters has been chosen according to the WiMAX Forum implementation profiles as: carrier frequency = 3.7 GHz, BW = 10 MHz, $N_{\text{used}} = 841$ (FFT size is 1024), $n = 28/25$ and $G = 1/32$ (throughput is privileged) [6]. From these values and using the 64-QAM modulation to observe the highest PAPR, we calculated the raw symbol rate as specified in [5]. The resulting symbol rate is 9.079 MSymb/s. The $\Sigma\Delta$ modulator proposed by [2] was used for simulations, it is an order 2 low-pass Butterworth modulator with high stability.

Number of samples per symbol is one of the key factors to choose in order to respect the emission power mask defined by [7]. Moreover, required number of samples also determines the $\Sigma\Delta$ frequency ((symbol rate)/number of samples). As it was proposed before, if digital mixing is implemented, it is interesting to use the same frequency generator for the ADPLL reference and for the $\Sigma\Delta$ modulator. Since the carrier frequency is 3.7 GHz, the same frequency has been chosen for the $\Sigma\Delta$ modulator. This choice means that each symbol is sampled 408 times and this is enough to guarantee that the spectral mask is respected.

The $\Sigma\Delta$ modulator used in simulations has a digital output. Hence, to simulate a $\Sigma\Delta$ modulator with an analog output, an up-sample bloc is used in simulation. The choice of the up-sampling factor (uk) is related to the sampling frequency (f_s) for general architecture simulation ($uk = f_s / f_{\Sigma\Delta}$). In fact, in order to correctly observe the behavior of the system, the sampling frequency must be higher than twice the sum of the $\Sigma\Delta$ frequency ($f_{\Sigma\Delta}$) and the carrier (f_c) frequency [8].

$$f_s = k(f_c + f_{\Sigma\Delta}) \quad \text{with } k \geq 2 \quad (5)$$

The up-sampling factor has been chosen to be 2 and hence the simulation frequency is 14.8 GHz. The phase signal was also up-sampled by the same factor. Finally, the digital carrier was simulated with a 3.7 GHz square signal varying between 1 and -1. The resulting $x(t)$ signal has a constant envelope and its spectrum can be observed in Fig. 4.

As it can be observed from Fig. 4, the $\Sigma\Delta$ modulator output is replied each $3*f_c$ (11.1 GHz). From simulations it has been concluded that to avoid the spectrum overlapping in the digital mixing architecture, the carrier frequency must be equal or higher than the $\Sigma\Delta$ frequency. This is a condition that is not always easy to respect in a multi-radio system, because some communication standards may demand a very high over sampling ratio from the $\Sigma\Delta$ while their transmitting frequency is not high enough.

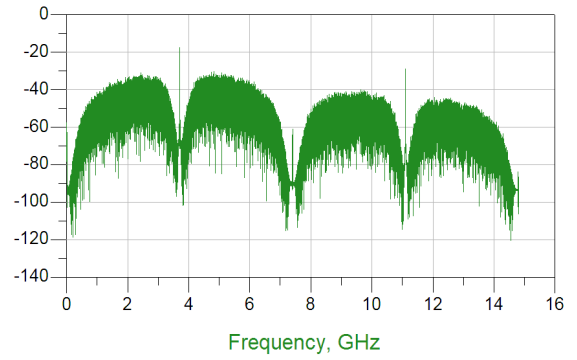


Fig. 4 Spectrum of the simulated signal ($f_c=3.7$ GHz)

This fact points out the importance of the correct evaluation of the relation between the signal bandwidth and the carrier frequency for each communication standard.

C. Frequency synthesizer architecture

From this point onward we will investigate the impact of the frequency synthesizer on the performance of the architecture presented in the section IIA. In the previous sections, an ideal frequency synthesizer has been considered.

Due to very high requirements given by the Mobile WiMAX standard, a PLL based fractional-N frequency synthesizer has been chosen. This architecture is capable to achieve very small frequency resolution equal to the fractional portion of the reference frequency and hence improve the in-band phase noise performance. More precisely, the minimum required frequency resolution of the synthesizer is derived from the required channel raster, which is imposed by the Mobile WiMAX standard as 125 kHz.

Frequency synthesizer presented in this paper considers the switched loop bandwidth topology that significantly improves the settling time performance [9] (see Fig. 5).

The local frequency synthesizer has to fulfil the tightest settling time and signal purity requirements that can be expressed in terms of the integrated phase noise (phase jitter) and the spurious output. These requirements given by the Mobile WiMAX standard are presented in Tab. I [9].

A simplified model of the synthesizer is depicted in Fig. 6. This model includes a tri-state PFD (Phase Frequency Detector) that produces output up and $down$ signals, proportional to the phase and frequency difference between the reference and the feedback signal. PFD employs two positive edge-triggered resettable FF (Flip-Flops) to detect the phase and frequency difference and one AND gate to monitor the up and $down$ signals.

TABLE I
MOBILE WiMAX CERTIFICATION PROFILES AND REQUIREMENTS.

Frequency Band [MHz]	Channel BW [MHz]	Settling Time[μ s]	Phase Jitter [$^{\circ}$ rms]
2300-2400	5, 8.75, 10	< 50	< 1
2305-2320	5, 10		
2345-2360	5, 10		
2496-2690	5, 10		
3300-3400	5, 7, 10		
3400-3800	5, 7, 10		

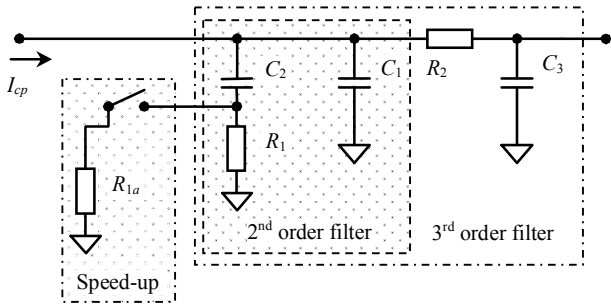


Fig. 5 A second and third order passive loop filter with the speed-up topology.

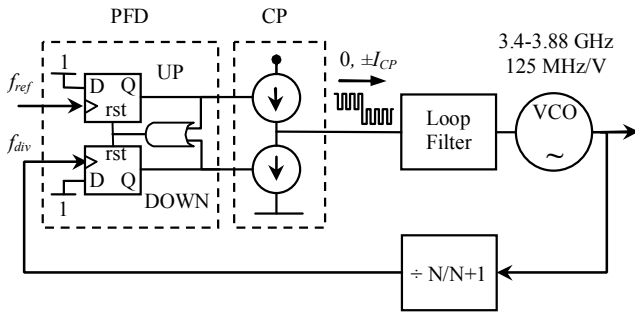


Fig. 6 A model of the fractional-N charge pump synthesizer.

The upper FF is clocked by f_{ref} , the lower by f_{div} . Signals *up* and *down* are used to switch the current sources in the CP. These CP current pulses change the voltage drop on the loop impedance and tune the VCO with tuning gain of 125 MHz/V and tuning range of 3.4-3.88 GHz.

The basic idea behind the switched loop bandwidth topology is to use a larger loop bandwidth during the frequency transition and then, after a certain programmable period, to shift the loop bandwidth to the normal value [9]. The speed-up mode is achieved when the CP current is increased by a factor of 16 ($I_{cp} \rightarrow 16 * I_{cp}$) while reducing the dumping resistance by a factor of 4 ($R_1 \rightarrow R_1/4$). So the PLL open-loop cross-zero frequency, the zero and pole frequency ($1/R_1 C_2$ and $1/[R_1 C_1 C_2 / (C_1 + C_2)]$) are all increased by a factor of 4. The loop stability remains unaffected. The dumping resistance is reduced by a factor of 4 using an extra resistor R_{1a} . This resistor is chosen such that the parallel combination of the dumping resistor R_1 and the resistor R_{1a} equals to $1/4$ of the original value of the dumping resistor R_1 .

Resulting phase noise of this synthesizer (at the carrier frequency 3.7 GHz) for both loop filter configurations is presented in Tab. II. Corresponding impact of the phase noise on the final constellation diagram is depicted in Fig. 7.

TABLE II

PHASE NOISE SPECIFICATION FOR A WiMAX FREQUENCY SYNTHESIZER

Frequency Offset (Hz)	1 k	10 k	100 k	1 M	10 M	100 M	1 G
Phase Noise 1 (-dBc/Hz)	96,90	96,90	94,20	117,10	148,70	159,60	159,60
Phase Noise 2 (-dBc/Hz)	96,90	95,90	100,50	129,60	149,60	159,60	159,60

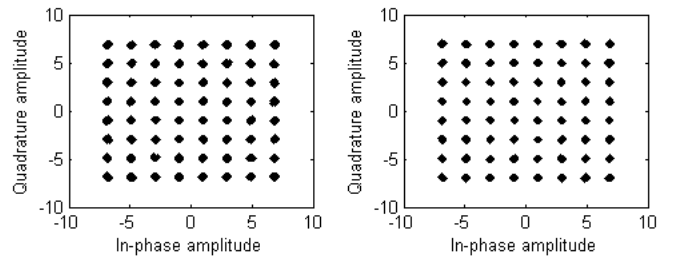


Fig. 7 Phase noise influence on the constellation diagram

IV. CONCLUSIONS

Two modifications to the polar $\Sigma\Delta$ transmitter architecture have been summarized in this article. Viability of using these architectures for multi-radio applications has been considered.

Communications standards require high over sampling ratio $\Sigma\Delta$ and this means high $\Sigma\Delta$ frequencies. This paper points out that if digital mixing is implemented in the polar $\Sigma\Delta$ architecture, frequency ratio between carrier frequency and the $\Sigma\Delta$ frequency has to be carefully chosen in order to avoid $\Sigma\Delta$ noise overlapping.

The proposed architecture of the frequency synthesizer fulfills the requirements of the mobile WiMAX standard in terms of the settling time and the phase jitter. Influence on the modified polar $\Sigma\Delta$ architecture performance has been discussed as well.

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