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Phase Noise Behaviour of Fractional-N Synthesizers with ΔΣ Dithering for Multi-Radio Mobile Terminals

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***Abstract*— This paper presents phase noise behaviour and design aspects of PLL based frequency synthesizers with ΔΣ dithering for cognitive multi-radio mobile terminals. Principal features of PLL based frequency synthesizers and 1-bit ΔΣ dithering are presented and simulated. Moreover, frequency synthesizer requirements for main standards in the frequency band 800 MHz to 6 GHz are investigated as well.**

I. INTRODUCTION

During the recent past, there has been a significant progress in wireless communications in terms of integration of various communication standards into a single mobile terminal. Instead of using multiple transceivers for different standards, the goal is to employ a single reconfigurable radio transceiver that is able to achieve all requirements of different communication standards. The goal of this evolution is to reduce the number of external components and to increase the integration in the low-cost CMOS technology. Another stage which pursues the evolution towards the cognitive radio and implies flexibility of each stage of the communication chain is the cognitive multi-radio. Cognitive multi-radio has the capability of the multi-standard concept and moreover it is capable to perform an efficient environment spectrum scanning in order to switch accordingly to an appropriate communication standard.

Single chip radios that support WLAN 802.11 a/b/g standards have already been proposed in [1], [2]. Another example of integration of cellular standards GSM 900/1800 and UMTS in a single chip can be found in [3]. These multi-radio proposals are mainly based on the direct conversion technique which is the most suitable techniques for 2G, 3G and 4G multi-radio terminals [4]. This is due to the fact, that the direct conversion eliminates the sensitivity to the image frequency and hence, it is not necessary to build any additional filters for the image rejection. One of the most challenging tasks in the multi-radio transceiver is the design of the frequency synthesizer. Frequency synthesizer has to provide all necessary frequencies for the down and up conversion with proper channel spacing that corresponds to the channel bandwidth and the raster of the communication standard. Frequency switching has to be performed agilely, with respect to the standard settling time requirements. Moreover, the local frequency synthesizer has to fulfil the tightest signal purity requirements which can be expressed in terms of the phase noise and the spurious output. These requirements given by the most diffused standards in the frequency band 800 MHz to 6 GHz, namely by GSM, UMTS, Bluetooth, WiFi and WiMAX, are summarized in Table 1 [5]-[9].

It can be seen, that the most critical local oscillator requirements in terms of the phase noise are imposed by the GSM standard. This is due to the fact that the powers of the in-band unmodulated interfering signals, so called blockers, are at very high level [10].

TABLE I. RF SPECIFICATIONS FOR THE MULTI-RADIO FREQUENCY SYNTHESIZER

Standard	Frequency Band [MHz]	Channel / Raster [MHz]	Settling Time[μs]	Phase Noise [dBc/Hz]
GSM 900/1800	880-960 1710-1880	0.2/0.2	577 150 (GPRS)	-122@0.6 MHz -132@1.6 MHz -139@3 MHz
UMTS FDD/TDD	1920-2170 1900-2025	5/0.2	200	-132@3 MHz -132@10 MHz -144@15 MHz
Bluetooth	2402-2480	1/1	150	-84@1 MHz -114@2 MHz -129@3 MHz
Mobile WiMAX IEEE 802.16e	2300-2400 2305-2320 2469-2690 3300-3400 3400-3800	3.5-10 / 0.25	< 100 (HFDD)	Phase Jitter < 1° rms
WiFi IEEE 802.11a	5150-5350 5470-5825	20/20	500	-102@1 MHz -125@25 MHz
WiFi IEEE 802.11b	2412-2472	20/5	225	
WiFi IEEE 802.11g	2412-2472	20/5	225	

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Various approaches for multi-radio frequency synthesizers have been proposed in [11]-[13], considering wideband tuning range VCO, use of multiple PLL loops or all digital PLL design. Although there are many techniques for frequency synthesis, the dominant technique used in wireless technology is based on the PLL principle. This technique is considered in this article. First, a linearized PLL model is described along with characteristic transfer functions. Furthermore, noise sources in the ΔΣ fractional-*N* PLL circuit are studied and simulated.

II. PLL ARCHITECTURE

A. PLL Linearized Model

Figure 1 displays a model of the ΔΣ fractional-*N* PLL. This model includes a charge pump phase-frequency detector CP/PFD with the gain K_d, a loop filter with the transfer function $F(s)$, a VCO with the gain K_0/s and a frequency divider dividing by *N*. The gain K_d can be written as follows:

$$K_d\,[A/rad] = I_{cp}/2\pi\,. \tag{1}$$

The charge pump current I_{cp} is proportional to the phase error in the phase detector and after low pass filtering by $F(s)$, it is applied to the control input of the VCO. In a conventional PLL, the frequency at the PLL output equals $f_{ref}N$. Divide ratio *N* can be an integer or a fractional value. In a fractional-*N* divider, the fractional division is achieved by periodic altering the division value between two integer values *N* and *N*+1, hence the average division becomes a fraction. However, the periodic switching between two division values leads to a sawtooth phase error which creates several spurious fractional tones. This problem is solved with help of ΔΣ modulator, which randomize the division ratio in the PLL but on the other hand, it introduces quantization noise into the loop as described in Section III.

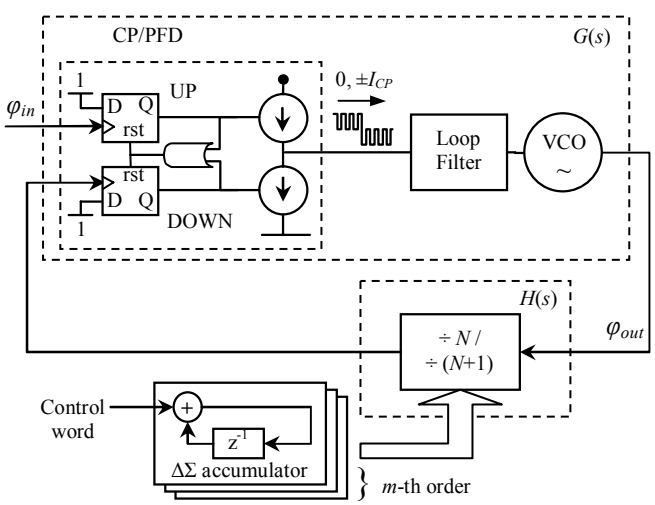

Figure 1. A Simplified model of fractional-*N* PLL frequency synthesizer with ΔΣ modulator that controlls the division ration of the divider.

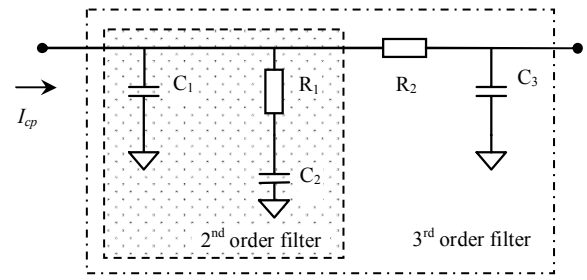

Figure 2. Second and third order passive filter.

According to the control theory, the effect of a closed feedback loop on the input signal φ_{in} can be described by the closed loop transfer function $T(s)$ as:

$$T(s) = \frac{\varphi_{out}(s)}{\varphi_{in}(s)} = \frac{G(s)}{1+G(s)H(s)} = \frac{\frac{K_d K_0}{s}F(s)}{1+\frac{K_d K_0}{s}F(s)\frac{1}{N}}, \tag{2}$$

where the $G(s)$ represents the forward transfer function and the term $G(s)H(s)$ open loop transfer function. $H(s)$ corresponds to the division factor $1/N$. Since the input signal at the loop filter is a charge pump current I_{cp}, the filter transfer function represents the transimpedance. The transimpedance of the 2nd order filter shown in Fig. 2 reads:

$$F(s) = \frac{1+sC_2R_1}{s(C_1+C_2)\left(1+s\frac{C_1C_2R_1}{C_1+C_2}\right)}\,. \tag{3}$$

In order to boost the reference spur suppression at the output of the PLL, additional RC low pass stages can be added [14]. However, additional passive components will contribute to the total phase noise at the output of the PLL.

III. PLL PHASE NOISE SOURCES

Phase noise performance of the frequency synthesizer is very important issue for many applications, notably for OFDM systems. The phase noise phenomenon in the PLL is a result of the thermal noise, shot noise, $1/f$ noise in all the active or passive components. Hereafter, we will analytically describe the phase noise behavior in the PLL circuit for the following noise sources: reference oscillator noise, VCO noise, loop filter noise and ΔΣ quantization noise.

A. Reference Noise

Reference oscillator's phase noise performance has been predicted with help of the Leeson's model [15] as:

$$S_{ref}(f_m)[dBc/Hz] = 10\log\left[\frac{FkT}{2A}\left(1+\frac{1}{f_m^{\,2}}\left(\frac{f_O}{2Q}\right)^2\right)\left(1+\frac{f_f}{f_m}\right)\right], \tag{4}$$

where f_m is the frequency offset, F represents the noise figure of the oscillator's amplifier, k is the Boltzmann's constant $1.38 \cdot 10^{-23}$ J/K, T is the absolute temperature, A is the power available to the amplifier from the resonator, Q is the loaded quality factor of the resonator, f_O is the carrier frequency and f_f is the flicker corner frequency. According to Fig. 1, the transfer function of the reference oscillator's noise S_{ref} injected at the input of the PLL corresponds to the low-pass filter function G_{LPF} with a loop bandwidth B_{PLL}. B_{PLL} is the frequency at which the open loop gain magnitude equals 1. Phase noise contribution $S_{ref,out}$ from the reference oscillator to the PLL output becomes:

$$S_{ref,out}(f) = S_{ref}(f)\left(\frac{1}{H(f)}\right)^2 \left|\frac{G(f)H(f)}{1+G(f)H(f)}\right|^2 = S_{ref}(f)N^2\left|G_{LPF}(f)\right|^2. \quad (5)$$

Fig. 3 demonstrates that the reference noise is low-pass filtered and hence the phase noise contribution at the PLL output becomes dominant at lower frequency offsets. Moreover, the reference phase noise is amplified by factor N, which is in this example equal to 2439 (≈67.8 dB). In order to keep low in-band phase noise, the division factor should be set as low as possible. This problem is solved by fractional-N dividers that can provide arbitrary small frequency resolution without the need of low reference frequency. Hence, the in-band phase noise performance is improved significantly [5].

B. VCO Noise

VCO phase noise S_{VCO} was modeled according to the Leeson's model as in (4). The transfer function is calculated similarly as in the reference noise case. The noise injected this time at the output of the VCO is high-pass filtered and hence the contribution of this noise to the PLL output reads:

$$S_{VCO,out}(f) = S_{VCO}(f)\left|\frac{1}{1+G(f)H(f)}\right|^2 = S_{VCO}(f)\left|G_{HPF}(f)\right|^2. \quad (6)$$

Due to the high-pass filtering, the VCO's phase noise will be suppressed within the loop bandwidth B_{PLL} and the dominant noise contribution will appear at higher frequency offsets. This phenomenon is depicted in Fig. 4.

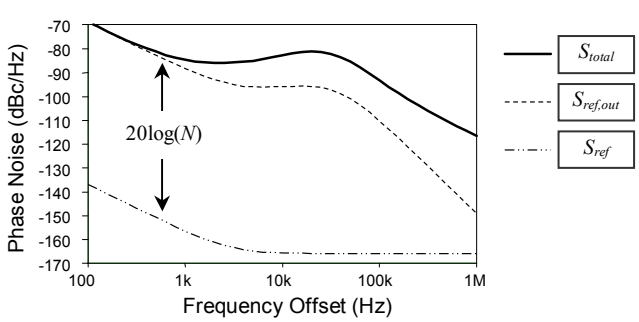

Figure 3. Reference oscillator's noise performance at the input and at the output of the PLL. Moreover, total phase noise at the PLL output is shown.

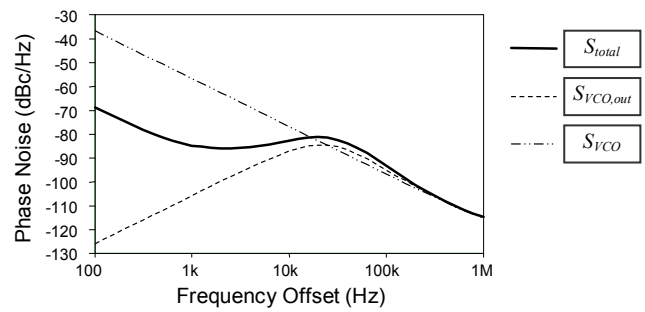

Figure 4. VCO's noise performance for open and closed loop case.

Furthermore, the out-band phase noise will drop to the VCO's noise floor which is defined by the oscillator's output power A and the system's noise figure F. Total integrated phase noise at the output of the PLL can be minimized by means of B_{PLL} reduction, however this will lead to settling time degradation. Hence, the tradeoff between the minimum loop bandwidth and the settling time has to be taken into account for design. A simplified tradeoff has been presented in [5] as $B_{PLL} = 4 / t_{lock}$, where t_{lock} is the settling time.

C. Loop Filter Noise

A passive loop filter consists of only resistive and capacitive components. Hence, the output voltage noise is the result of the thermal noise present in the real part of the complex admittance of the loop filter. Two sided PSD of current fluctuations is defined by the Nyquist equation as:

$$S_{fil}(f) \approx 2kT\,\mathrm{Re}(Y(f)), \quad (7)$$

where Y is the loop filter admittance that corresponds to the inverse filter transimpedance $1/F(f)$. Furthermore, this thermal noise is band-pass filtered (see Fig. 5) by the PLL and the noise contribution to the output of the PLL reads:

$$S_{fil,out}(f) = S_{fil}(f)\left|F(f)\right|^2\left|K_0 / j2\pi f\right|^2\left|G_{HPF}(f)\right|^2. \quad (8)$$

Fig. 5 shows the loop filter noise contribution to the PLL output for two values of the CP current. If the CP current is increased while keeping the same PLL transfer function, the thermal noise will be reduced since the loop filter resistor becomes smaller in order to keep the same output voltage.

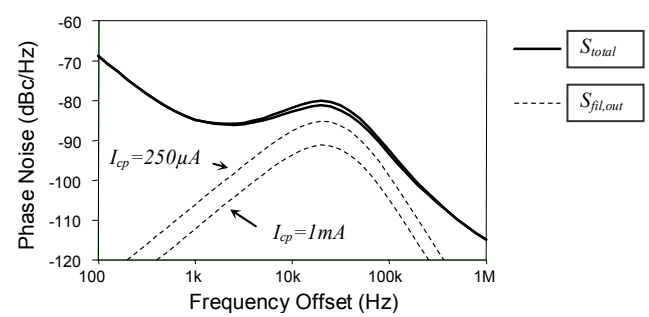

Figure 5. Noise contribution of the 2nd order filter for two values of I_{cp}.

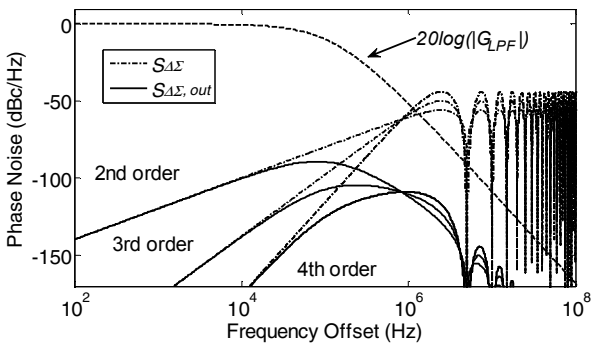

Figure 6. Noise spectrum induced by the 2nd, 3rd and 4th order ΔΣ modulator (dash dot) and the noise spectrum at the PLL's output (full line).

D. Quantization Noise from ΔΣ Modulator

The ΔΣ modulator used in a synthesizer is to randomize the instantaneous division ratio and hence push phase noise associated with the divider from low frequencies to high frequencies [16], see Fig. 6. The spectrum of the quantization noise $S_{\Delta\Sigma}$ is described for m-th order ΔΣ modulator as [17]:

$$S_{\Delta\Sigma}(f)[\mathrm{rad}^2/Hz] = \frac{(2\pi)^2}{12F_{ref}}\left[2\sin\left(\pi f/F_{ref}\right)\right]^{2(m-1)}. \qquad (9)$$

We consider the quantization noise $S_{\Delta\Sigma}$ to be injected before the frequency divider N/N+1. Hence, the noise transfer function of the phase corresponds to the low-pass transfer function G_{LPF} as derived in equation 5. Furthermore, the noise contribution to the output of the PLL reads:

$$S_{\Delta\Sigma,out}(f) = S_{\Delta\Sigma}(f)\left|\frac{G(f)H(f)}{1+G(f)H(f}\right|^2 = S_{\Delta\Sigma}(f)\left|G_{LPF}(f)\right|^2. \quad (10)$$

Notice the 20, 40 and 60 dB/decade slopes for the 2nd, 3rd and 4th order of the ΔΣ modulator respectively. Higher ΔΣ order provides better spurious suppression. Moreover, it can be seen that the ΔΣ modulator of higher order contributes less quantization noise close to the carrier, but on the other hand, it adds more noise to the PLL's output at higher frequency offsets (around 12 dB difference between the 2nd and the 4th order at higher frequency offset).

IV. Conclusion

In order to meet demanding synthesizer requirements for considered standards, understanding of the phase noise behavior in PLL based synthesizers becomes critical. We have presented phase noise behavior of PLL components, including noise sources of the reference oscillator, VCO, loop filter and quantization noise of the ΔΣ modulator. It has also been shown that the noise contribution of the loop filter can be reduced by means of the charge pump current optimization and by optimizing values of loop filter components. In this particular simulation, the noise contribution was reduced by 6 dB.

Moreover, frequency synthesizer requirements of the most diffused standards in the frequency band 800 MHz to 6 GHz have been presented as well. The most challenging synthesizer design issues are dictated by GSM and WiMAX standards. More precisely, GSM standard with very straighten phase noise requirements due to large allowed interferers and WiMAX standard due to very low settling time. Due to diverse requirements of considered standards, a multiple frequency synthesizers or reconfigurable loop filter might be considered. The most promising techniques include fractional-N ΔΣ approach which offers a significant improvement over integer-N synthesizers and it provides low phase noise performance and small step size which is indispensable for future cognitive multi-radio terminals.

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