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Keywords

<<JFET>>, <<Silicon Carbide>>, <<Voltage Source Converter>>

Abstract

JFET are experimentally stressed to provide data for modelling, inverter and driver design. The experimental set-up is described. A surge generator is built and a SiC JFET is stressed. During the stress, a temperature estimation is done at increasing time steps, in order to obtain the full thermal response versus time.

Introduction

SiC JFET inverters have been presented at various conferences over the last few years. High temperature and high power densities were the main subjects. A paper from SiCED [4], states the ruggeness of the devices when submitted to repetitive avalanche. Short-circuit and over load behaviour as also been studied in [2]. In some applications the inverter output conductors might be struck by lightning induced over-voltage. The modelling of lightning induced over-voltages is developped in ref [6].
This work focuses on SiC JFETs under lightning-induced over-voltages according to standards : CEI 801-5 Electromagnetic compatibility of electrical equipment, Part 5, class 3 (latest reference is CEI 61000-4-5). The JFETs are studied in the electrical environment of a voltage source inverter. We have developped a surge generator and a method to estimate the internal temperature of the JFET by using thermo-sensitive electric parameters. The novelty of the paper is the experimentation with JFET carying much more current than the channel saturation current. In such conditions, standard models are out of range and thermal behaviour must be taken into account. This paper describes an experimental setup to provide data for electro-thermal modelling of the JFET under overload.

Lightning surge generator

The european standard for electromagnetic compatibility of electric and electronic equipments [3] states the references for the normative lightning-induced overvoltages. A so-called 1.2/50μsec pulse, is used in our experiment with a peak voltage of 2kV (open load) and a maximum current of 120A (short-circuit). These values have been verified by simulation and measured experimentally on the prototype generator, see figure1. For information purposes here are the values used in the generator : C=5uF, L=50uH, R1=16.5Ω, R2=11Ω and R3=66Ω. K1 is a high voltage IGBT driven through a fiber-optic link, L1 is an air-coil inductor to get saturation-free operation. The generator circuit and the pre-charge voltage are set to comply with CEI 61000-4-5 class 3 voltage surge immunity tests regulation. This class applies for moderately exposed equipment, with voltages up to 2kV. Higher levels of surge energy depends on the global qualification of the whole electrical environment of the inverter, this is outside the scope of this paper.

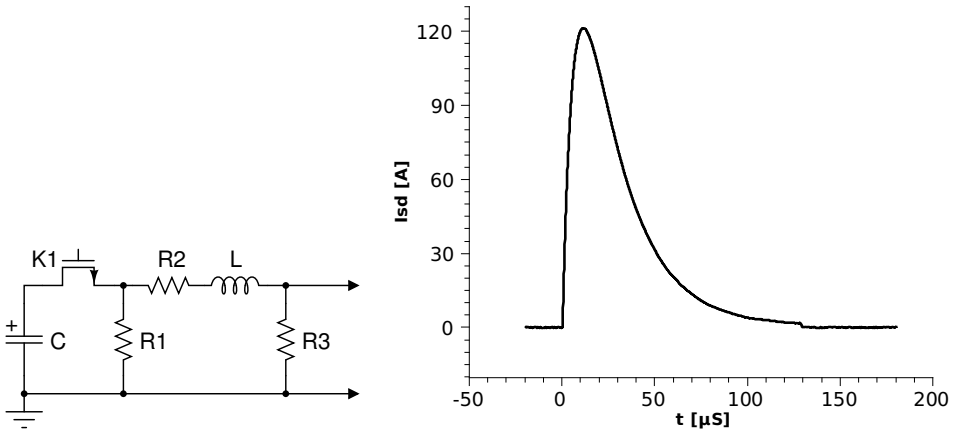


Figure 1: Normative lightning stroke generator : Generator circuit and measured short-circuit current.

Inverter, JFET and lightning surge

Assumptions

On a practical voltage fed inverter, the DC bus impedance is low because the stray inductance has been reduced to improve efficiency and bus capacitance is high to sustain the reactive power of the load. In figure 2 this translates as the following assumption : DC voltage source Zr is low enough and DC bus capacitor C is large enough to maintain a constant Ubus voltage despite the lightning stroke. In that case, the voltage source can be replaced by a short-circuit and experimental measurements can be carried out directely on a SiC JFET stuck by a lighning surge. Another consequence is that applying lightning surges on the DC bus is not relevant.

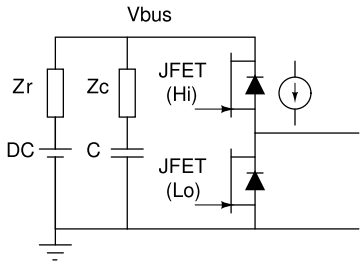


Figure 2: JFET voltage inverter stressed by lightning-induced surges on it's output terminals

Simplification

In the inverter of figure 2 each JFET, as any power switch, can be driven-On or Off by the gate driver. In the experiment described here, the simplification implies studying one JFET at a time, which is possible if one assumes that the 'other' JFET is always Off. Turning the opposite JFET On during a surge will cause the two JFET to produce a short circuit, this case is not within the scope of this paper. In ref [2], short-circuit behaviour of JFETs is studied in details. In the practical case of an inverter, the JFET gate driver will turn the opposite JFET Off –short circuit protection– so the simplification proposed is valid.

Three cases

The lightning surge may have a positive or negative polarity when applied to the inverter's terminal. Inside, two JFETs forms a leg, each JFET can be controlled On or Off at the obvious exeption of both JFETs On. Table I summarises the 6 possible cases induced by the preceeding statements. But one more information must be included here : a JFET is able to conduct current despite an 'Off' control applied by the Gate driver. A reverse voltage will force a current through the internal diode of the JFET, an Off JFET doesn't mean there is no current. Table I is used to draw the 6 corresponding circuits of figure 3. The inverter's DC link is represented, and, as assumed earlier, the impedance of the DC-bus is low compared to the JFET's ability to conduct current. From that, three cases remain to be studied :

Table I: Possibles cases when applying a lightning surge at the output of an inverter.

Case number	1	2	3	4	5	6
Surge Polarity	+	+	+	-	-	-
High side JFET	Off	On	Off	Off	On	Off
Lowside JFET	Off	Off	On	Off	Off	On

- Conduction of the internal diode only, such as in cases 1 and 4
- Conduction in the channel only, such as in cases 3 and 5
- Conduction in both channel and diode, such as in cases 2 and 6

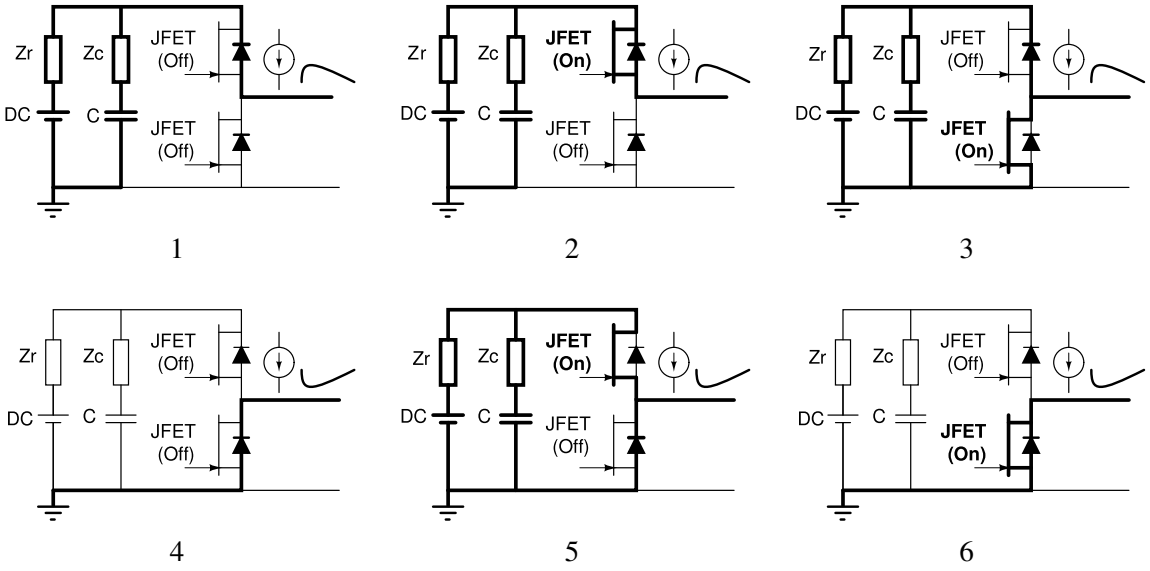


Figure 3: Possible current paths of a lighning surge applied at the output of a JFET inverter.

The experiment

The principle is to aply the voltage surge produced by the lighning stroke generator to a JFET, for various biasing conditions –the three cases– and to measure a thermo-sensitive parameter to compute the temperature response. All measurements are transients, single shot, so no averaging or synchonous detection techniques apply.

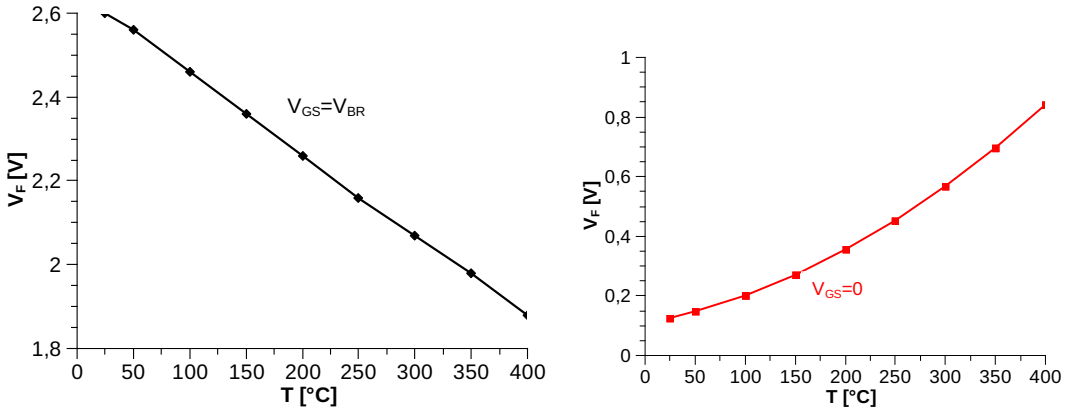
Thermal sensing

Thermo-sensitive parameters

To get the internal temperature of the device during a surge, for the three cases listed before, two separate thermo-sensitive parameter (TSP) are used.
The choice of two thermo-sensitive parameters, according to the JFET Gate biasing, is to simplify the experiment and reduce possible errors. The experiment uses the thermo-sensitive parameter that is directely available on the JFET, without modifing the Gate biasing. Using a single parameter would mean changing Gate bias during the stroke, thus creating one more source of difficult-to-control transients and adding complexity to the circuit to be taken into account for modelling.
First, when the Gate of the JFET is negative in such a way that no current flows in the channel, the device is equivalent to a diode. Hence, the choice of the forward voltage drop in a diode at fixed constant current. It is a good linear temperature indicator despite a poor gain (2mV/K).
Second, when the JFET is turned On, the Gate to Source voltage is nulled, the internal diode in shunted by the channel conduction. Here, the temperature estimator is the channel resistance at reduced voltage, to make sure no conduction occurs in the diode. Here the gain corresponds to the RDSON of the JFET, which is, again, quite low (0.3 Ohm at room temperature).

Thermal calibration

Thermo-sensitive parameters are calibrated prior to the experiment by applying a fixed temperature for a long enough time on the JFET and measuring the electrical response. A fixed current source is used for both parameters: diode voltage drop and On-resistance. To avoid self heating during the experiment and possible interaction between the stroke and the sensing circuit, the measuring current is applied during a short period through a controlled switch. The full experiment circuit diagram is described in the next paragraph, in figure 5.



V_F= Diode forward voltage drop @ 200mA.

V_F= On-voltage across channel @ 300mA

Figure 4: Calibration curves of thermosensitive parameters.

During calibration a constant current pulse is applied on the device under test. The electrical circuit is not altered between calibration and measurement. The same control unit is used for sequencing the switches (see figure 5), the difference during calibration is that the stroke carries no power (Vc=0) and the temperature is set externally by a thermo-regulated heated slab. The TSP is an image of temperature, fitting the data sets permits to write the equations of temperature as a function of V_F for each TSP, see table II.

Table II: Equations used to sense the temperature with thermo-sensitive parameters.

Diode @ 200mA	$T_{diode} = -5,17.10^2 V_F + 1,37.10^3$
Channel @ 300mA	$T_{On-resistance} = -1,17.10^2 + 1,31.10^3 V_F - 1,42.10^3 V_F^2 + 6,99.10^2 V_F^3$

Thermal sensing during a stroke

Thermal sensing through electrical measurements during a stroke is performed by interrupting the stroke at increasing time steps, isolating the device under test, and then, applying a fixed current to get a voltage response. Each step (during each stroke) produces one temperature value associated with a time delay. The set of values can then be supperimposed on a single plot to form a 'real time' thermal response.
Four switches are used and are controlled by a common programable logic unit, triggered by the push of a button. Now lets give a look at figure 5. K1 is the main switch of the stroke generator, it connects the precharged capacitor C to the passive network that produces the normalized stroke waveform. K2 permits to interrupt the stroke by diverting the current to ground, K2 is operated after a variable duration Δt1 and remains closed until the total energy of capacitor C is dissipated in the network. K3 isolates the stroke generator from the JFET under test to allow the voltage measurement of Vf, after a deadtime Δt3 of 1μs. A second deadtime of 1μs is placed before the application of the measuring current Im by K4. This switch is turned On for a fixed duration, Δt4 of 10μs. This is when the TSP voltage Vf is acquired. It reflects the temperature response of either the diode or the channel. t1 is increased gradually to the entire stroke's duration (up to 200μs) to measure the temperature step by step.

Experimental results

Due to severe Electro-Magnetic-Interference (EMI) it is not possible to get the measured TSP voltage during a period of several μs after the interruption of the stroke. For that reason, linear extrapolation is used to 'go back in time' from acquired data. The acquisitions are visible on the picture of figure 6,

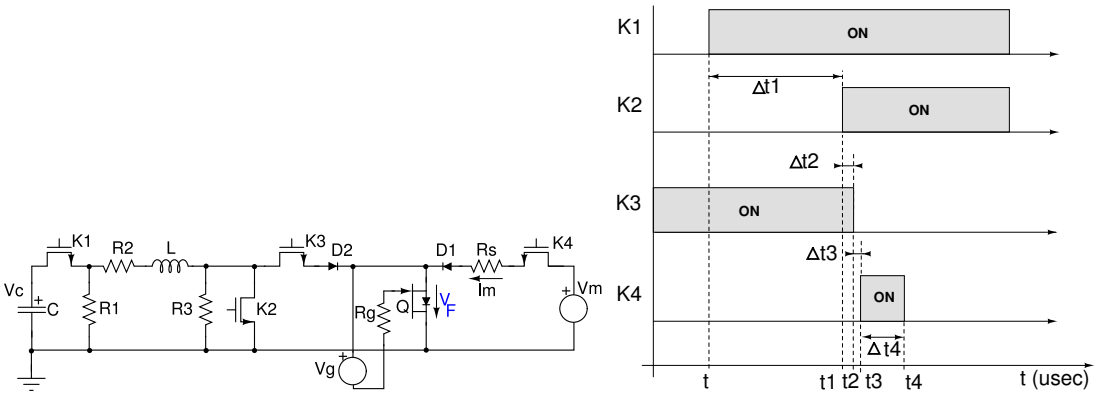
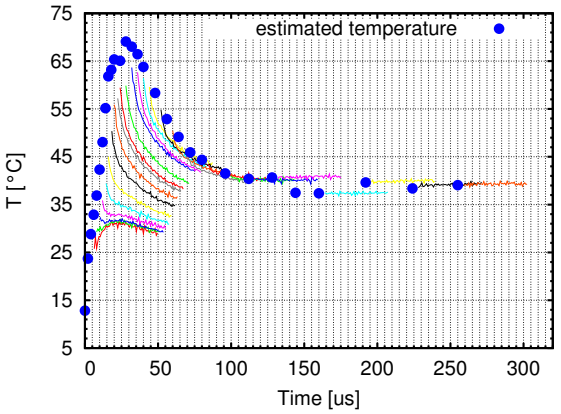


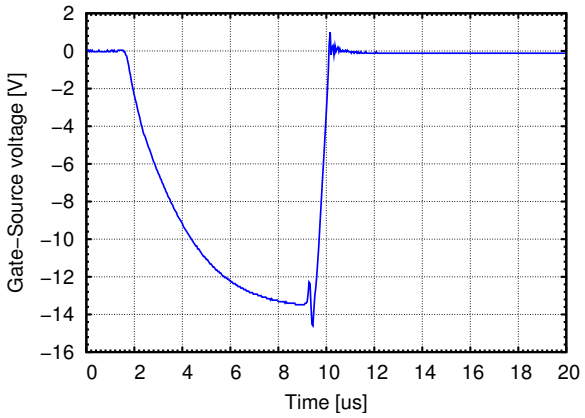
Figure 5: Experimental setup circuit and switching sequence.

blue dots are calculated from each separate acquisition. The error due to the electrical measurement is estimated to 10°C. The error due to extrapolation is more complex to estimate and a filtering effect can be observed.
A first section describes the experiment for cases 3 and 5, as in Table I, a stroke is applied to provoque a direct conduction from Drain to Source, in the channel only. A second section treats both cases 1 and 4 and cases 2 and 6, as the JFET is stressed in reverse conduction.
For all experiments, a specific Gate biasing circuit is used. This circuit is described at the end of this section.

Direct conduction



Estimated temperature, conduction of channel only



Gate-Source voltage during a stroke (interrupted at t=10us)

Figure 6: Experimentally estimated thermal response and Gate voltage.

To get a conduction in the direct conduction mode, one has to bias the Gate-Source voltage to zero volt. A short circuit is an obvious answer. Nevertheless, care must be taken to control the Gate current in order to prevent destruction. We have set a biasing circuit (see figure 8) that permits a high common mode impedance for EMI reduction.
More, the stroke generator produces a strong EMI across the whole circuit. Carefull decoupling of common mode and single ground connexion is compulsory. One more difficulty is the dynamics of the signals: within 1us, measured current and voltages change by a ratio of 1000.
The estimated temperature is plotted in figure 6. The temperature rise is not important, this is due to the limitation we have put on the input voltage : 1kV instead of 2kV as stated in the CEI 61000-4-5 class 3 standard. This limit is directed by several facts : increasing the energy on the circuit increases EMI, thus degrading the precision of the measurements. More, we have observed an unexpected voltage variation between Gate and Source as shown on figure 6. The voltage is supposed to be set at zero by the Gate biasing circuit. During the stroke, there is a voltage appearing between Gate and Source, reaching -15V. The breakdown voltage of the Gate is -19V for the device we have used. For safety reasons, we have not increased the energy for this experiment.

Inverse conduction

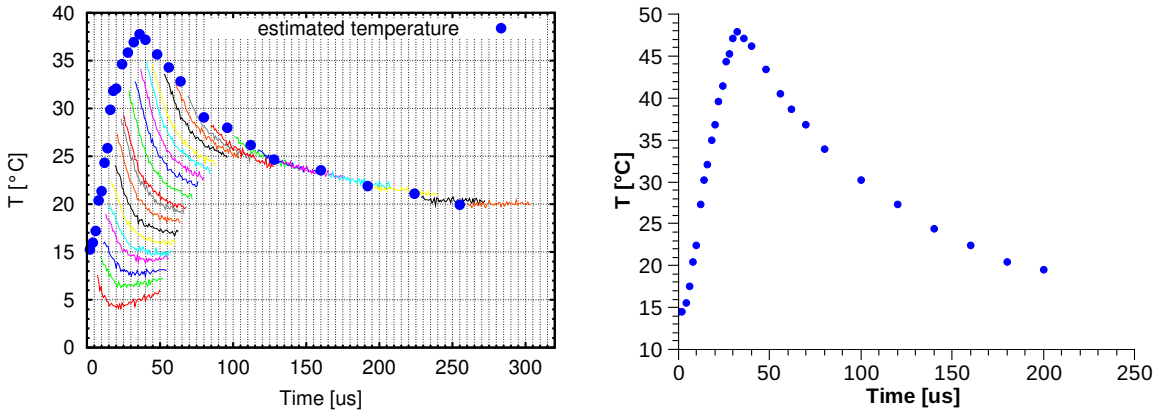


Figure 7: Experimentally estimated thermal response

For the sake of comparison, the energy level, although low, was kept identical for all tests. The difference between the plots of figure 7 is the Gate bias value. To get the internal diode of the JFET to conduct on its own, a negative Gate bias is applied. Both channel and diode may conduct if the Gate is zero biased (in reference to the Source).

Gate biasing circuit

A specific circuit, (see figure 8) is designed to obtain safe Gate biasing and a good control of the channel conduction. A high common mode impedance is obtained by using high values for Ra and Rb (typically 68 kΩ). Cg is a high value film capacitor for get a low differential impedance in order to maintain a constant voltage, 10 μF. Rg emulates the output impedance of a Gate driver, here a 33 Ω resistor. The key role of Ra-Rb and Cg is to drive safely the JFET Gate-Source into punch-trough in order to be sure that no current flows through the channel. Ra-Rb limit the static Gate current to acceptable values, while Cg maintains the voltage during transients. The dynamic Gate current is limited by Rg.

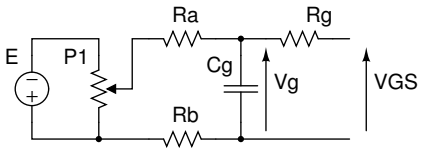


Figure 8: Gate biasing circuit.

Verification of thermal sensing by simulation

To verify the consistency of the estimated temperature we have developped a thermal model in witch the experimentally measured power is used as an input. The simulation is purely thermal as the building of an electro-thermal model of the JFET under over load is very complex. For simplicity, the thermal model is a classical R-C equivalent thermal circuit as shown on figure 9. The SiC chip is 'cut' into 30 regions getting wider as the distance from the active area increases. We also made simplifications due to the fact that only short durations are observed : a single thermal path from the top of the JFET to the backside. The backside is kept at room temperature. It is not important to increase the precision of the thermal model knowing that the temperature estimation has an error in the order of 10°C. By using experimental measurements of current and voltage accross the JFET, instantaneous power is computed and used as a power source in the thermal model. This technique permits to separate the thermo-electrical behaviour of the JFET from the purely thermal cooling phenomenom in order to verify the temperature estimation.

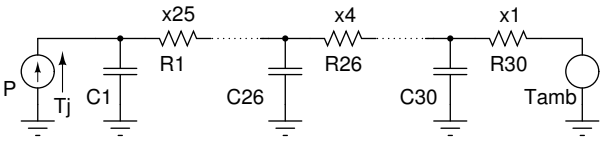


Figure 9: Equivalent electrical circuit for the thermal behaviour of the JFET chip at very short time durations

In the next sections, the simulated temperature is plotted on the same graphs as the experimentally estimated temperature for each of the three experiments (the three cases). In all cases, the matching is not close but the curves shows the same behaviour.

Direct and inverse conduction

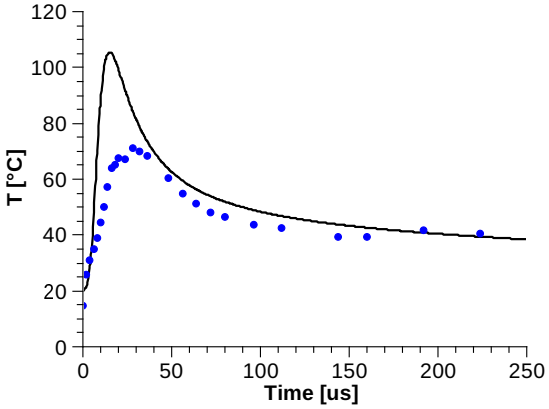


Figure 10: Comparison of simulation versus experimental thermal response.

It is in direct conduction that the maximum temperature is reached. This observation can be linked to the observation of the Gate-Spource voltage. For direct conduction, the Gate is biased at zero volt by the circuit of figure 8, thus letting the channel to be normally-On. During the stroke, the overload current produces a Drain-Source voltage that can be as high as 20V, as a consequence, the Gate potential is moved, and an external Gate-Source voltage of -15 can be observed. We suppose that in such conditions the channel is no more fully On, further investigation is needed at this point.

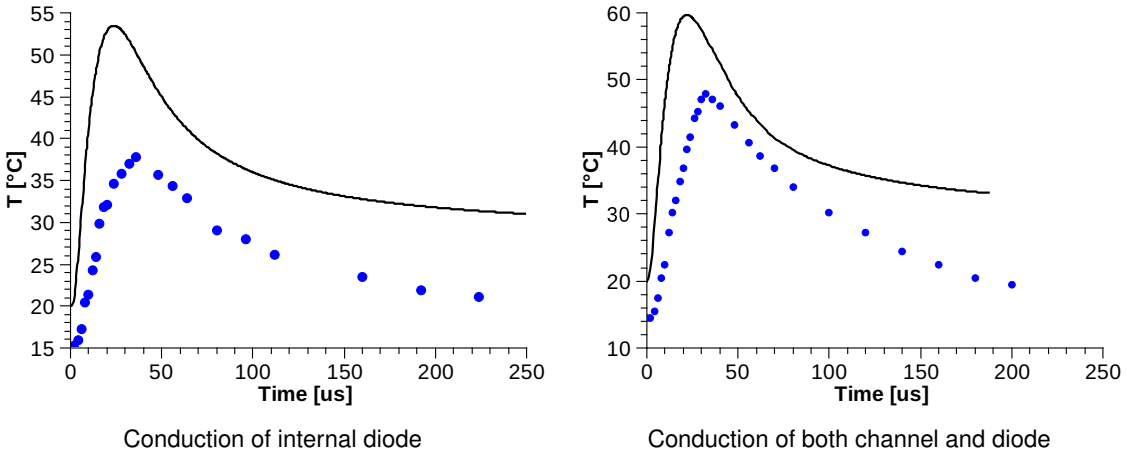


Figure 11: Comparison of simulation versus experimental thermal response.

Discussion

On the plot in figure 11, as in the one in direct conduction, the simulated response (solid line) shows a peak that is delayed from the measured temperature using TSPs. As the same triggering signal is used in all experiments and as the reference signal for the thermal simulation is the current and voltage acquired with that trigger, trivial error is not possible. Another information from the plots is that the estimated temperature (measured) response looks like a low-pass filtering has occured. This can be a thermal phenomenom inside the JFET as power dissipation is not located exactely where the TSP region is situated. More, the TSP voltage is extrapolated over a segment of 10μs. For each of the three cases the current path differs hence different regions of the device are stressed differently. In this paper, we do not pretend to address the physical aspect of the problem, nevertheless, important variations on experimental thermal responses asks for an attempt of explanation. As expressed in the previous section, errors on the use of TSP take part in the difference observed between experiment and simulation. Another source of incertainty is the thermal model that as probably too simple for very short periods of time. And more generally, the difference of geographic situation of the heated region versus the TSP region inside the JFET. In figure 12, for example, the Drain-Source diode is situated at the top of the chip while power dissipation occurs in both the channel and the diode in reverse conduction with zero volt Gate bias. In that case the TSP used is the Diode forward voltage.
Further study of the Gate behaviour and its hability to withstand current surges will enable high power strokes to be tested and perhaps the thermal limits of SiC clearly showed?

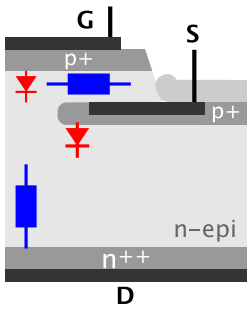


Figure 12: Simplified cross section of JFET

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