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Local ESD protection structure based on Silicon Controlled Rectifier achieving very low overshoot voltage

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Abstract - This paper presents a new local ESD protection structure. This structure is based on static triggered SCR and realized in a 45nm CMOS technology node. This protection achieves very low static triggering voltage, low on-resistance, low DC leakage current for off configurations. This new structure is latch-up free and fail safe.

I. Introduction

The purpose of this work is the development of local ESD protection structures in the same way as the authors in [1]. Local protections can be used at the signal pads to provide a direct ESD current path from the pad to the ground. Furthermore, classical dynamic triggered ESD clamps cannot be used on signal I/O local protection. To cope with this problem, the triggering of the proposed ESD protection is achieved through static triggering. A silicon controlled rectifier (SCR) component is preferred to a MOSFET because of its good ESD performance [2]-[5] in terms of low on-resistance, small footprint area, high second breakdown current and low intrinsic leakage. As proposed in previous work, an efficient static triggering can be implemented using a diode stack as shown in figure 1 [1-3]. In the present work, we analyze the benefits of an amplifier on the ESD performance

This work is realized to solve the latch-up problems due to a classical RC-trigger. While an RC-trigger detects the rise time (dV/dt) of the ESD event, the static trigger turns the SCR on when the voltage drop reaches a defined voltage level. The protection structure becomes independent of the rise time and depends only of the voltage drop of the event. One of the advantages is that for an SCR with a static trigger, the protection structure protects the integrated circuit against an ESD event even if there are pre-discharge spikes [6] or if the event is not in the classical RC filter window.

The proposed structure also has the advantage of not using a capacitive component, that results in silicon area saving. Diodes used in this protection are small

and the saved area is 60% for the ESD protection in the 1.2V power domain, and 20% for the ESD protection in the 1.8V power domain. The paper is organized in six sections, the first one being the introduction. In section II, a new structure based on the SCR device is presented. Characterization and measurement results are presented in section III. Section IV, compares electrical simulation of the new structure with a previous structure, the DTSCR. Section V describes the implementation of the structure in the ESD network. Section VI presents the conclusions this paper.

[Keywords: static triggering, ESD, SCR].

II. New SCR structure

The turn-on time of the SCR generates a voltage overshoot which can lead to load damage. Two elements can explain this overvoltage. The first is intrinsic to the SCR structure and is due to the diode overshoot as seen in [7], [8]. The second element is the trigger circuit and its capability to turn-on the SCR faster to limit the voltage overshoot.

To trigger a P+/NW/PW/N classical SCR with a low overshoot voltage, one efficient solution consists in connecting a string of diodes between the Nwell (PNP base) and the ground. This structure, called diode-triggered SCR or DTSCR, was presented by [9]-[11] and is reported in figure 1.

When an ESD event occurs, the conduction of the diode string results in the injection of current into the base of the PNP (Nwell) which in turn will trigger on the SCR. The triggering voltage of the protection can be adjusted by changing the number of diodes in the string. This enables to adapt the ESD protection to the

technology (to guarantee that the breakdown voltage is not reached) and the supply voltage.

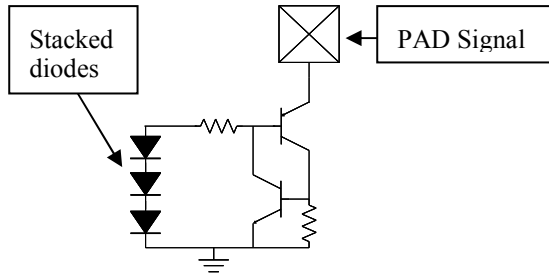


Figure 1 : Circuit schematic of the DTSCR

In this structure, diodes are expected to drive several milliamperes to trigger the SCR, which should lead to large area of diodes if a minimum overvoltage is required. A trade off has to be made between efficient triggering capabilities and a low leakage current as explained in [10]-[11].

The proposed structure aims at achieving the following characteristics: low static triggering, reduced triggering and overshoot voltages, low leakage current, and minimized area.

The protection is illustrated by the Fig.2 for two power domains:

- GO1: 1.2V power domain, thin oxide thickness.
- GO2: 1.8V power domain, thick oxide thickness.

For a positive ESD stress, this protection consists of a static detector, composed by three diodes and a resistor which generates the reference voltage, an amplifier, composed by a first stage with one PMOS and one resistor and a second stage with one PMOS and one NMOS. Finally, the Nwell through N+ of the SCR is connected to the output of the second stage of the amplifier. This driver is properly designed to provide the SCR triggering current by electrical simulation using STMicroelectronics developed fast transient SCR model realized in 45nm node technology from previous work [12]. One diode is added to drive the current due to a negative stress. The signal I/O is composed by 20% of triggering circuit and 80% of the power device. The SCR width is 10 times less than the width of a big MOSFET in classical MOSSWI clamp.

The aim of this new protection is to realize a static protection with a small area footprint and a leakage current smaller than the DTSCR (fig. 1). The triggering current (flowing through the Nwell) is provided by the amplifier; the diode string is only

supposed to drive the small capacitance amplifier input which leads to smaller diode area. As a result the leakage current which is proportional to the diode area can be reduced.

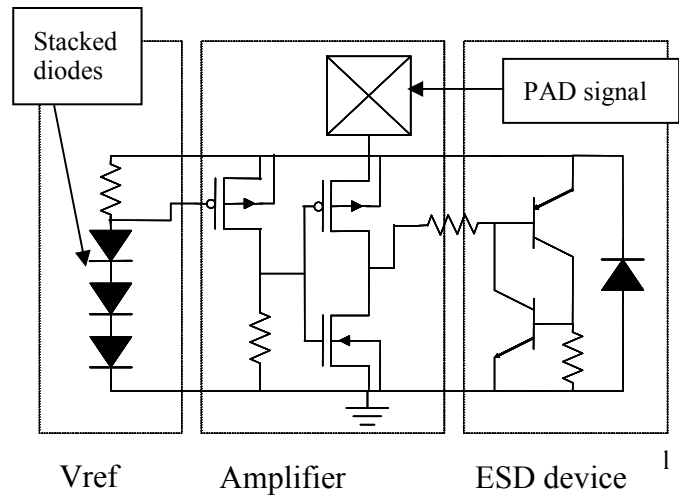


Figure 2 : Circuit schematic of the SCR protection using a new static triggering circuit

III. Experimental Results

A. TLP Device Characterization

The protection structure shown in figure 2 has been realized in a 45nm CMOS technology. Figure 3a) shows the TLP curve for the 1.2V structure achieved with a GO1 triggering circuit. The TLP pulse-width is 100ns with a rise time of 10ns. This curve shows a maximum quasistatic TLP triggering voltage $V_{t1stat}=3.5V$. The holding voltage is $V_h=1.25V$ and the on-resistance is equal to $R_{on}=0.18\Omega$. The device can handle 3A without failure, which corresponds to 4kV HBM stress.

Figure 3b) shows the vTLP I-V characteristics for a pulse width of 9ns and a rise time of 250ps. Similar characteristics are observed with a $V_{t1}=3.4V$, $R_{on}=0.14\Omega$ and $V_h=1.22V$.

Figure 4 compares the quasistatic TLP I-V characteristics of two structures, 1.2V protection made of GO1 amplifier of the triggering circuit and 1.8V protection made of GO2 amplifier of the triggering circuit. The only difference between the both structures is the amplifier which is realized by GO1 MOS (thin oxide thickness) for the GO1

structure whereas the amplifier of the GO2 structure is realized by GO2 MOS (thick oxide thickness).

The triggering circuits of the two structures were optimized to achieve the same $V_{ti}=3.5V$. Figure 4 shows that similar quasistatic characteristics for the GO1 and the GO2 structures are achieved. The triggering voltage is shifted from 3.5V for GO1 to 3.7V for GO2 and the holding voltage is the same. To achieve the same performance than the GO1 protection, the GO2 triggering circuit area has been increased of 250%.

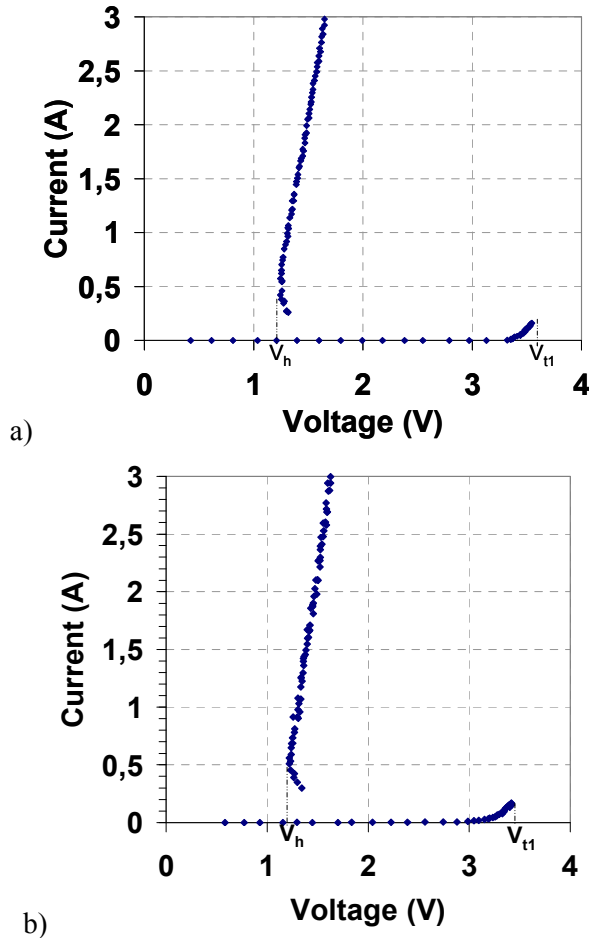


Figure 3: curve a) is a 100ns TLP I-V curve and curve b) is 9ns TLP I-V curve of the proposed SCR for 1.2V power domain.

The measurement proves that a single ESD protection (GO2 triggering) can be used for both 1.8V and 1.2V supply voltages.

B. Transient overshoot voltage

For a good protection, the SCR must turn on rapidly with a minimal overshoot to avoid oxide damages. To

evaluate the impact of the triggering strategy, we compared the switching characteristics of three different designs. The first structure is the SCR without any triggering circuit, the second one is the structure presented in Fig.2 and the third one is a GO1 triggered SCR with a ggNMOS added in parallel as proposed in figure 5. The ggNMOS width is of 25% of the SCR width. The purpose of this ggNMOS is to clamp the overshoot.

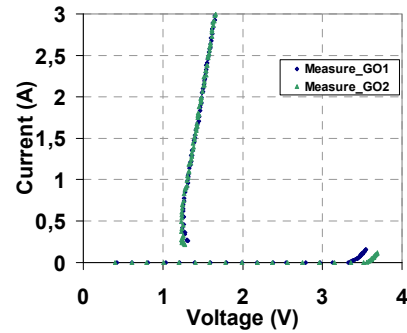


Figure 4 : 100ns TLP I-V curves for two static structures in two power domains GO1=1.2V and GO2=1.8V

The transient turn-on characteristics of these three structures were measured using a CDM-like pulse (Fig. 6, 7). The measurements were realized by Time Domain Transmission (TDT) measurements with repetitive pulses for very fast transient characterization system (vfTCS) [13]. The vfTCS system has been used to characterize the SCR triggering in dipole to capture its transient behavior with a great accuracy.

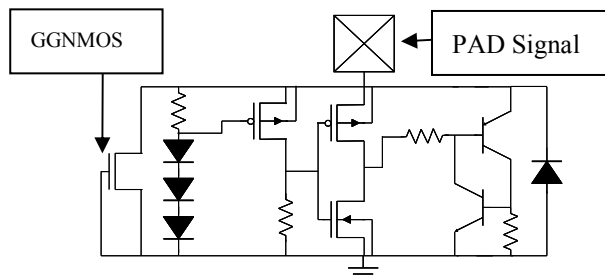


Figure 5 : Complete protection

The figure 6 shows the transient voltage for 1.7A quasistatic current. The maximum overshoot voltage is obtained for the SCR without triggering circuit (12V). The structure presented previously reduces the overshoot down to 7V and for the structure with the added ggNMOS, the overshoot is decreased down to less than 4V [14] [15]. The turn-on time is similar and equal to 0.7ns for the standalone SCR and the

structure without the ggNMOS, whereas it is increased up to 1ns for the last structure.

This result shows that if the overvoltage is high enough (4V), the ggNMOS triggers on and clamps the transient overshoot so that the overvoltage is limited. This second stage of protection is very efficient in CDM time domain and can be optimized depending on load. For the rest of the stress (from 3ns to 10ns), the SCR protection structure is capable to turn on and sustain the quasistatic part of the stress. This assumption is confirmed by the results reported in

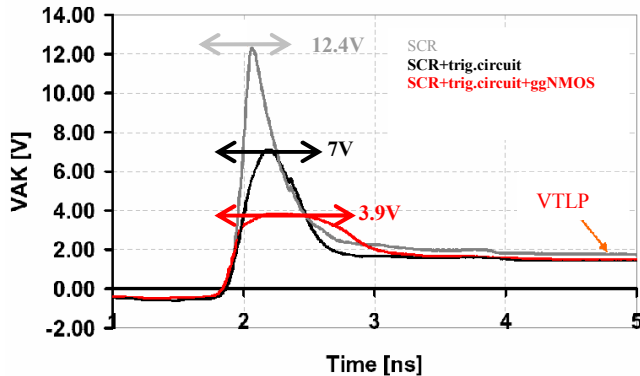


Figure 6 : Transient Voltage for 250ps rise time and 9ns pulse width for the three SCR structures: standalone, with triggering circuit of Fig2 and triggering circuit of Fig.5

figure 7. Indeed, in this figure we can verify that the overshoot voltage is clamped by the ggNMOS around 4V and in the same time the quasistatic curve remains the same whatever the ggNMOS is present or not.

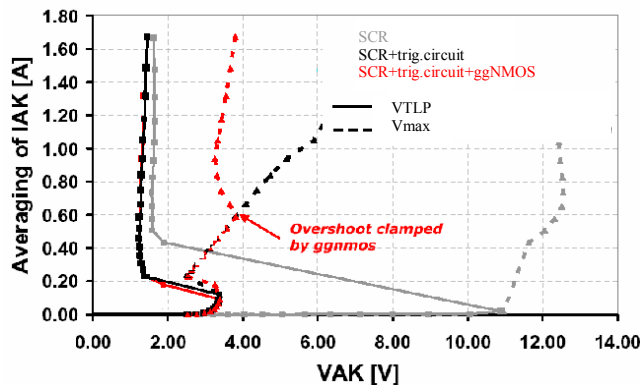


Figure7 : GO1 triggering Quasi-static current vs. TLP quasi-static (plain line) Max overshoot (dotted) voltage in three configurations

C. DC Leakage Characteristics

Figures 8 and 9 show the DC leakage characteristics of the three structures at 25°C and at 125°C

temperatures, respectively. Firstly, without the ggNMOS, the GO1 triggered structure has a higher leakage current than the GO2 structure at 25°C and at 125°C. The leakage current of the proposed SCR is 0.054nA/um for a GO1 triggering and only 0.037nA/um for a GO2 structure at VDD=1.2V±10%. But for GO2 power domain (VDD=1.8V), the leakage current is increased up to 0.081nA/um at VDD±10%.

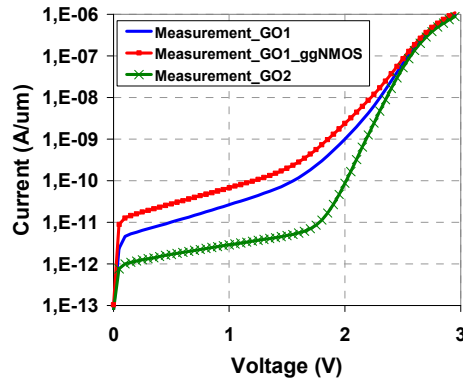


Figure 8 : DC leakage current measurement for two static structures in two power domains GO1=1.2V and GO2=1.8V at 25°C

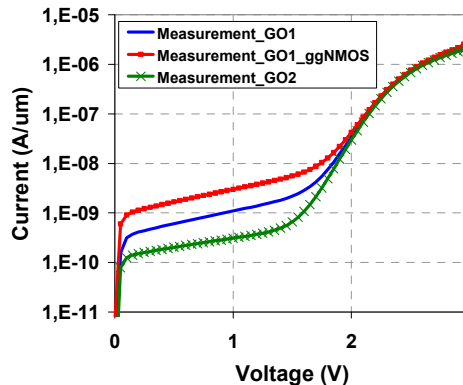


Figure 9 : DC leakage current measurement for two static structures in two power domains GO1=1.2V and GO2=1.8V at 125°C

At 125°C, the leakage current is degraded: for the GO1 structure, the current reaches almost 1.57nA/um at the same voltage, whereas for the GO2 structure it is 0.43nA/um. But for VDD=1.8V the current reaches 32.4nA/um. The main leakage current is due to the MOS of the amplifier of the structure. That's why the GO2 structure with thicker oxide keeps the leakage current lower.

Thus without the ggNMOS, the achieved leakage currents are reasonably low.

Then, at both temperatures, it can be seen that when the ggNMOS is added, the leakage current is

increased due to the ggNMOS leakage current contribution but the total leakage current remains low.

Finally, the latch-up immunity is achieved by a triggering current of the structure higher than 100mA at 125°C JEDEC standard.

IV. Comparison with the DTSCR

This part of the paper compares the new ESD protection structure with diodes trigger SCR (DTSCR). This study is only based only on spice electrical simulation using an SCR model and compares the triggering voltage, turn-on time and leakage at 25C and 125C for the SCR with diodes string and an amplifier (figure 1) and the DTSCR, SCR and diodes string only (figure 2) .

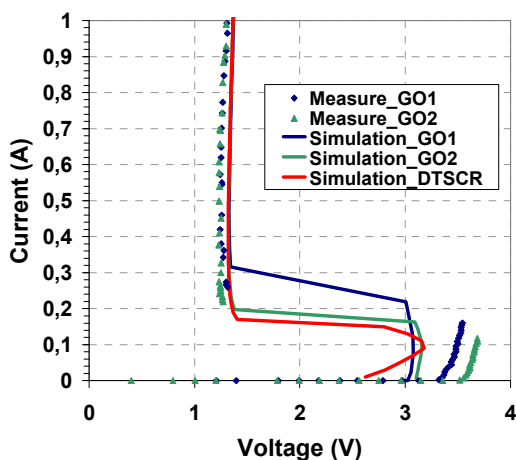


Figure 10: 100ns TLP I-V curves for three static structures in two power domains GO1=1.2V (blue), GO2=1.8V (green) and DTSCR (red). Dots curves are the electrical measures whereas the plain lines are electrical simulations.

A. Triggering Voltage

The figure 10 shows the correlation between real measurements and simulation results of the SCR with the static voltage trigger not including the ggNMOS.

The I-V 100ns TLP curves show a good matching between modeling results and experimental data, with same on-resistance, same holding voltage and a reasonably well predicted triggering voltage.

The DTSCR was designed to reach the same performance as the SCR with static triggering for GO2 power domains. That is why the triggering voltages of these two structures are similar.

B. Transient overshoot voltage

To observe the turn-on time of the different ESD protection structures, the three ESD structures are simulated during a 3A current pulse with a rise time of 10ns. Figure 11 provides a comparison of the overshoot voltages of the presented structures for GO2 power domain, 3 diodes string DTSCR (DTSCR3) and 2 diodes string DTSCR (DTSCR2).

To decrease the overvoltage of the DTSCR, two ways are investigated. The first one is to remove one diode in the three diodes string, so that the trigger current can flow earlier through the 2-diodes string and enable a faster turn-on. The second way is to increase the size of the three diodes, but even using larger diodes does not allow reaching the low overvoltage level of the proposed SCR static triggering. Thus the overshoot reaches 5V.

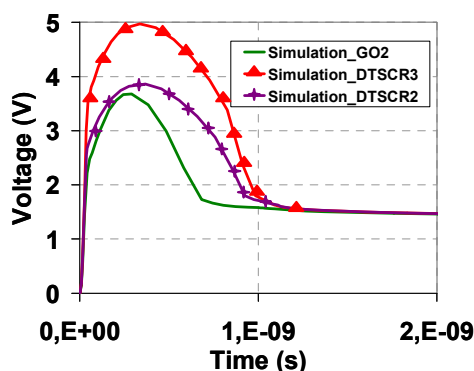


Figure 11 : Voltage waveform at current level of 3A for 10ns rise time

This simulation shows that the magnitude of the voltage overshoot is higher for the three diodes string DTSCR. The only way to improve the turn-on time of the DTSCR is to reduce the number of diodes. The 2-diodes string DTSCR achieves similar performance (3.86V) to the SCR with the proposed trigger (3.68V) in terms of turn-on speed.

Furthermore the duration of the overvoltage increases from 0.7ns for the proposed structure up to 1ns for the DTSCR whatever the number of diodes in the string.

C. DC Leakage Characteristics

Figures 12 and 13 show the DC leakage characteristics of the two DTSCR structures with two or three diodes string normalized by the leakage current of the presented structure for GO2 (I0) at 25°C and at 125°C temperatures, respectively.

At 25°C, the level of the leakage current of both simulated DTSCRs is lower for the structure made in

GO2 for the 1.2V power domain. But for 1.8V power domain, DTSCR with the two diodes string has its leakage current level (I_0) reaching ten times more than that of the proposed GO2 structure (almost 0.8nA/um), whereas the leakage of the 3 diodes string DTSCR remains very low (ten times less, near 0.008nA/um).

At 125°C, as expected, the leakage current is degraded. However for 1.8V, the trends are more favorable for the proposed structure. Indeed, the leakage current increased but not at the same rate: 30uA/um for the two diodes string DTSCR, around 300nA/um for the three diodes string DTSCR, and in the range of 30nA/um for the GO2 presented protection.

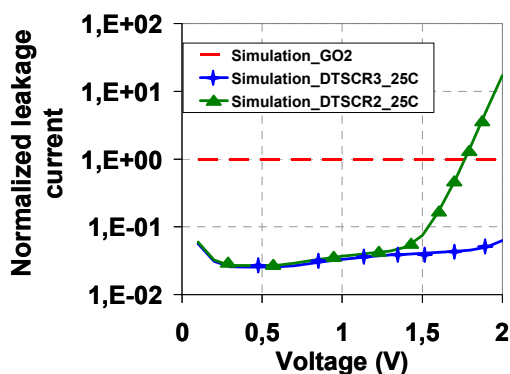


Figure 12 : DC leakage current for DTSCR with two or three diodes normalized by the leakage current of the presented structure for GO2 power domain (I_0) at 25°C

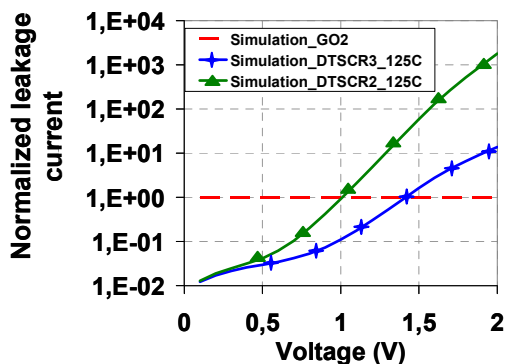


Figure 13 : DC leakage current for DTSCR with two or three diodes normalized on the leakage current of the presented structure for GO2 power domain (I_0) at 125°C

The main difference between the DTSCR and the presented structure in term of DC current is that in the first case the leakage current is determined by the size of the diodes, whereas in the second case the leakage current is mainly due to the MOS amplifier and not due to the diodes string.

D. Triggering circuit Area

The triggering circuit area footprint must be as small as possible and in the same time keeping a good performance to turn the SCR on. So the comparison of the size of the DTSCR and the new structure shows that the new triggering circuit reduces the footprint area by a factor of 37% compared with the three diodes string and 16% compared with the two diodes string.

E. Summary

Table 1 summarizes of the simulation comparison made previously, between the GO2 structure presented in this paper and the two or three diodes string DTSCR.

Device	GO1_ structure	GO2_ structure	DTSCR3	DTSCR2
Vt1	3.07V	3.14V	3.18V	3.19V
Overvol- -tage for 3A	2.46V	3.68V	5V	3.86V
Turn-on time	0.7ns	0.7ns	1ns	1ns
Ileak 25C (1.8V)	0.3 nA/um	0.01 nA/um	0.001 nA/um	0.1 nA/um
Ileak 125C (1.8V)	8nA/um	5 nA/um	50 nA/um	5 uA/um
Normal- -ized Trigger area	0.4	1	1.3	1.16

Table 1: Summary of the comparison between GO2_structure and DTSCR with two or three diodes string

V. Implementation

This proposed protection structure is designed to be used as a local clamp for I/O pins as shown in Fig. 14. It is capable of clamping positive ESD events on the input pad thanks to the static triggered SCR and negative events thanks to the forward diode. As the triggering is caused by the clamped overvoltage (>3.4V), the structure is immune to high speed transient signals. Its high external latch-up triggering current (>100mA) makes it latch-up free.

The excellent latch-up performance allows contemplating using it as a power clamp protection in IO ESD protection strategy.

In summary, both the robustness and the leakage current are better when the gate oxide thickness is higher, but in the same time, silicon area, turn-on time and overvoltage are increased. GO2 triggering structure is preferred if the leakage current must be minimized. GO1 structure is preferred if overshoot voltage and area must be minimized.

The final optimized structure will be a trade-off between a good turn-on time, a low overvoltage, a high robustness, a minimum area and a low leakage current.

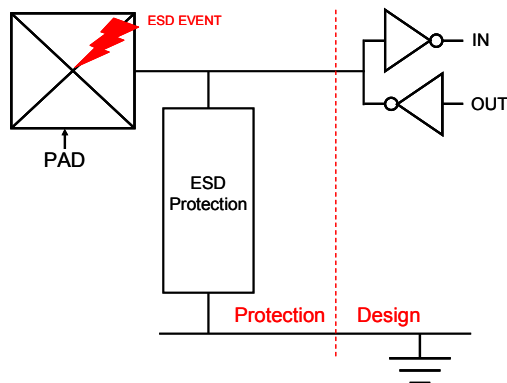


Figure 14 : Implementation of the proposed structure

VI. Conclusions

A new SCR with a static voltage triggering methodology is introduced in this paper. This structure solves several issues associated to SCR-based protection structures. The static triggering allows getting rid of the unexpected triggering of the SCR due to a high frequency electrical signal and thus can be used as a local protection for signal pads. The second interesting characteristic is a low triggering voltage compatible with advanced technology nodes, while keeping a low overshoot voltage with a smaller footprint area than the dynamic triggered SCR. Then we have shown that for different signal voltages, a single protection can be used. Furthermore, adding a ggNMOS clamping device allows drastically reducing the transient overvoltage under very fast stresses which can be limited to very low values (4V) with a small increase of the total leakage current. Finally, simulation comparisons with the DTSCR give the advantage in term of transient overshoot, turn-on time, trigger area and leakage at high temperature.

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