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# Complementary MOS structures for common mode EMI reduction

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## Keywords

EMC/EMI, efficiency, MOSFET

## Abstract

The paper deals with the management and the reduction of conducted common mode EMI noise in power converters. Especially, it is presented how complementary P-N MOSFET structures, used in a specific manner, are able of great and natural common mode current reductions. The advantages obtained by the use of complementary MOSFET topologies are balanced with the additional conduction losses that P MOSFETs are responsible of. The paper presents these issues based on simulation and practical results.

## I. Introduction

In power electronic, the common mode conducted noise in switched mode power supplies may cause radiated noise emissions and unexpected disturbances to the other equipments [1][2][3]. Therefore, it is important to reduce this noise and standard have been established to limit radiated and conducted EMI [4]. For that purpose, many works have been carried out to develop power converters that meet standard regulation limits. Indeed, the passive filters [5][6], active filtering [7][8], dynamic reduction of noise sources and symetrization of conducted current's propagation paths [9][10] have been studied. The common feature of these works is to add active or passive components in the conventional structure in order to block or to recycle the propagation of conducted EMI. This is usually done by increasing the amount of components and the global cost of the converter.

This paper proposes to investigate the EMI signature of complementary topologies based on the utilization of N and P types MOSFETs. In some cases, it will be shown that complementary structures, by a full symetrization of the topology, are able of great and natural reductions of the conducted common mode disturbances. As an example, a half-bridge complementary inverter is implemented in this paper and its EMI operation is compared with the one produced by a comparable converter based on N type transistors. The mechanism of common mode noise reduction is explained. Since the introduction of the P type MOSFET in the converter will introduce additional ON state losses, the performances of the conventional and complementary half bridge topologies are also studied and compared thanks to simulation and experimental results.

## II. Introduction to the concept of complementary inverter circuits

In power electronics inverter topologies, the main propagation paths of common mode current harmonics are through the parasitic capacitor connected between the middle point of each inverter leg and the frame ground. This parasitic capacitor is usually formed by the copper plate on which is soldered the backside of the power dies in isolated module or even the case of the chip (connected to the backside electrode of the power die) in the non isolated packages (ex. TO220 or TO247). In most cases, the heat sink being connected to ground, a large parasitic capacitor is created between each power die backside and the ground, offering a common mode current propagation path. Then, as a function of the voltage variations appearing on these parasitic capacitors, large common mode

disturbances may be generated. Fig. 1 gives an illustration of the parasitic capacitors' physical locations whereas these capacitors are added to the schematic on Fig. 2.

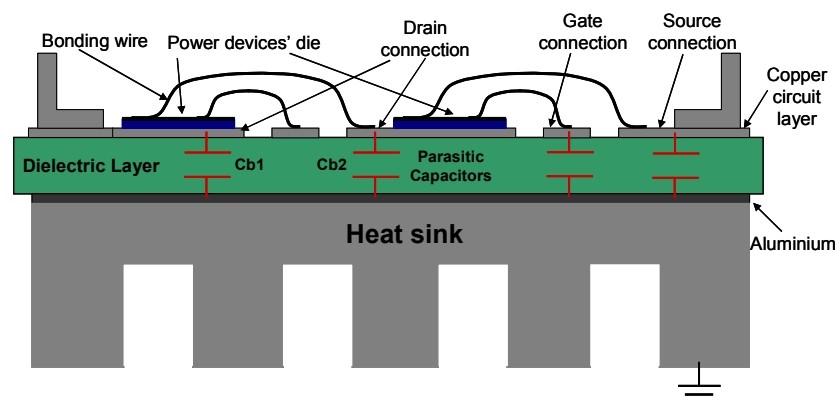


Fig. 1: Main common mode parasitic capacitors in a conventional power electronic structure

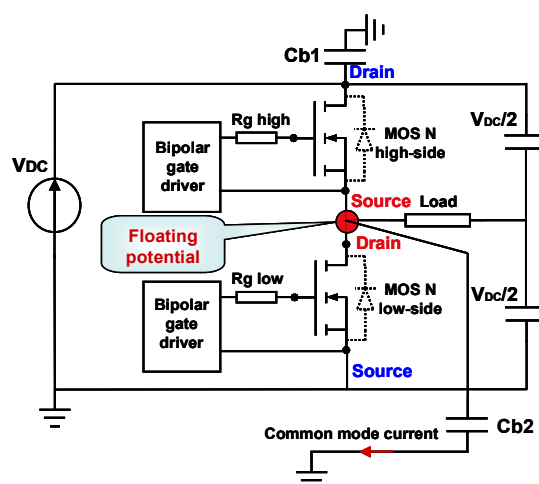


Fig. 2: Conventional half-bridge inverter - schematic and electrical location of common mode parasitic capacitors.

The conventional inverter structure is depicted on Fig. 2. It is a half-bridge topology where the main parasitic capacitors relating to the drain of the two MOSFET transistors are Cb1 and Cb2, of which the Cb2 capacitor is connected to middle point to the inverter leg. In switched mode power supplies, the middle point whose potential is floating exhibits large voltage variations with respect to time ( $dv/dt$ ) each switching transition. Therefore, a large current pulse flows through the parasitic capacitance Cb2. Consequently, this leads the large common mode conducted noise current. On the other hand, the parasitic capacitors connected to the DC bus of the converter are a lot less excited by large  $dv/dt$ .

In this context, we propose to investigate how a complementary half-bridge inverter topology, as shown in Fig. 3, could be able to reduce conducted common mode disturbances. In complementary topologies, each leg is made with a series association of a N type and a P type MOSFET transistors. This topology which is interesting for EMI reduction is not the classical inverting CMOS structure with the P type transistor as the "high side" transistor and the N type transistor as the "low side" transistor. It is the topology with the complementary transistors associated in series but having their sources connected at the same potential as it is presented in Fig. 3. This structure is fully symmetrical and presents the main parasitic capacitors (Cb1 & Cb2 located at the back side of the power dies) located mainly on the DC bus whose potentials are more stable. Therefore, in this configuration, the common mode conducted current levels are decreased significantly. The confirmation of common mode conducted reduction will be presented in the next section.

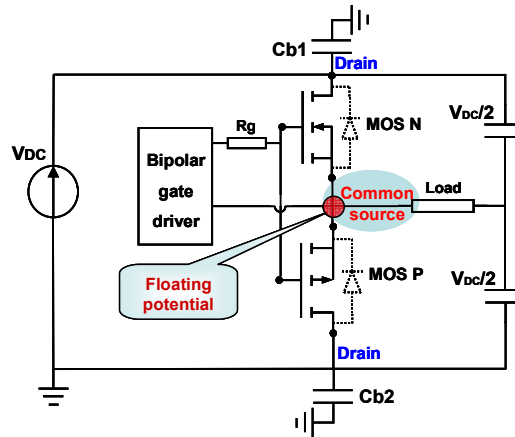


Fig.3: Complementary half-bridge inverter

### III. Simulation and experimentation results

#### A. Case study

In order to analyze the common mode conducted noise evolution as a function of the topology, two half-bridge inverter structures were simulated thanks to SIMPLORER and were implemented on metal isolated substrates (Fig.4). The conventional topology being made for reference is based on N type MOSFET devices and two bipolar isolated gate drivers. The complementary structure was built thanks to a pair of N and P type MOSFET transistors and only one isolated bipolar gate driver. This unique driver is able of driving both transistor gate electrode with the same control signal since the power devices are complementary N and P type transistors. Moreover, the two inverters were also designed to operate in a similar manner and to exhibit identical functionalities. Especially, in order to keep EMI sources and switching losses comparable in both cases, the switching transition dynamics were set to be alike. The parameters of the studied topologies are listed in the Table I.

In a first approximation, the parasitic capacitors can be deduced by:

$$C_b = \epsilon \cdot \frac{S_b}{e} \quad (1)$$

where  $\epsilon$ ,  $e$ ,  $S_b$  are respectively the dielectric permittivity, the dielectric thickness and the surface of the copper layer related to the backside of the transistor's package.

	Input voltage	Power devices	Gate resistances	Input Capacitances	Switching frequency
Conventional topology	150 V	MOSFET N: <i>IRFP240</i> – Package <i>TO247AC</i>	Rg high = 47 ohm Rg low = 47 ohm	2×470μF 250V	36 kHz
Complementary topology		MOSFET N: <i>IRFP240</i> – Package <i>TO247AC</i> MOSFET P: <i>IRFP9240</i> – Package <i>TO247AC</i>	Rg = 22 ohm		

**Table I: Global characteristics of the two inverters topologies**

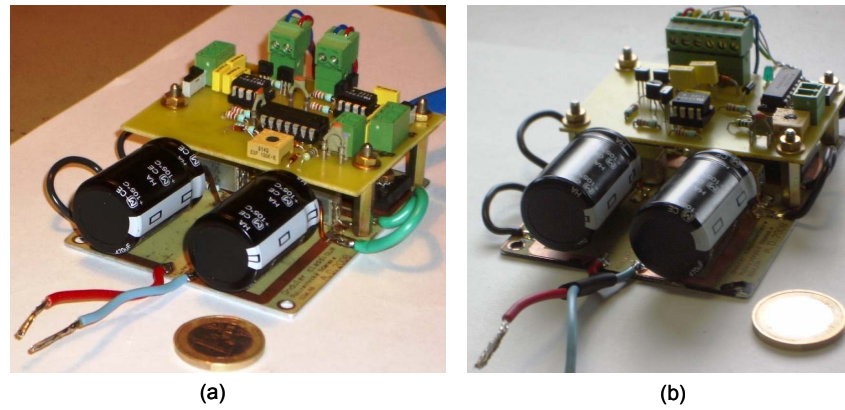


Fig.4: Two half-bridge inverters implemented. (a) Conventional topology. (b) Complementary topology

## B. Simulation and experimentation results

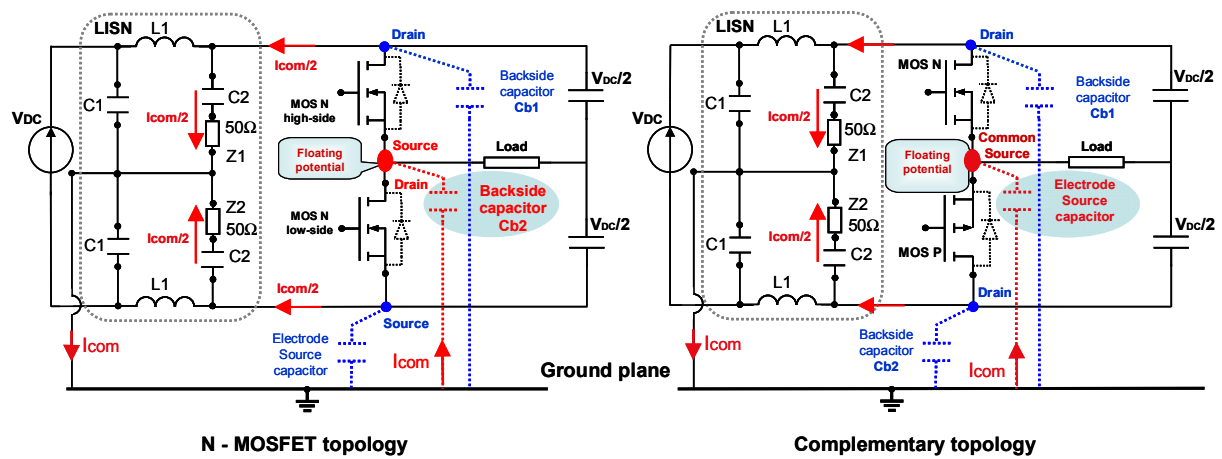


Fig.5: Half bridge inverter showing the common mode propagation paths

The topologies that were simulated are depicted on Fig.5. Besides the main parasitic capacitors approached in previous section, the parasitic capacitor of the source electrodes which is formed by the source tracks on metal isolated substrate (see Fig. 1) was also estimated and considered. This capacitance can be calculated as:

$$C_s = \epsilon \cdot \frac{S_s}{e} \quad (2)$$

where  $S_s$  is the surface of the track. Thus, the proportion between backside capacitance  $C_b$  and electrode source capacitance depends on ratio of backside's surface and source tracks' surface.

$$\frac{C_b}{C_s} = \frac{S_b}{S_s} \quad (3)$$

The common mode current can be defined by:

$$I_{com} = C \cdot \frac{dV_m}{dt} \quad (4)$$

A special attention has been paid to the evolution of the middle point voltage  $V_m$ . Since it is the main common mode source in the half bridge converter considered in this work, the converters were set such that in simulation and in practice, this middle point voltage exhibits comparable  $dv/dt$ . Then, the EMI sources are kept comparable for two topologies (Fig.6), making possible the comparison between the two converter topologies.

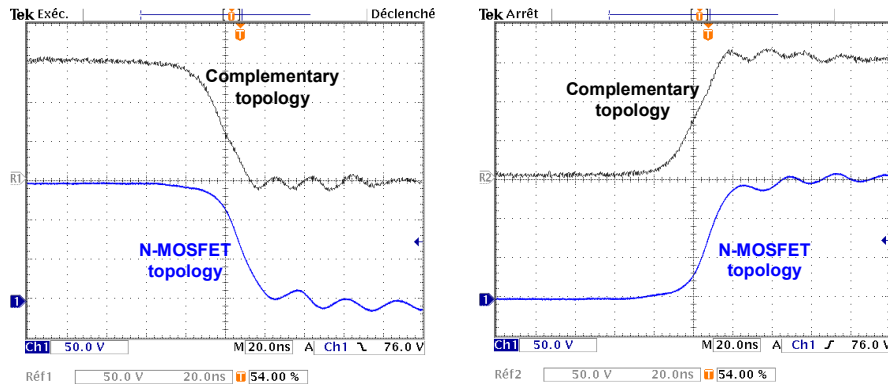


Fig.6: Switching voltage waveforms of the middle point of the inverter leg with respect to ground for both topologies

The frequency spectrums of the common mode currents obtained for both topologies and simulated with Simplorer are shown on Fig.7 (a). It is observed that the common mode current generated by the complementary structure is more than 25 dB $\mu$ A lower than in the conventional topology over a large frequency spectrum. This is due to the location of the main parasitic capacitors in the complementary topology. It leads to a considerable reduction of the parasitic capacitor located at the middle point of the inverter leg in the complementary structure. Since this capacitor is mainly dependent on the size and surface of the copper track necessary to connect together the sources of the transistors and the middle point to the load, its value can be reduced. Ideally, this copper track having a limited or even negligible thermal contribution, it can even be removed from the SMI substrate, leading to a greatly reduced parasitic capacitor. Of course, if this is possible with complementary transistors, this could not be made with the use of only N type transistors.

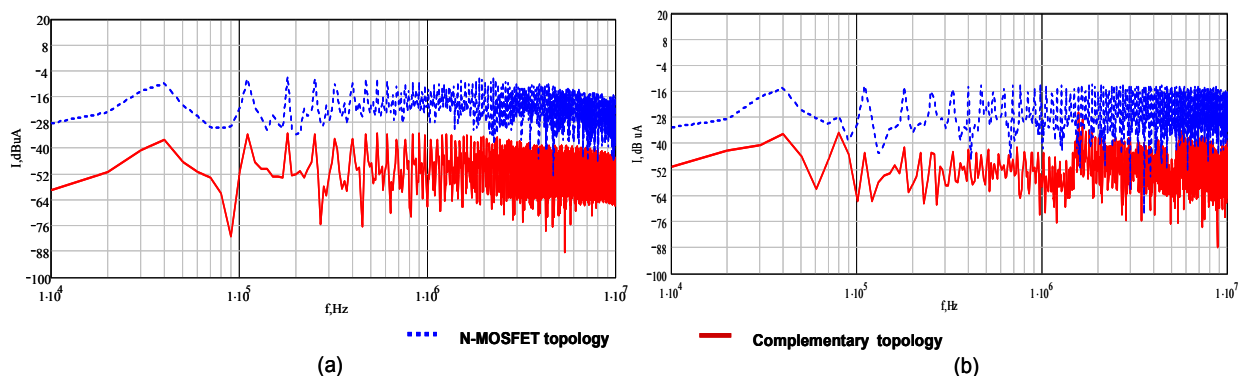


Fig.7: Frequency spectrums of the common mode current levels for both topologies (measured at ground LISN terminal [4][11][12]). (a) Simulation results. (b) Experimental results

A similar investigation was carried out in experiments where the source electrode of the inverter was not connected on the SMI substrate but directly from the pins of the chips. The experimentation results are given on Fig.7 (b). We can see that the simulation and experiment results are comparable (Fig.8), leading to a parasitic capacitor ratio between, drain and source in the range of 20 (as estimated in theory).

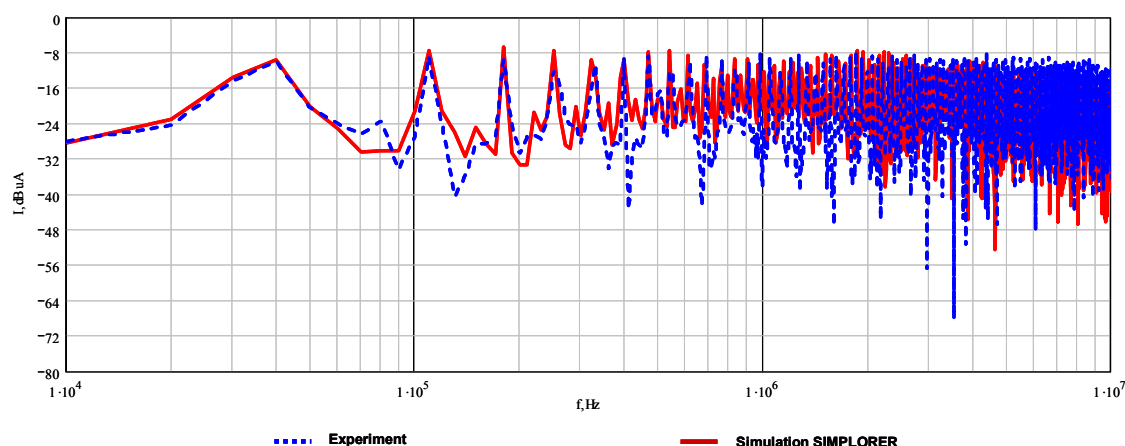


Fig.8. Difference of common mode current's frequency spectrum (for the conventional structure) between SIMPLORER and experiment results.

In order to show even more clearly the advantages offered by the complementary structure with respect to common mode EMI generation, standard measurements across LISN resistors [4][11][12] were carried out and the passive filters were designed and implemented to ensure that the two structures meet the EN55011 standard Class A. These topologies were set identical to ease the comparisons and it is showed on Fig. 9.

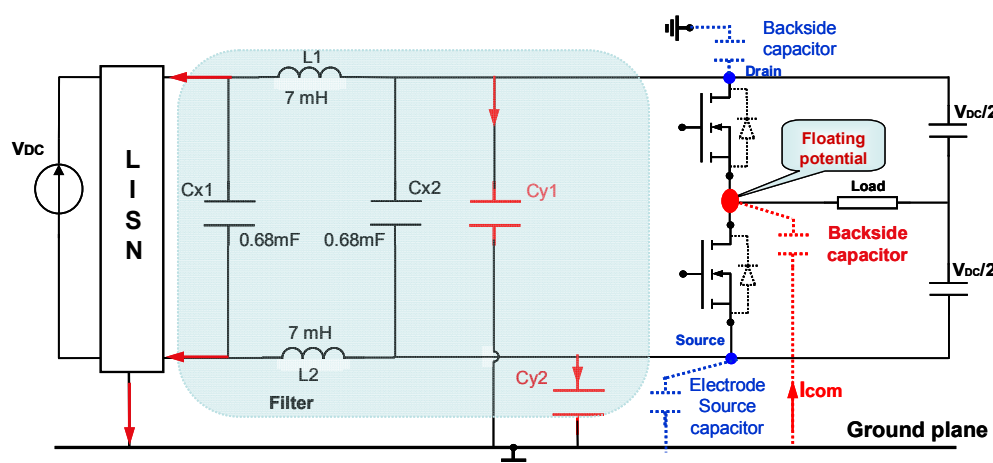


Fig.9. Conducted EMI noise filter topology

For that purpose, the same differential mode current filters ( $L1=L2=0,7\text{mH}$ ,  $Cx1=Cx2=0,68\text{mF}$ ) were built for two topologies. Indeed, complementary topologies are not acting on differential mode disturbance levels. On the other hand, each converter topology requires a different common mode filter such as  $C_{y1}=C_{y2}=133\text{nF}$  for the conventional inverter and  $C_{y1}=C_{y2}=10\text{nF}$  for the complementary topology. Therefore, we can see that a filtering ratio of 13,3 is required between the two common mode filters in order to comply with the regulation standards. The frequency spectrums of both topologies obtained in practice with and without EMI filters are presented on Fig.10.

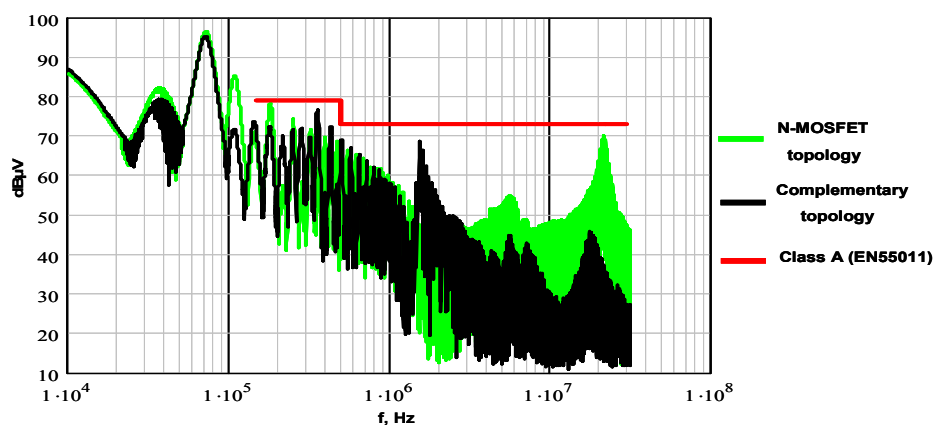


Fig.10: Conducted EMI frequency spectrum measurements with filter for both topologies (the voltage across the impedance  $Z_1$  of LISN) with and without EMI conducted filters

Since it is not realistic or even possible to implement common mode EMI filter with large  $C_y$  capacitors, the common mode EMI filter needed for the conventional topology would require normally the use of a common mode choke. This would result in an additional cost and additional losses. These results demonstrate the interest in considering complementary topologies as far as common mode EMI reductions are concerned. However, as it is well known, the introduction of P type transistors into a power electronic converter leads usually to the increase of the ON state losses and the reduction of the efficiency levels. Let's investigate this point in the next section of this paper.

Please note on Fig. 10 that common mode disturbances are simple to separate to differential mode disturbances. Indeed, in a half bridge inverter, common mode disturbances appear at each switching frequency multiple whereas differential mode noises appear at each multiple of twice the switching frequency. Therefore, it is simple to identify on the frequency spectrum the contribution of the common mode currents added to the differential mode currents on the global disturbance levels.

#### IV. Efficiency analysis

The main drawback of this approach corresponds to the extra losses introduced by the implementation of P type transistors with increased ON state voltage drops. This issue is investigated in details in practice in order to evaluate what is the price to pay as a function of the design and the operating conditions of the two types of inverters. Table II below summarizes a set of experimental efficiency measurements for the conventional topology and the complementary structure. Fig.12 are plotted the levels measured and reported in Table II. It is well known that in a converter, the ratio conduction losses over power flow increases linearly whereas the ratio switching losses over power flow is about stable as a function of power flow. Therefore, it appears that, as expected, when the conduction losses increase due to a larger power flow, the complementary structure is less efficient. As it could be expected, the complementary topology induces larger conduction losses. When the switching losses are in the range of the conduction losses, the decrease in efficiency is reasonable. However, for larger load levels, the losses generated by the complementary converter are twice larger than in a conventional converter.

In Table II, another test is presented where the complementary converter was built with a P type transistor twice as large as before (Fig.11). In this case, the conduction losses are reduced and are closer to the one of the conventional topology.

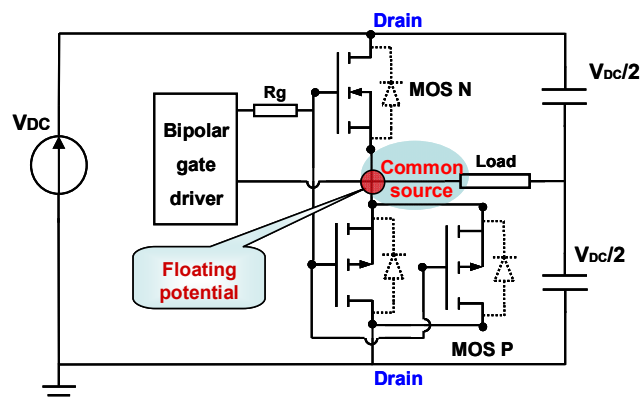


Fig.11: Complementary topology implemented with two parallel P-type MOSFETs

Input Power, W (at $V_{in}=150V$ )		50	100	200	300	400
Efficiency %	N-MOSFET topology	98.85	98.06	96.26	95.07	93.68
	Complementary topology (1 P-MOSFET)	98.04	96.14	92.82	89.37	85.66
	Complementary topology (2 parallel P-MOSFET)	98.45	97.10	94.21	92.49	90.65

Table II: Efficiency table as a function of the topology, the input power level and the number of P-MOS devices

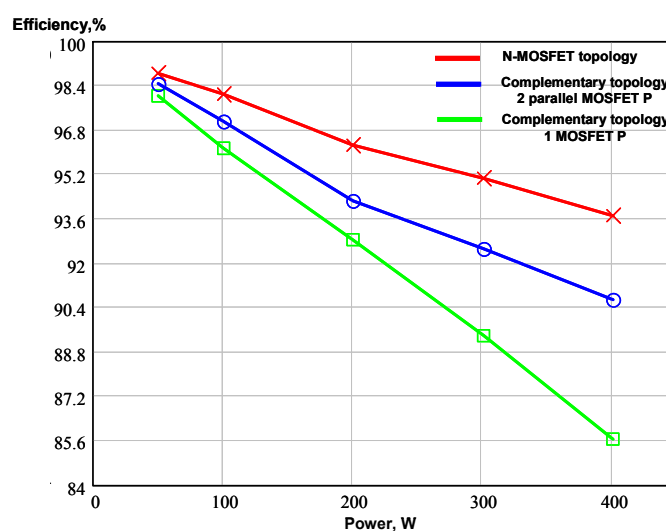


Fig.12: Plot of the evolution of the efficiency as a function of the topology, the input power level and the number of P-MOS

Moreover, the structure with two P type MOSFET associated in parallel does not degrade the EMI advantages of complementary structure highlighted in the previous sections because two backside (Drain) electrodes parasitic capacitors are connected in the DC bus whose potential is relatively stable. This can be seen on the Fig.13 where a new frequency spectrum of the conducted EMI is plotted when two P type MOSFET are used for the implementation of the half bridge inverter leg. It is shown that

the complementary topology including two parallel P type MOSFETs meet the EMI standard with the same passive filter as for the converter based on one P type MOSFET.

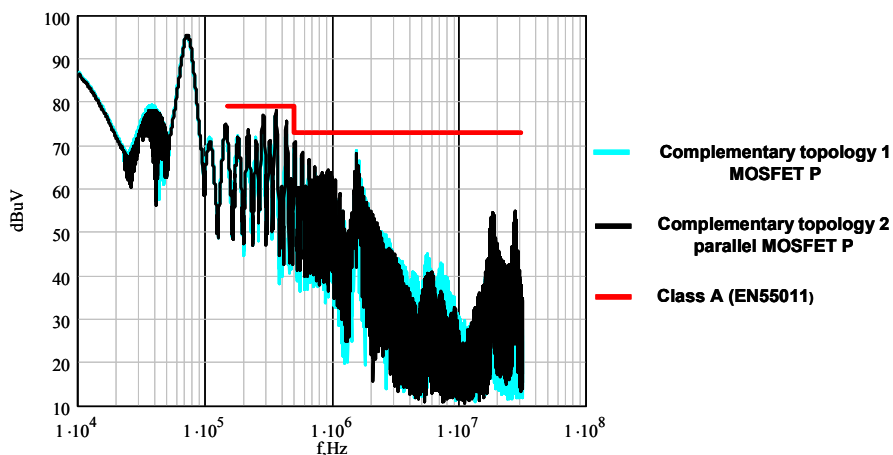


Fig.13: Conducted EMI frequency spectrum measurements with conducted EMI filter for both complementary topologies (the voltage across the impedance Z1 of LISN)

Therefore, great reductions on conducted EMI levels are obtained enlarging the size of a power device. In some applications, for low and medium power, replacing passive filtering elements with extra active silicon devices may lead to cost effective solutions and improved integration levels, especially if efficiency is maintained high enough by employing larger active devices. In some high voltage high frequency light load application, the work presented in this paper can offer an interesting answer for the reduction of the common mode current management and reduction.

## V. Conclusion

To conclude on this work, it is shown that common mode conducted EMI could be treated as a function of the topology of the converter and the type of device used for the implementation. Based on simulation and experimental results, the work detailed in this paper demonstrates that valuable reductions of common mode current levels and propagation paths could be achieved using complementary devices. As a function of the layout design of the converter, great reductions in common mode filtering needs can be obtained. However, this structural advantage must be balanced by the additional conduction losses introduced by the P-MOS transistor implementation. It is also exhibited that the additional conduction losses generated by P-MOS transistor could be limited using a larger power device. This is obtained without altering the improvements obtained on the EMI behavior of the complementary structure.

This work shows that possible modifications on active device size and type enable to reduce filtering requirement for standard compliance. This means that in an effort of converter integration, more active devices may be used to limit the sizes of passive devices which are harder to integrate. It is then a question of compromise as a function of efficiency, integration, cost and global performances. In some applications, especially but not only under reduced power levels, the converters implemented thanks to complementary power devices may be preferred.

It is now a question of power device optimization. Indeed, it is simple to find any type of N type device at any voltage and power level. It can not be said the same thing for P type power devices. Especially, as far as IGBT are concerned, it could be of interest to develop P type power devices to see if the compromise between the switching and the conduction losses could be set differently. Finally, the global design and optimization of the converter could be based on complementary power devices.

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