



HAL
open science

Design and Realization of Autonomous Power CMOS Single Phase Inverter and Rectifier for Low Power Conditioning Applications

Olivier Deleage, Jean-Christophe Crébier, Yves Lembeye

► **To cite this version:**

Olivier Deleage, Jean-Christophe Crébier, Yves Lembeye. Design and Realization of Autonomous Power CMOS Single Phase Inverter and Rectifier for Low Power Conditioning Applications. EPE 09, Sep 2009, Barcelone, Spain. hal-00422518

HAL Id: hal-00422518

<https://hal.science/hal-00422518>

Submitted on 7 Oct 2009

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Design and Realization of Autonomous Power CMOS Single Phase Inverter and Rectifier for Low Power Conditioning Applications

Olivier Deleage, Jean-Christophe Crebier, Yves Lembeye
Grenoble Electrical Engineering Laboratory (G2Elab)
ENSE3 - BP 46 – 38402, Saint-Martin-d'Hères Cedex, France
Tel.: +33 / (0) – 4.76.82.63.51, Fax: +33 / (0) – 4.76.82.63.00
E-Mail: deleage@g2elab.grenoble-inp.fr
URL: <http://www.g2elab.grenoble-inp.fr>

Keywords

Monolithic power integration, High frequency power converter, MOSFET, Power integrated circuit

Abstract

This paper deals with the design, the realization and the characterization of an integrated converter for low voltage and low power, isolated applications (3.3 V, 1 W). It is based on the association of two generic silicon dies performing DC to AC and AC to DC operations. The power dies are designed in CMOS technology and operate at high frequency (1 MHz) and high efficiency. This high power density realization includes the power circuit and the control electronic. The integrated conversion structure can operate as an inverter or as a rectifier in a wide range of power flows and input voltages. Three important issues are addressed in this paper: design of the power part at high efficiency, reduced consumption of the control electronic and the gate drivers, and implementation with reduced parasitic behavior. The practical implementation and characterization are also addressed in a second part. First tests are carried out with packaged dies on PCB boards, in order to simplify the implementation. The efficiency of the inverter reaches up to 92% as a function of input voltage with these conditions. The second experimental investigation is a full DC to DC converter implemented with two CMOS power dies (one inverter and one rectifier) together with an HF transformer and an output LC filter. This article ends with the study of the packaging in order to minimize parasitic elements, such as resistances and inductances, which can be very harmful for the global efficiency of our micro-converter.

Introduction

In order to increase the efficiency of the power conversion levels, researches are leading to improve the characteristics of actives and passives components. These progresses allow to increase the switching frequency of the converters, allowing to reduce the size of the passives components, and in consequence, the size of the global converter. High switching frequency implies that the characteristics of the environment of the components are also important. Indeed, the parasitic elements such as resistance and inductance of the inter-connexions are non-negligible when the power converter works at high frequency and low voltage levels, even if each component is designed for this operating point. That is why the packaging of the converter has to be taken into account, to reduce these parasitic elements. As a consequence, the efficiency of the micro-converter can reach a high level if care is paid to the integration and the packaging.

This article deals with the design of monolithically integrated power converters [1]. In particular, the study and the design of the silicon dies are detailed. These dies include all the power components required for a single phase inverter, their optimized gate drivers [2, 3] and the electronic command. In a second part, experimental tests are carried out with a single die operating as an inverter and implemented with a regular packaging in a SOIC package, with wire bonding inter connexions.

The operation of the converter is presented based on experimental results of the integrated inverter. This part is followed by the implementation of a full DC-DC converter with electrical isolation. Packaging of global DC-DC converter is studied to optimize efficiency in a third part.

Design of the silicon die

The goal of this work was to design a classical power conversion structure including an HF transformer for electrical isolation. Applications of such integrated converter could be the supplies of the gate drivers in higher power converters or in any case when a small and isolated power supply is needed. The topology of the converter has been chosen to minimize the size of the HF transformer which remains a limiting point of the monolithic integration of the whole converter. Therefore, we have chosen to use a classical full bridge inverter plus rectifier, based on numerous active devices, which could be integrated at limited design cost. Moreover, the selected topology includes the maximum active part and the minimum number of passive components, in order to optimize the size of our micro-converter. That is why a full bridge converter was studied here, as shown in figure 1.

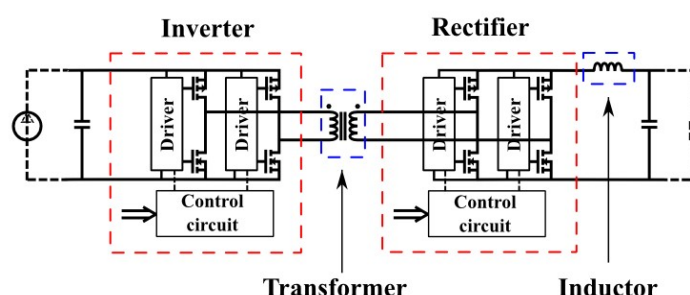


Fig. 1: Topology of micro-converter

Power MOSFET and drivers

First of all, the technology of the active parts was chosen regarding to several criteria, such as efficiency and operating switching frequency possibilities. An analytical study was carried out to optimize the efficiency of the power structure, where the conduction and switching losses were estimated (equation (1)). The acceptable level of losses chosen, involve the choice of the technology and the switching frequency of our structure. As a result, the 0.35 μ m AustriaMicroSystems technology and a 1 MHz frequency were chosen to obtain, in theory, an efficiency of 98% for the power part of the converter considering nominal voltage and current respectively equal to 3,3V and 0,3A.

Conduction losses	Switching losses
$P_{cond\ cell} = \frac{1}{2}(R_{DS_P} + R_{DS_N})I^2$	$P_{com\ cell} = \frac{1}{2}(C_{ISS_N} + C_{ISS_P} + C_{DS_N} + C_{DS_P})V_{DD}^2 f$

(1)

These expressions were filled up with resistance and capacitance of the MOSFETs as a function of their gate width (for a NMOS : $R_{DS_N} = K_{R_N}/W_N$, $C_{ISS_N} = K_{ISS} * W_N$ and $C_{DS_N} = K_{DS} * W_N$ taken from [10]). Moreover, PMOS gate width was chosen 3 times bigger than NMOS gate width to get similar on-state resistance. Then, the derivative of total losses expression gives the optimal gate width which depends on the technology characteristics and the specifications of our converter (equation (2)).

$$W_{N\ optimal} = \sqrt{\frac{I^2(K_{R_P} + 3K_{R_N})}{12V_{DD}^2 f(K_{GS} + K_{DS})}} \quad (2)$$

Our specifications are a nominal voltage of 3.3 V under 1 W power load, which give us the value of the optimal channel width. K_{RP} , K_{RN} , K_{GS} and K_{DS} are parameters depending on the technology. As a result, we obtain the following values for the channel widths for our power MOSFETs:

$$W_N = 38000\mu\text{m} \text{ and } W_P = 98000\mu\text{m}.$$

Now, we have to command these power MOSFETs. Because important channel widths have been chosen, driving these MOSFETs requires a specific care. Indeed, if the charge time of their gate capacitance is too important, switching losses would be too high. In order to enhance the drive of these power MOSFETs and to ensure the best switching performances, we have to design several amplification stages [4][5]. Moreover, CMOS technology presents short-circuits during switching transitions, that's why we have to pay attention on time shift between power NMOS and PMOS gate command, to manage a short dead time between their conduction times.

In order to satisfy these criteria, a driver topology has been proposed and is presented figure 2.

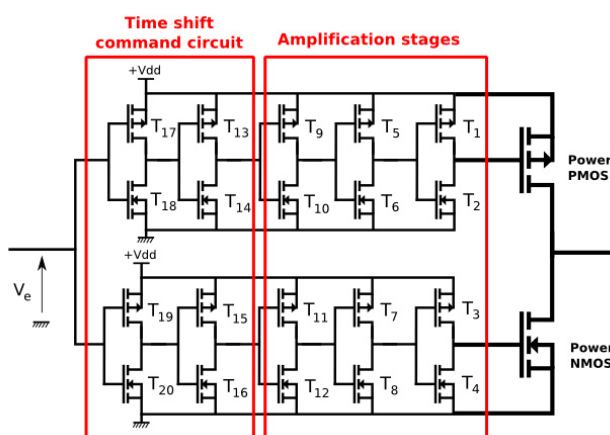


Fig. 2: Topology of drivers

In this driving topology, it is important to notice that the power MOSFETs are driven by their own gate drivers allowing to separate switching events and to optimize the dead time between the commutation of the two power devices. The design of each stage have to start from the largest stage (the nearest to the power MOSFET). Indeed, this first stage is critical with respect to converter global switching losses. Oversized first amplification and driving stage would generate undesired additional and superfluous switching losses, but if this stage is under-designed, the power MOSFET will switch slowly. The figure 3 presents the optimal channel width of the first amplification stage transistors, which achieves the best compromise between size and losses.

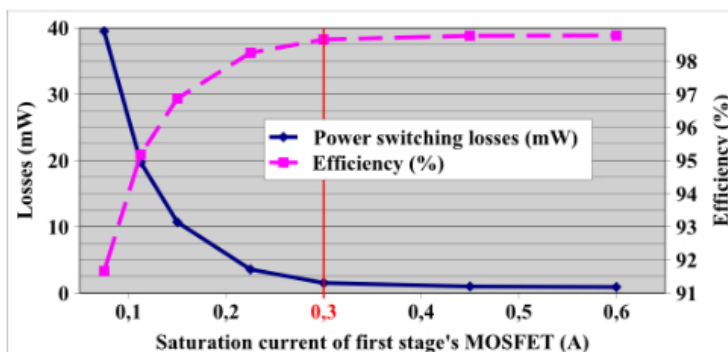


Fig. 3: Design of first amplification stage of drivers (simulations results) (T1 - T4). Saturation current is a parameter function of transistor channel width [10]

The second stage is designed regarding the input and output dynamics of the first stage. Indeed, the first stage is still too big to ignore its short-circuit duration, but a separate command of NMOS and PMOS is too complex to implement too. To reduce the short-circuit current, we designed the on-state resistance of second stage in order to have a larger switching time at the output than at the input. By this way, the first stage has the time to switch before the voltage, which is at the origin of the short circuit, increases (figure 4). Indeed, the switching of the first stage can be dissociated in three phases: first, the input voltage of the first stage is higher than threshold voltage of PMOS (phase 1). Then, when the input voltage of the first stage is between the threshold voltage of NMOS and PMOS (phase 2), the two transistors are on-state causing a short circuit. We can notice that the third stage is not represented here and the stage 2 is supplied with a ideal voltage supply for his design. To limit the impact of this short circuit, we have, in our design, to choose the widths of transistors T7 and T8 to ensure a low on-state resistance, in order to have an input dynamic faster than the output dynamic of the first stage. This design is possible due to the large parasitic gate capacitance of the following stage (the power MOSFET). So, The NMOS of first stage (T4) is off-state before the output voltage of this first stage becomes too high (phase 3).

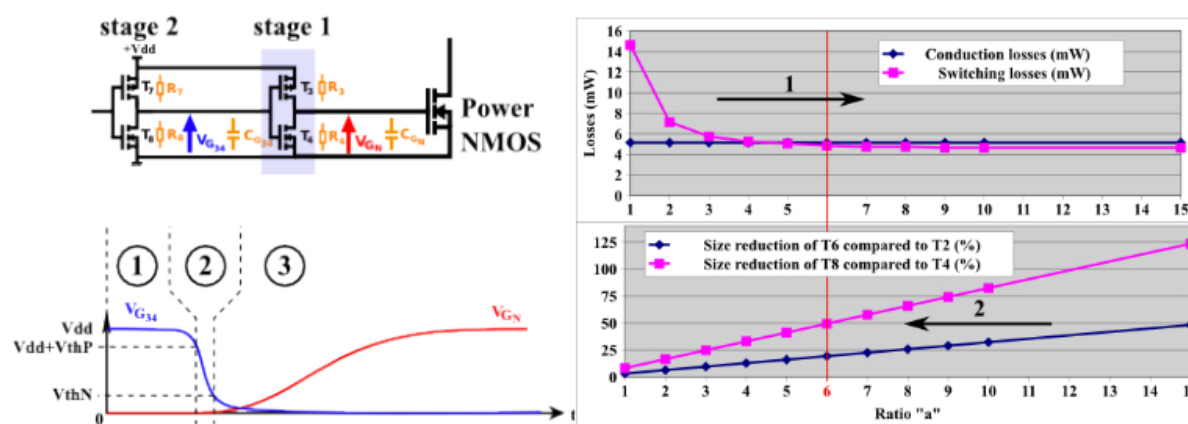


Fig. 4: Design of second amplification stage of drivers (T₅ - T₈). Qualitative presentation of phase 1 to 3 gate signals for stages 1 and 2.

Sizes of third stage MOSFETs are simply designed regarding the global efficiency of the power stage as shown in figure 5, on the left.

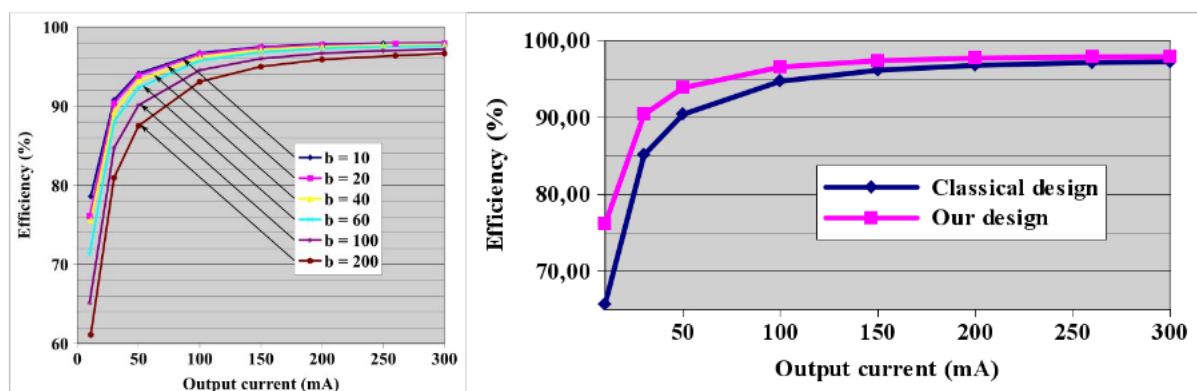


Fig. 5: Design of third amplification stage of drivers (T₉ - T₁₂) and comparison between a classical design and our design

To control the phase shift time between power NMOS and PMOS to avoid the short-circuit of the CMOS harms in power structure, we have to design a circuit which creates a dead time between power MOSFETs on states. This dead time has been designed thanks to transistors (T₁₃ - T₂₀). These stages

are not identical in order to introduce a delay for the power MOS concerned at each half period. This has been carried out realizing inverting stage with different on-state resistances for the transistors T_{18} and T_{19} .

The design of this circuit which creates the phase shift time has to pay attention to the possible conduction of the body diodes of the power devices. Indeed, their ON state losses are greatly higher at these operating voltage levels. As a result, the design of this circuit was realized regarding the global efficiency of the power structure. In consequence, the optimal design was obtained with a short time during which current flows through the diodes.

In order to validate our design, and to demonstrate the interest of this specific gate driver, its operation has been compared with classical design. The classical design consist in reducing each stage by a factor of ten, with the same total number of stages than in our design. The figure 5 (on the right) shows the efficiency levels of these two different designs as function of the output current level.

We can conclude that our design allows to preserve a higher efficiency than the classical design for any output current, specially for low values.

Electronic command

In order to control the switching transitions of the power structure, an electronic command is monolithically integrated on the power die. This digital circuit has been described in VHDL language, synthetized, and then, implemented in AMS technology. The main goal of this circuit is to control the micro-converter in a project called “network of micro-converter” leaded in our laboratory [6]. Without entering deeply in the functionality integrated in this control part, a block diagram is depicted on figure 6 [6].

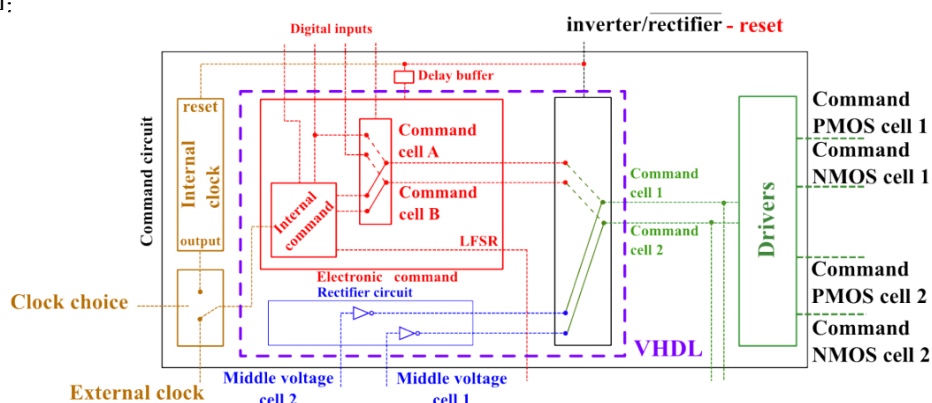


Fig. 6: Topology of the digital circuit monolithically integrated with the power devices

This circuit allows to choose if the converter must operate as an inverter or a rectifier. Indeed, the power structure is similar in these two cases, only commands are different, as shown figure 6. Besides, an internal clock is also monolithically integrated in order to prevent from the use of external clock circuit. This clock is realized with a ring oscillator at a frequency of 120 MHz. This topology of oscillator can be completely integrated at limited cost, the only limitation being the stability of the oscillator.

The consumption of this circuit has to be as reduced as possible regarding the global efficiency of the micro-converter. Simulation results show that the global consumption of the control circuit is about 5 mW to compare to the 1W nominal power of this die.

Results of design

The most important issues of our active structure have been addressed, therefore, the design of the layout has been carried out and is presented figure 7.

Power pads are designed to allow flip-chip connexion of the die, and to minimize parasitics elements [7].

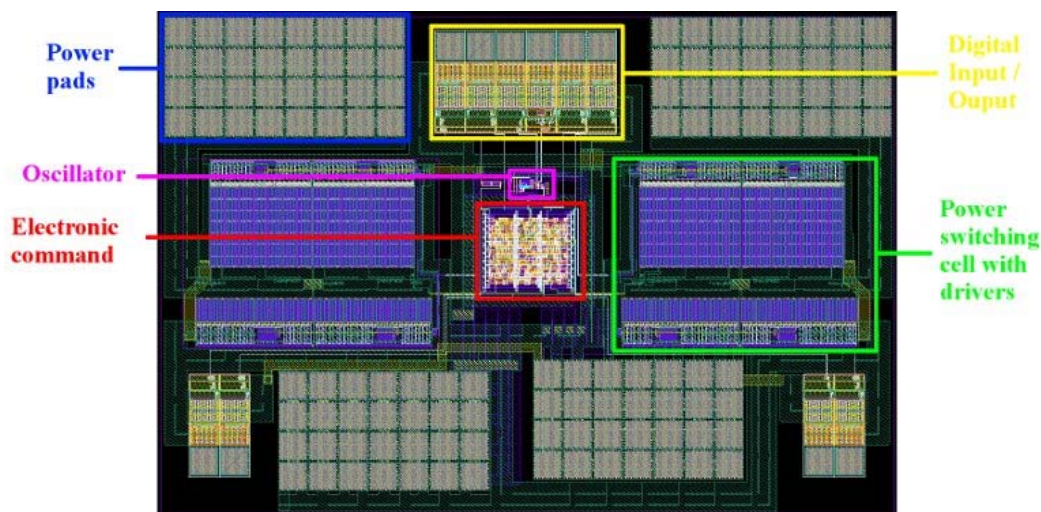


Fig. 7: Layout of our micro-inverter/rectifier

Experimental results

Inverter on SOIC 16 package and PCB board

In a first tests campaign, we have implemented an inverter packaged in a SOIC 16, and soldered on a PCB board, as shown figure 8.

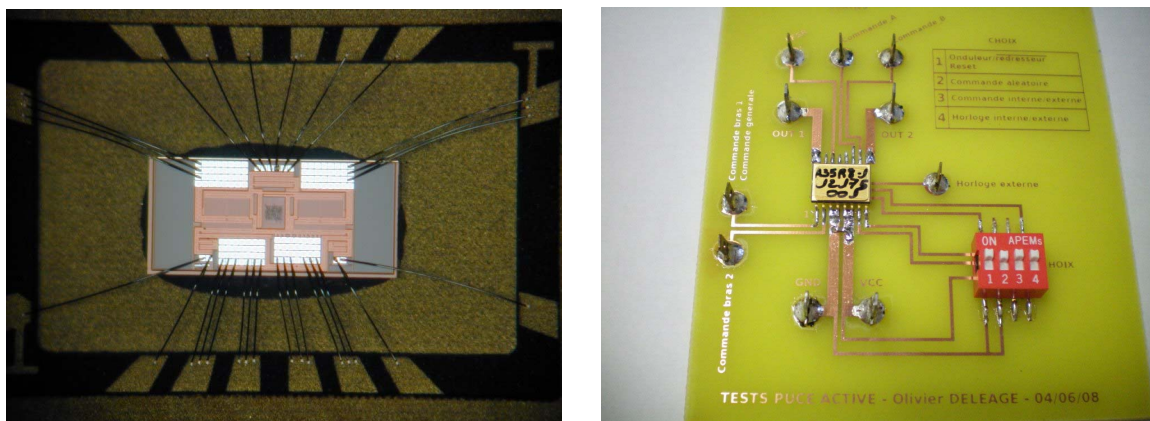


Fig. 8: Silicon die on SOIC package and PCB implementation for inverter tests

This environment exhibits non-negligible parasitic resistances and inductances, which decrease reachable efficiency levels, but it's the simplest way to test our micro-inverter. The figure 9 shows the efficiency obtained as a function of the duty cycle of the inverter command, for several voltages, and for a nominal resistive load (10 Ω).

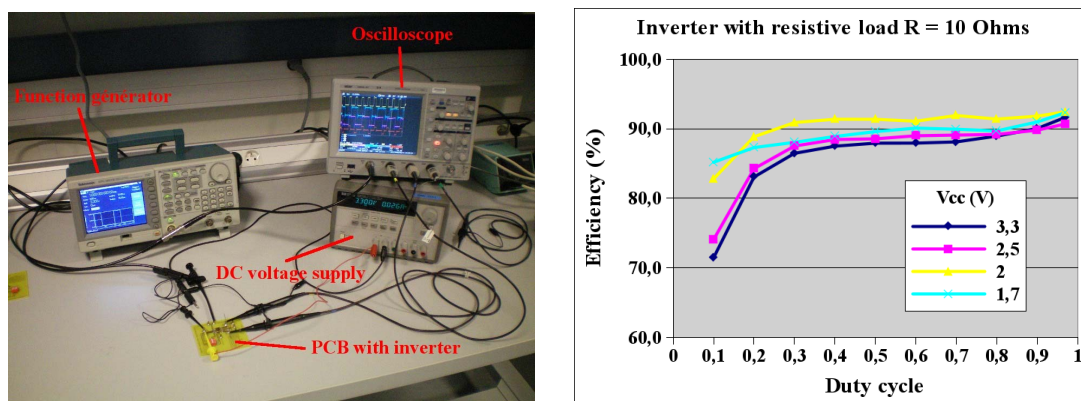


Fig. 9: Experimental implementation and efficiency of inverter as a function of duty cycle.

The efficiency measured is lower than the expected one due to the parasitic elements introduced by the wire bonds and the copper tracks which present non-negligible resistances and inductances. Moreover, these results take into account the consumption of the electronic command which is of course directly supplied through the power part.

Full DC-DC micro-converter on SOIC 16 and PCB board

After validating the correct operation of the inverter, we can implement a full DC-DC converter, as shown in figure 10.

This DC-DC converter is realized with two power dies packaged in SOIC package, one for the inverter and one for the rectifier. The inductive parts (transformer and filter inductor) are realized on thin substrates of Kapton.

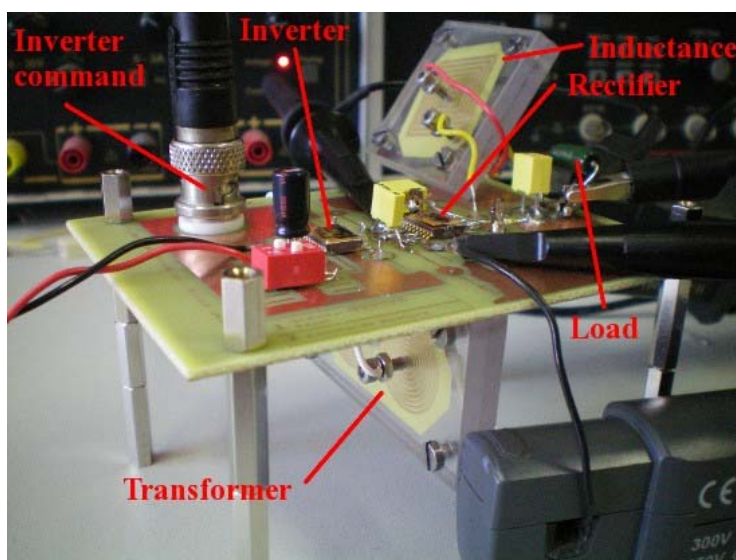


Fig. 10: Full DC-DC micro-converter on SOIC packages and PCB

The transformer and the inductor have been designed to obtain sufficient values of magnetizing inductance and self-inductance, respectively $1,5\mu\text{H}$ and $2\mu\text{H}$, without magnetic core to simplify their implementation. However, in this case, DC resistance and skin effect are not negligible (figure 11).

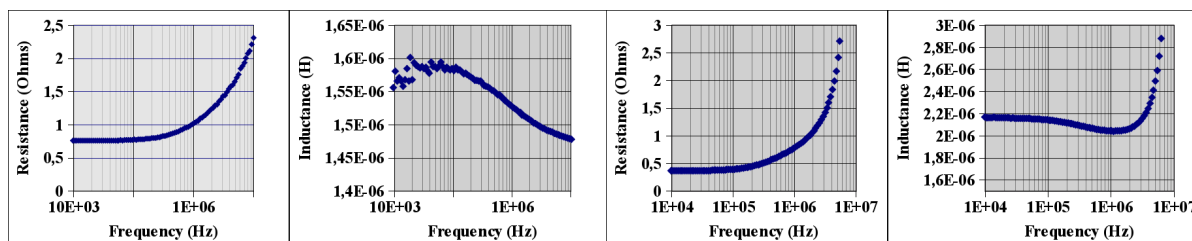


Fig. 11: Characteristics of inductive parts (transformer on the left, inductor on the right)

This non-optimal environment is fully functional as it can be seen on figure 12 and it provides encouraging results. Indeed, the efficiency of global DC/DC converter reaches 52%. Since the passive elements exhibits quite conduction losses, we consider these results encouraging, the efforts having to be focused now on magnetics and parasitics.

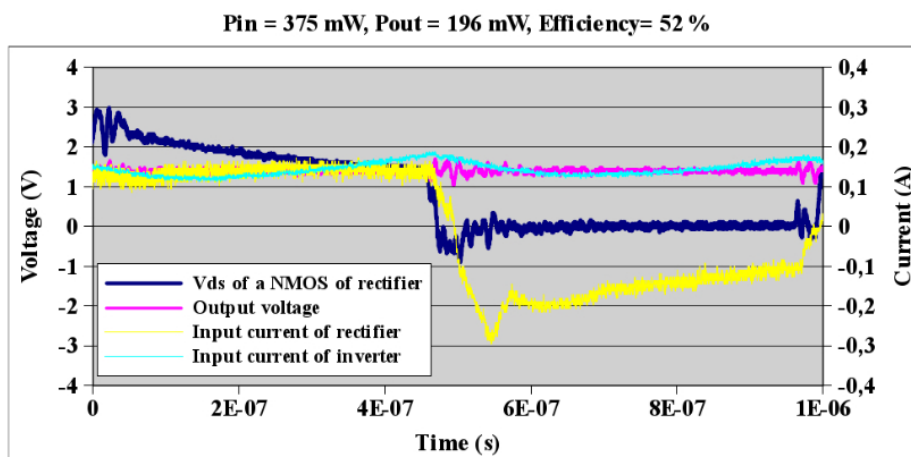


Fig. 12: Waveforms of the full DC-DC converter over a switching cycle (1MHz)

Some problems appeared during the tests, mainly due to the parasitic elements created by the copper inter-connexions. Indeed, at nominal input voltage (3.3 V) important voltage oscillations across the power MOSFET have been observed, and over-voltages in the range of 10 V could be reached. These voltages correspond to the breakdown voltage of the transistors implemented in AMS 0,35 μ m technology. In consequence, the previous results, shown figure 15, were realized at an input voltage of 2.6 V. Moreover, conduction losses estimation in inductive elements shows that the efficiency can reach up to 74 % if the transformer serial resistance at 1 MHz and inductor DC resistance are about 0.1 Ω . However, in this test, the resistance of each windings of transformer is about 1 Ω at 1MHz, and the DC resistance of inductor is about 0,4 Ω . Besides, harmonics are not taken into account in this estimation. This explains why the total efficiency of our structure was only 52%. Extra work is needed toward the optimization of the passive elements but also on the integration and interconnects of the components.

Packaging of final micro-converter

In order to reduce the impact of the interconnect parasitic elements and their consequences, highlighted with the tests on SOIC packages and PCB, a special packaging should to be implemented. Several topologies are possible, but in this paper, we will focus on a technological solution based on Kapton layers and silicon monolithic integration.

Micro-converter on Kapton board

First, the easiest topology which can reduce consequently the parasitic elements is based on a Kapton layer on which are implemented the passive component windings but also the interconnects for the active power dies. This topology consists in using a thin Kapton substrat ($25\mu\text{m}$), and printing on each side, copper tracks in order to incorporate windings of transformer and inductor. The figure 13 (on the left) shows a 3D view of such a micro-converter.

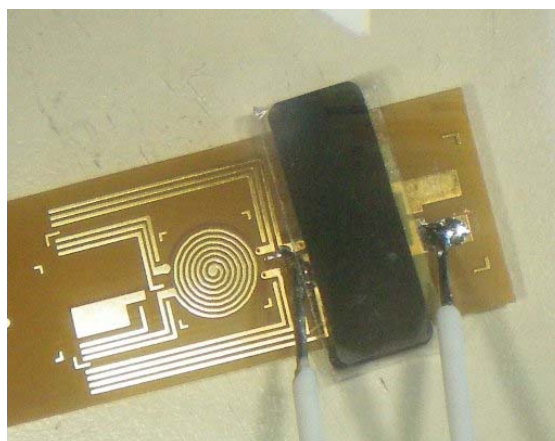
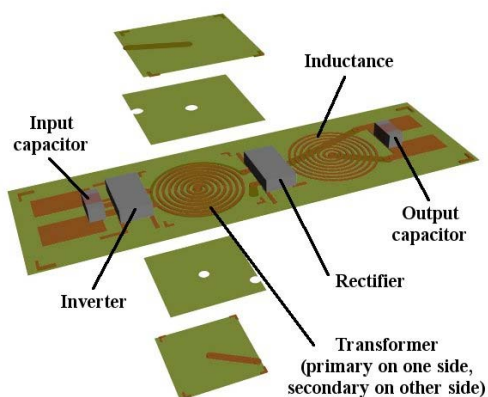


Fig. 13: Full micro-converter on $25\mu\text{m}$ Kapton board ($7\text{mm} \times 22\text{mm}$) and measure implementation of the inductor of the micro-converter implemented with the magnetic core.

The active parts are connected with the flip-chip technique on the Kapton substrate. This approach avoids to use wire bonds, which may exhibit excessive resistive and inductive behaviors, and which are relatively breakable in comparison to flip-chip connexion.

With a single layer of copper on each side, the transformer winding topology must be based on a double layer structure, in order to contact the center of windings. That is why we can see four additional layers for the transformer, two layers with copper tracks, and two layers to isolate windings and additional copper tracks.

Without magnetic circuit, these windings (which external diameter is about 5mm) have too low values of inductance for our micro-converter (about 100nH), that is why we have to add magnetic circuit on each side [8].

The figure 13 (on the right) shows the magnetic circuit added to the inductor and isolated using a $25\mu\text{m}$ Kapton film. The magnetic circuit used in this test is realized using 3F3 Ferroxcube material.

The characterization of the inductor is presented on figure 14. The component exhibits sufficient value of inductance, about $1\mu\text{H}$, but the serial resistance is increased due to the losses in the ferrite core beyond 100kHz and higher losses in windings.

With a better magnetic core, like 3F4, we can work at a higher switching frequencies (due to reduced losses [9]), even if the inductance value is slightly decreased.

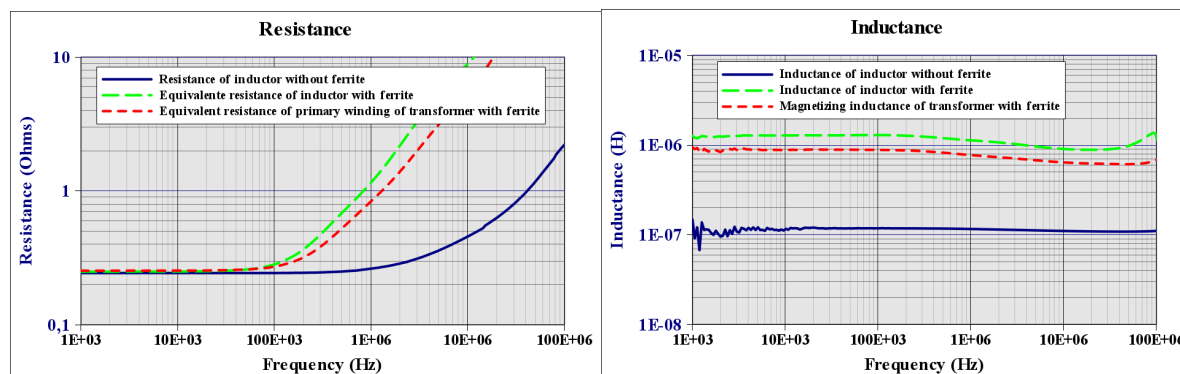


Fig. 14: Results of characterization of inductor and transformer with magnetic circuit.

For the transformer, the accumulation of thin layers is harmful for the air gap between the two magnetic layers. That is why we were not able to reach the same value for magnetizing inductance than for the inductor, as shown in figure 14. But, as a benefit, the magnetizing field is lower, that implies a reduction of equivalent resistance (due to the reduction of losses in ferrite and in windings).

Conclusion

The paper has presented the design of the active parts as well as their optimization in simulation. Their practical implementation has demonstrated the limits of regular and classical packaging and interconnect techniques. The first experimental results (with silicon dies in SOIC package and soldered on PCB) has shown that the passive elements and the parasitic elements didn't allow to reach a good efficiency (only 50% whereas up to 70 or 80% were expected). That is why a care must be paid on the packaging of the devices but also on the passive components. First elements of packaging on Kapton substrate was depicted, with experimental results concerning the passive parts to associate with the active parts designed and described in this paper.

References

- [1] J.-C. Crebier, Y. Lembeye, H. Raisigel, O. Deleage, J. Delamare, and O. Cugat, « High Efficiency 3-Phase CMOS Rectifier With Step up And Regulated Output Voltage - Design And System Issues For Micro Generation Applications », Design, Test, Integration and Packaging 2007, Stresa, Italy.
- [2] Katayama, Y. Edo, M. Denta, T. Kawashima, T. Ninomiya, T. "Optimum design method of CMOS IC for DC-DC converter that integrates power stage MOSFETs" Power Electronics Specialists Conference, PESC 04.
- [3] Chandrakasan, A.P. Brodersen, R.W. "Minimizing power consumption in digital CMOS circuits", Proceedings of the IEEE, Apr 1995
- [4] Volkan Kursun, Siva G. Narendra, Vivek K. De, Eby G. Friedman, « Low-Voltage-Swing Monolithic dc-dc Conversion », IEEE TCAS—II: Express briefs, vol. 51, no. 5, may 2004
- [5] Volkan Kursun, Siva G. Narendra, Vivek K. De, Eby G. Friedman, « High input step-down DC-DC converters for integration in a low voltage CMOS process », IEEE Computer Society, 2004
- [6] Ha Dang Thai, Olivier Deleage, Hervé Chazal, Yves Lembeye, Jean-Christophe Crebier. « Design of Modular Converters : Survey and Introduction to Generic Approaches ». Applied Power Electronics Conference 2009, Washington DC, 2009.
- [7] Brock LaMeres, Sunil Khatri, « Broadband Impedance Matching for Inductive Interconnect in VLSI Packages », International Conference on Computer Design 2005 (ICCD'05), proceeding.
- [8] S.C. Ó. Mathúna, T. O'Donnell, N. Wang, K. Rinne "Magnetics on Silicon: An Enabling Technology for Power Supply on Chip" IEEE Transactions On Power Electronics, VOL. 20, N° 3, May 2005
- [9] Datasheet of 3F3 and 3F4 : <http://www.ferroxcube.com/prod/assets/powapp.htm#power>
- [10] AMS data sheet of C35B4 technology