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# Automatic Layout Optimization of a Double Sided Power Module Regarding Thermal and EMC constraints

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**Abstract** – This paper presents an automatic layout process for power electronics integrated modules. The chip position and power layout is automatically generated according to the best EMC/Thermal trade off. Optimization techniques use simple but fairly accurate EMC and Thermal models, presented in this paper. The proposed method is illustrated on a 4 legs 2kW inverter used for aircraft applications. The realization will use double sided technology.

**Index Terms**– Electromagnetic compatibility, Electrothermal effects, Power Electronics, Printed circuit layout, Semiconductor device packaging,

## I. INTRODUCTION

Power electronics integration is one of the major developments of modern power electronics. After a first period of technological maturation, several products are now available. The new challenges consist now in optimizing integrated devices, either to use the technology at its maximum performances, or to decrease cost, weight or volume, what is especially important in embedded systems, such as aircraft applications which are a new driver for integrated power electronics [1].

Among the various problems to be solved when building integrated power modules, thermal and ElectroMagnetic Compatibility aspects (EMC) generate strong constraints: on the one hand, the chip temperature must be as uniform as possible, to avoid hot regions and to use the cooling system as the best. On the other hand ElectroMagnetic Interferences (EMI) must be reduced at minimum values. For a given switching speed and operating frequency, the first point is clearly linked to the dies position, whereas the second one is governed by the choice of the power layout. Consequently, these two thermal and EMC aspects cannot be dissociated. For instance, chips located close together reduce the surface of the layout and thus EMC problems, but thermal coupling may increase the overall chip temperature, if they are wrong used. Another bottleneck is the difficulty of providing easy external connection outside the power module. This originates strong constraints on the layout, and often governs the power layout design, despite any EMC or thermal consideration.

The aim of this paper is to propose an automatic optimization technique, and the associated models, in order to handle such complex problems: the optimal chip position and the associated layout will be automatically determined, based on thermal and EMI criterion. All constraints related to the technological realization and the disposition of the external connection will be taken into account. The proposed example, a 2kW inverter for aircraft application, realized in double sided technology [2-3] will be presented in section II. Section III will detail the optimization models, to account for both thermal and EMC aspects. Optimization results will be presented in section IV.

## II. THE STUDIED POWER MODULE IN DOUBLE SIDED TECHNOLOGY

### A. Integrated Topology

The studied power module has to achieve a three phases inverter function: the DC bus is 540V and the switching frequency is 20kHz. A four leg inverter topology has been chosen. Due to the quite low current (a few tens of amps), the power switches can be built using single IGBT and Diode chips per phase. Therefore, the problem is to determine the location of 8 IGBT and 8 Diode dies, as well as the associated layout. Due to industrial constraints, the DC bus access and the phase output must be located on different sides of the power module.

### B. Double sided Technology

The technology chosen for integrated inverter realization is the double sided technology [2-3]. It brings several interesting features, such as a better chip cooling by limiting the number of interfaces from silicon component to cooling fluid, and also reduced interconnection stray inductances, using a stacking of chips and substrates. Wire bondings are removed and replaced by soldered connection (metal bumps), as illustrated Fig.1. An external package is added around the double sided technology, to fit with aerospace requirements (protection against environment, ...) (Fig. 2.). To help in understanding the layout, Fig. 3 shows the different tracks connecting the chips on both substrate sides.

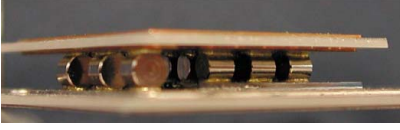
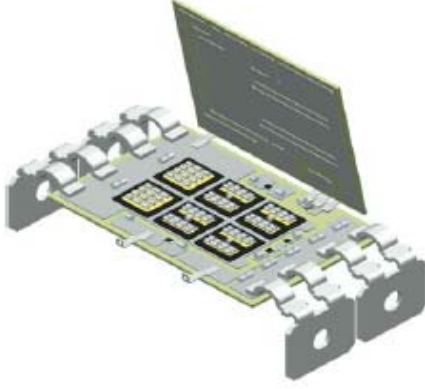


Fig. 1. Double sided technology. top: example of power switch – Bottom metal bumps.

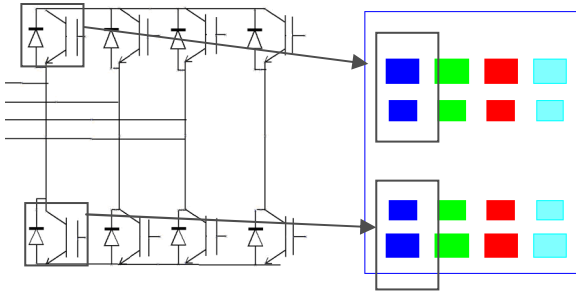
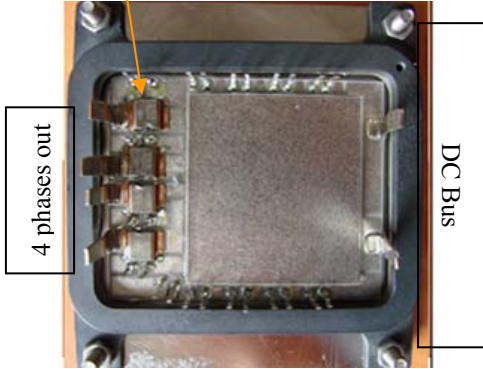
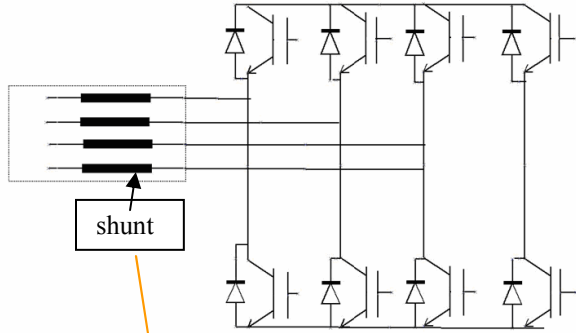


Fig. 2. The chips and associated substrates are integrated in a conventional package, fitting with aerospace requirements.

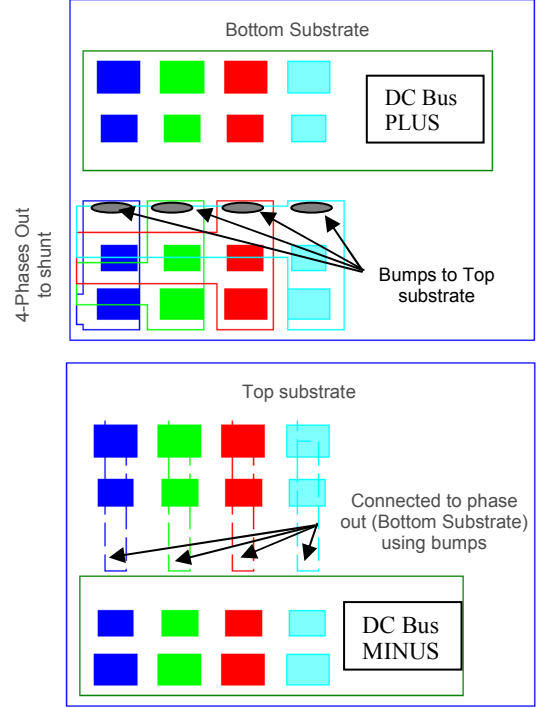


Fig. 3. Top and Bottom substrates with chip location, DC Bus and phase out tracks. Middle point connections are linked to bottom tracks using bumps.

To simplify the description, the "Phase out" tracks have been described using simple shapes, and cross over are allowed. Obviously, actual realization will have to provide bonding solutions to avoid this, but emerging bonding techniques such as [4] or multilayers substrates [5] are available to solve this problem. Furthermore, more complex description of these tracks may allow overcoming this cross-over in future versions of this work.

### III. OPTIMIZATION MODELS

#### A. Thermal Model

The basic model starts from a matrix representation of the thermal behaviour [6]:

$$\begin{bmatrix} \Delta T_1 \\ \vdots \\ \Delta T_n \end{bmatrix} = \begin{bmatrix} R_{th11} & \dots & R_{th1n} \\ \vdots & \ddots & \vdots \\ R_{thn1} & \dots & R_{thnn} \end{bmatrix} * \begin{bmatrix} Q_1 \\ \vdots \\ Q_n \end{bmatrix} \quad (1)$$

The matrix elements are obtained from thermal simulation results using a numerical software on a given technology [7-8]. An example of simulation result is given in Fig. 4. Using these results, thermal resistances  $R_{thii}$  can be determined for each chip size and solder technique. This allows taking into account some edge effects, since the resistance of an element increases when it approaches the substrate edge, due to reduced thermal spreading. However, in the treated example, the chip location on the substrate is kept far enough from the edge, thus this phenomenon can be neglected: all  $R_{thii}$  are thus independent from chip location.

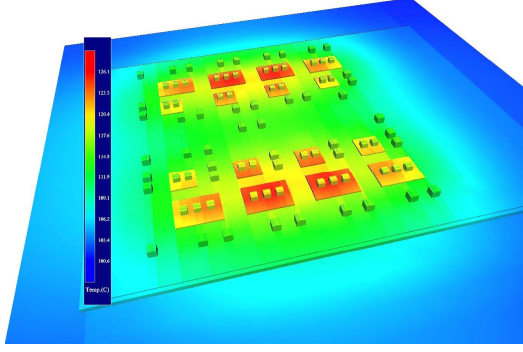


Fig.4. Example of thermal simulation [7] to obtain a set of thermal resistance matrix for each studied technology.

For coupling thermal resistance  $R_{thij}$ , a basic example using two chips has been studied in the numerical software, and interpolation is used to determine  $R_{thij}$  as a function of the distance between the chips. Table 1 gives an example for two 6mm\*6mm dies soldered on an Aluminium Nitride Substrate (180W/mK thermal conductivity), using a 25W/mK solder. Cooling conditions were defined by an exchange factor  $h = 12000 \text{ W/m}^2$ .

TABLE 1: EXAMPLE OF THERMAL SIMULATIONS TO DETERMINE COUPLING THERMAL COEFFICIENTS  $R_{thij}$

| Distance [mm] | $R_{thij} [^{\circ}\text{C/W}]$ |
|---------------|---------------------------------|
| 0             | 0.07                            |
| 1             | 0.06                            |
| 2             | 0.05                            |
| 4             | 0.0414                          |
| 6             | 0.0304                          |
| 8             | 0.0268                          |
| 15            | 0.0164                          |

These kinds of results have been summarized using a simple mathematical function which can be inserted into any optimization method:

$$R_{thij}(d) = -0.2 * \arctan(0.05*d + 0.2) + 0.1 \quad (2)$$

The choice of the arctan function is important, since it provides a good behaviour for high values of  $d$ , and prevents (2) from giving non physical values for  $R_{thij}$  (e.g. negative values), what may guide the algorithm to completely wrong solutions.

To account for several ceramic thicknesses, what is a key point in both EMC and thermal performances, several numerical simulations have been carried out for several thicknesses, between 0.3mm and 3mm. This allows choosing an optimized ceramic thickness in addition to the optimal layout and chip position. Mathematically, this corresponds to several interpolation functions identical to (2), but with various coefficients depending on the substrate thickness.

Another important issue is to account for the temperature dependant losses in the chips, expressed as  $Q_1, \dots, Q_n$  in (1). Several solutions may be employed for this, using for

example a bank of precise simulations results. We chose a simpler way by using the manufacturer datasheets, providing the switching energies and voltage drop as a function of chip temperature (Fig.5.). This is obviously not so precise, since the switching energy also depends on stray inductance and gate drive characteristics. However, for a pre-design step, the accuracy is sufficient. Solving the thermal problem (described by (1)) becomes thus a non linear problem, since  $Q_i$  depends on temperature. However, this is not a real mathematical difficulty and this has been taken into account in the optimization process.

### B. EMC Model

The EMC model of the inverter uses equivalent disturbance sources [9] and a propagation path. This one is mainly composed of common mode stray capacitances between the power module and the ground. These latter depend on the power layout. Fig.6 shows the complete equivalent model, including the inverter disturbance sources, some inductive stray elements, and the Line Impedance Stabilization Network (LISN) [10]

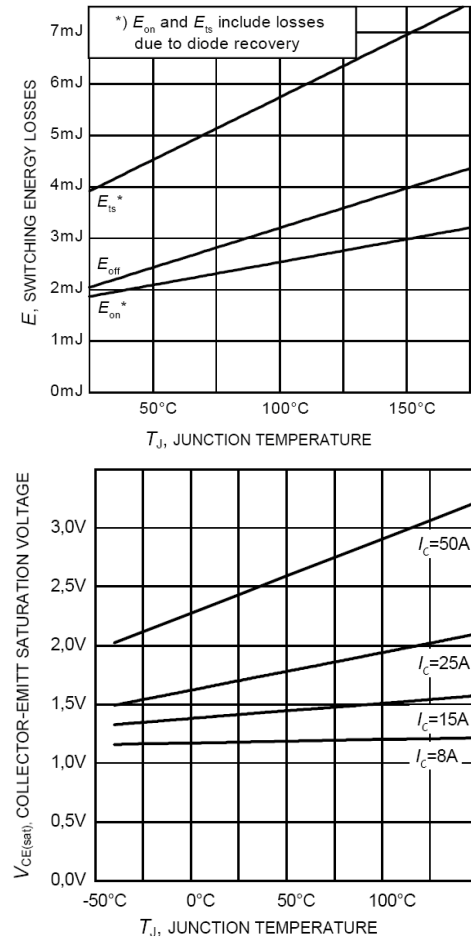


Fig.5. Accounting for electro-thermal coupling using datasheet [11] commutation losses and voltage drop as a function of chip temperature.

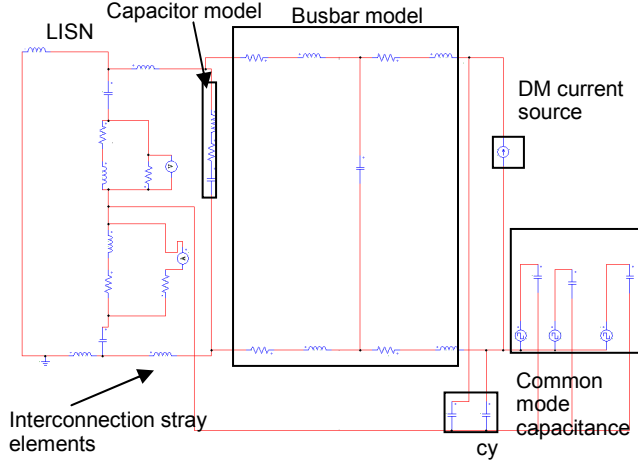


Fig. 6. EMC equivalent model.

The stray inductance and capacitance of the busbar are fixed, since we only focus on the power module layout, which has to be inserted in a representative environment. Concerning the stray inductance associated with the chip layout, a preliminary study has been achieved, in order to determine if the geometrical disposition of the dies really impacts on their values. Fig.7 shows that the impact of the distance between two chips is not very important for usual distance. Even if this may be included in the optimization procedure, this has not been taken into account at this step, since it does not really impact on EMI prediction accuracy, because the variation (between 3 mm and 10 mm for instance) is small and the values are negligible in front of the other stray elements outside the module (power leadframe, busbar, ...). Therefore, the layout is considered to act on the capacitive aspects only. Stray capacitors are computed based on the track shape, using analytical formulae [12], validated in comparison with the used technology. Also dielectric thickness and characteristics are therefore taken into account.

Since this model is computed directly in the frequency domain, it can be evaluated very quickly and seems therefore suitable to be implemented in an optimization process. The power layout impacts on the propagation path, which itself modify the EMI measured on the LISN.

An additional simplification is that the disturbance sources (current and voltage sources) are independent from chip disposition.

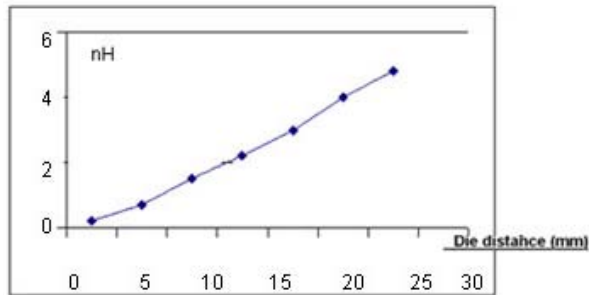


Fig. 7. Impact of the distance between chips on stray inductance.

This EMC model of the converter has been validated in the past [9], and even if it is not the most accurate, it is sufficient to guide the layout on an EMC point of view.

#### IV. LAYOUT AND CHIP LOCATION OPTIMIZATION

##### A. Thermal criterion only

Starting from the initial layout and chip disposal defined in Fig.3., the optimization has first been run on a thermal criterion only. The objective function has been defined as the square root of the sum of the square of all  $\Delta T$ . For the initial position, the objective function value has been evaluated as 219°C.

A first optimization on the chip location only, without any constraint on the tracks, has lead to the solution of Fig. 8, with an objective function of 22°C, what is far more uniform. The substrate thickness has been kept constant at 0.6 mm for this optimization.. It can be observed that the diodes have been located at the centre of the substrate, with the IGBTs around. The explanation is that, even if the diode thermal resistance is higher, the diode losses are lower than the IGBTs ones, and therefore, the temperature is lower. Thus, surrounding the diodes by the IGBTs increases their temperature, what leads to a more homogeneous temperature field in the module.

However, this chip disposition is not acceptable, regarding the interconnection constraints and especially the links between top and bottom substrates, described in Fig. 3. Therefore, another optimization has been achieved, still accounting for thermal behaviour only, but taking into account the necessary tracks and the associated shapes. Geometrical constraints have been added (a total of 286 constraints), in order to guarantee all electrical links between the dies. The new result is presented Fig.9. The objective function has been a little degraded at 45.2°C, but this is still better than the initial one. The maximum difference between the chip temperatures is 3°C in this configuration, compared to 2°C in the disposition of Fig. 8.

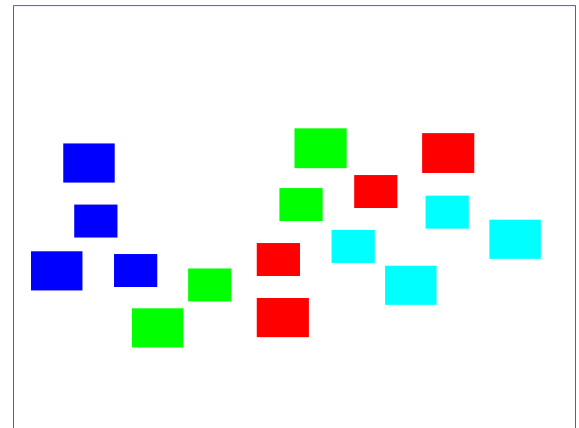


Fig. 8. Optimization result on a thermal criterion only, without any constraints on chips interconnections.

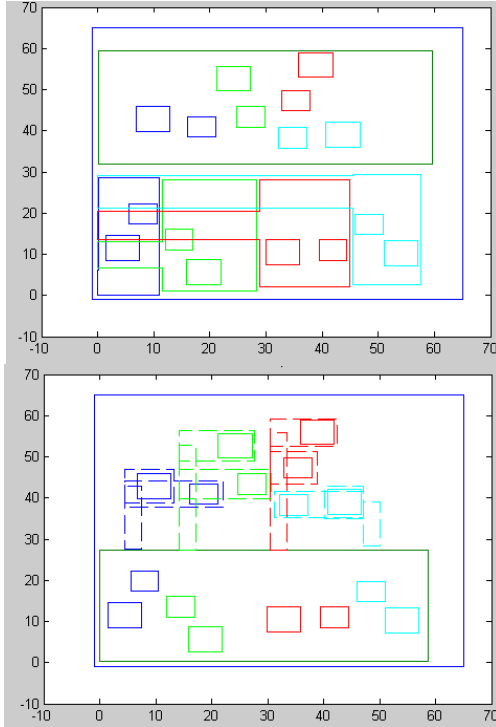


Fig. 9. Optimization result on a thermal criterion & chips interconnections constraints. Top: bottom substrate – Bottom: top substrate.

#### B. EMC criterion only

On the other hand, if we don't account for thermal aspect but on EMC level only, represented by the voltage across LISN, another solution can be found. With a variable substrate thickness, the algorithm does not really act on the track geometry, since the most important parameter on the capacitive behaviour is the dielectric thickness. It reaches the highest possible value in the optimization process, 3mm. The EMC criterion is not easy to be defined. After a sensibility study, 10 MHz frequency has been found to be not sensitive to any resonance effects, and chosen as reference frequency for giving an indication of the global EMC level. For the initial layout, the value was 70.25 dB $\mu$ V, and after optimization with a 0.6 mm substrate thickness, it reaches 61 dB $\mu$ V with the geometry described in Fig.10. The usual conclusion can be derived from this geometry: the floating points (phase output potentials) have reduced surfaces, whereas the DC bus tracks, which act as Cy integrated filters, exhibit increased areas [13]. All these effects are obviously limited by the geometrical constraints. Last, it should be noted that with a 3 mm thickness (maximum value), the EMC level is reduced at 28 dB $\mu$ V, what shows the big impact of this parameter.

However, this new chip disposition leads to a thermal criterion worst than the one from Fig. 9: 148°C, in comparison with 45,2°C. It is thus clear that improving the EMC behaviour reduces the uniformity of the thermal field. Combined criteria are thus needed to investigate possible trade off.

#### C. Combined Thermal-EMC constraints

The usual way of addressing trade-off studies is to draw the pareto front of the optimization problem [14]. The pareto front represents a set of optimized points in the space defined by all optimization criteria. In our studied case, we computed all points in the "Thermal-EMC" plane. The result, depicted in Fig. 10, may help the designer to choose between the best thermal performance or the best EMC behaviour. Two different points of this pareto front are illustrated in this Fig. 10. The point A is good on an EMC point of view, whereas the point B corresponds to the best thermal-EMC compromise. The comparison is not obvious at all, since many parameters act together: the substrate thickness modifies both EMC and thermal behaviour. The chip location is governed by the thermal criterion, and is limited through the tracks shapes, which are constrained by both geometrical and EMC aspects. The interesting trend is that both optimal layouts propose a chip disposition with the diodes located in the middle of the IGBTs to provide a more homogeneous temperature, as seen in the pure thermal optimization. On this basis, the degradation of one criterion or the other is linked to the substrate thickness and the track geometry, which acts on the capacitive behaviour.

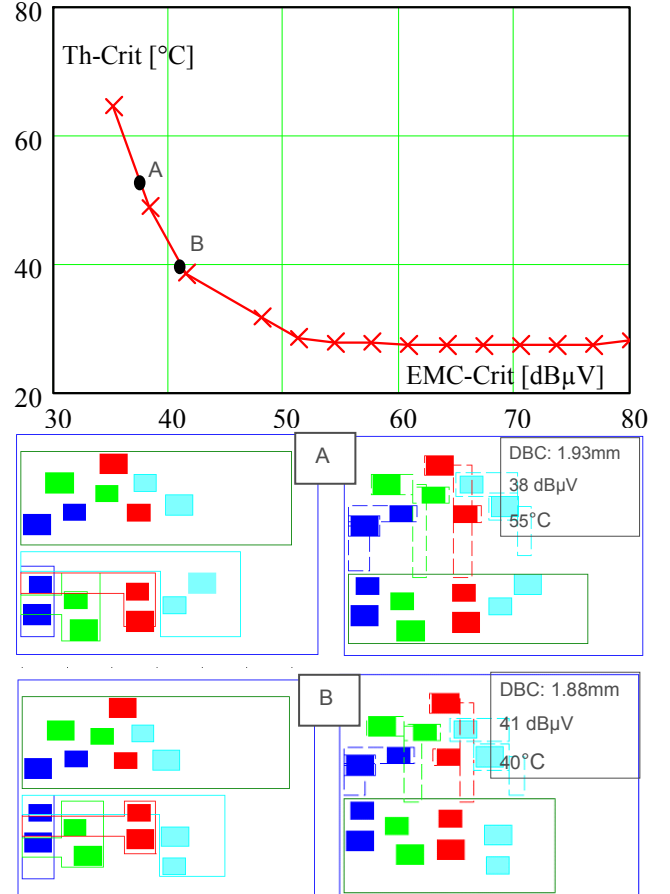


Fig.10. Pareto front representing the possible compromises between thermal and EMC performances. Illustration of two specific results for best EMC (A), or best compromise (B) results (DBC is the substrate thickness)

An easier interpretation is to check the results of the algorithm when looking for a very bad behaviour. This one is obviously far from the optimal points of the pareto front, illustrated in Fig.10 ! The substrate thickness is reduced to its minimal value (0.3 mm), what increases the stray capacitance and thus the EMC generation; the area of the floating points is very large also. In addition, the chips have been disposed far from each other, what increase the temperature difference.

Obviously, this optimization with all degrees of freedom allowed is on a practical point of view not realistic: for instance, all substrate thicknesses are not available commercially. However, it is interesting to let this parameter free, in order to investigate all the potentialities of a given technology. Furthermore, as stated before, the geometrical description used for the substrate tracks is limited, since overlap is allowed, what is obviously not desirable with conventional technologies. Some improvement must be made on this aspect, since even with this rough description the number of equations to code in the software is already huge (286 constraints). In addition, the way of describing the tracks is limited to this geometry and is not generic, if other inverter topologies are studied.

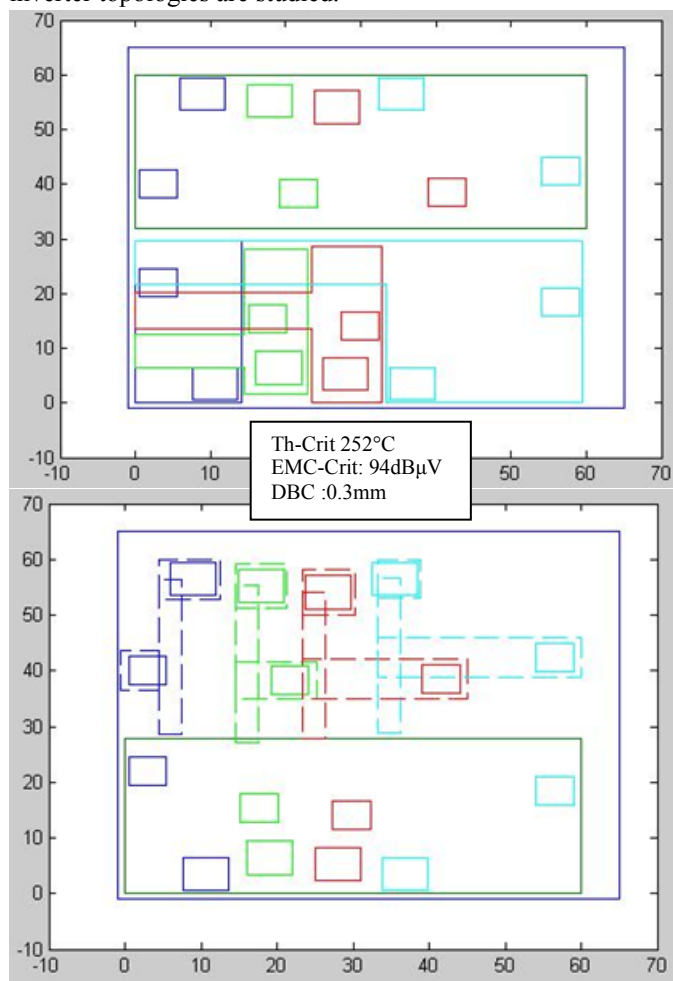


Fig.11. Optimization result when looking for the worst solution regarding both EMC and Thermal criteria (DBC is the substrate thickness).

Nevertheless, the work presented in this paper has shown that optimization techniques using simple models may allow proposing a new approach in the power layout, even if industrial limitations may also be considered. For instance, all substrates are not commercially available, or industrial fabrications may limit the proposed layouts. At least, using this method may allow determining a theoretical optimum of a given technology, and comparing any industrial realization with it.

## V. CONCLUSION

This paper has shown that chip location and power layout of an integrated power module can be optimized using simple models. These models have been validated in the past in comparison with measurement; Even if they do not provides the best precision, they give the good trend, what is sufficient for optimization. Thermal and EMC aspects have been taken into account simultaneously, what is mandatory since they are linked through the design of the power layout and the chip location. The proposed technique has been illustrated with the example of a 2kW four legs inverter, realised in double sided technology. Even if the proposed method exhibits some limitations for the moment, it is a new approach which should be considered in future power electronics designs.

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