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High temperature operating converter

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Abstract: Two sample SiC JFET are characterized and used to build a high operating temperature converter. Power losses are evaluated, the effect of temperature on ON-State resistance and saturation current is measured and discussed. Temperature effects on dynamic behaviour is not a major issue. Total losses vary with temperature. A 600V/300V converter is build and tested. JFET and inductor are cooled at 300°C.

1. Introduction.

High temperature power electronics has become a possibility by the development of Silicon Carbide (SiC) components. Breakdown voltage remains high at high temperatures, over 250°C, where silicon devices reach an absolute limit. The perspective of high operating temperature power components permits to imagine heatsink-free systems or converters embedded in the vicinity of internal combustion engines. Extreme environments are a new area for power electronics based on SiC. This is why we are studying converters with a cold cooling source at temperatures in the 300°C range. JFET components are becoming available outside laboratories, the devices used in this work comes from SiCED. A SiC-JFET/Si-MOSFET cascode assembly provided in a plastic flat package, rated 1200V-2A. Cascode is used to get rid of the normally-ON behaviour of JFETs or to use SiC-JFET as an 'almost pin to pin' replacement of MOSFETs or IGBTs. Nevertheless, in this work cascode operation is not used, the MOSFET is disabled (G and S terminals are connected together) and the JFET is driven using a slightly modified standard integrated MOSFET- IGBT driver. High junction temperature converter brings to the foreground leakage current limitations of diodes however the reverse characteristics of JFETs make possible diode-less converter. Free wheeling take place in the bulk structure of the JFET used. Another issue of high temperature is passive components. Capacitors are almost inexistent at 300°C while magnetic cores can be purchased on the web. Conductor designed for high temperature are also common. The converter presented in this paper is a 600V/350V buck converter with both inductor and switching cell cooled at 300°C.

2. Static characterization

SiC JFET power components are characterized to study temperature effects on majors parameters and to define the thermo-electrical limits. This knowledge is the basis for the design of the inverter. Temperature is set by a hot air furnace and verified by thermo-couples placed on the metal case of the devices, ranging from 30°C to 300°C.

To start with, the JFET are characterized as power switches this is why the Drain to Source voltage is limited from -2V to 2V in the ON -State, see Fig.1.

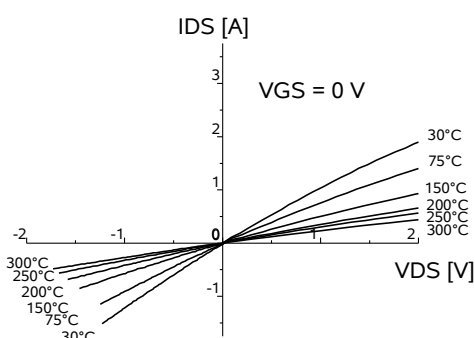


Fig. 1 Static measurement in the ON-state

It can be seen that the ON-resistance varies with temperature from 1Ω at 30°C to 4Ω at 300°C. Saturation current is measured and drops by a factor of 4 as temperatures rises to 300°C. It should be noted here that the devices used in this paper are first generation JFET from SiCED and that newly released versions have a reduced temperature dependency.

For testing reverse conduction properties of the JFET the same voltage range is used for comparison purposes. In the OFF-state the JFET exhibits a reverse conducting characteristic as a diode that is used for free wheeling, see Fig 2.

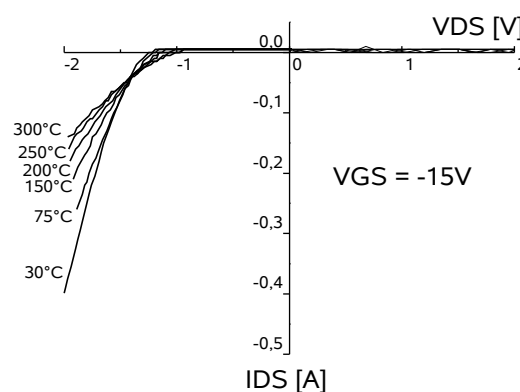


Fig. 2 Static measurement in the OFF state VGS=-15

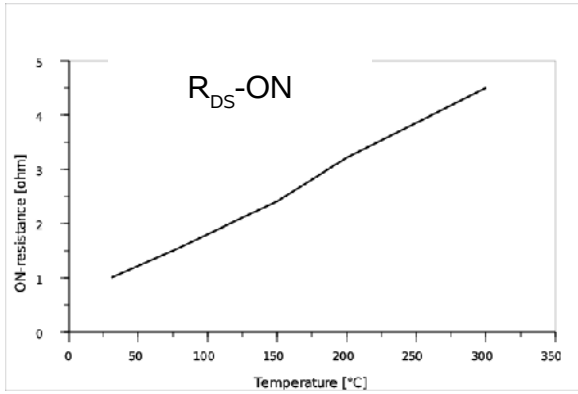


Fig. 3: JFET ON-resistance as a function of temperature measured at constant $V_{DS}=2V$.

On Fig. 4 ON resistance is plotted against temperature, a strong dependency with temperature can be observed. Power losses increases greatly as temperature rises because of the positive temperature coefficient. It should be noted again that the devices used in this paper are first generation JFET from SiCED and that the latest released samples now exhibit 50mΩ ON-resistance for 1200V-50A devices.

Conduction losses

JFET are unipolar devices hence a resistive conduction behaviour. R_{DS-ON} is measured at different temperatures in the 30°C to 300°C range using Drain-Source voltage and current, see Fig. 4. Conduction losses can be calculated from the value of the ON resistance of the JFET when Drain current is known and this is the case: a buck converter at fixed input voltage, load and duty cycle.

3. Switching losses measurement

In an inverter leg, dead-time, t_m , and gate resistor, R_g , can have a dramatic effect on losses, E_{on} and E_{off} , [1] An experimental test setup is used to electrically measure switching losses at turn-ON and turn-OFF, see Fig. 5. with dead-time, t_m , gate resistor, R_g and temperature, T , as parameters.

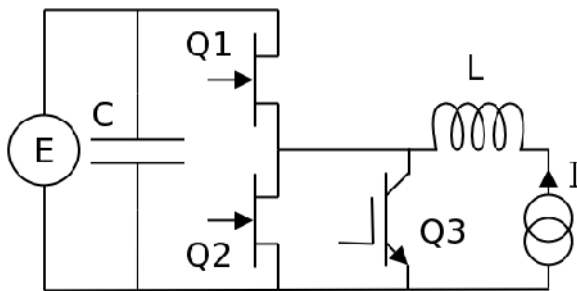


Fig. 4: Experimental setup for the measurement of switching power losses in a pulsed mode.

The inverter leg is built using sample SiC JFET connected to a ceramic capacitor on a double sided printed circuit board with a grounded back plane to reduce inductive parasitic effects. Q3 of Fig. 4 is used to connect a constant current source to the inverter leg during a switching sequence, thus allowing pulsed mode operation. Pulsed mode operation is chosen to limit self heating of the JFET under test, therefore case temperature can be assumed to be equal to internal junction temperature. Case temperature is set by placing the devices in a hot air furnace. When electrical measurements are stable in time it is assumed that thermal equilibrium is reached. Drain current is sensed using a coaxial wide band-pass shunt – 1GHz – and voltage is measured with two paired probes placed in a differential arrangement, bandwidth is approximately 400 MHz. Probes are compensated and deskewed.

We have published [2], this year at EPE, such work and results. The converted described here uses the same switching cell, so previous optimization work can be used. The optimal values of resistance and dead-times are used in this paper. Fig.5 summarizes it and presents the switching losses as a function of temperature.

T (°C)	E_{on} (uJ)	E_{off} (uJ)
35	24	7
75	22	6
150	19	5
200	20	5
300	20	5
	$R_g = 47\Omega/3$	$R_g = 47\Omega$
	$t_m = -30ns$	$t_m = 150ns$

Fig. 5. Switching losses versus temperature. Optimal values of R_g et t_m for reduction of losses Supply voltage = 350VDC Switched current = 1A

4. Total power losses evaluation

A simple evaluation is made from static and dynamic data in order to set the maximum possible frequency range of the JFET switching cell built using the tested devices. Static measurements are used for conduction modelling. Dynamic measurements produced switching losses as functions of dead time and gate resistor. Switching losses, not much affected by temperature, are multiplied by frequency and added-up. While conduction losses are computed using the value of the current, conduction time and ON-resistance varying with temperature Fig. 6 shows that 100kHz to 300kHz operation is possible.

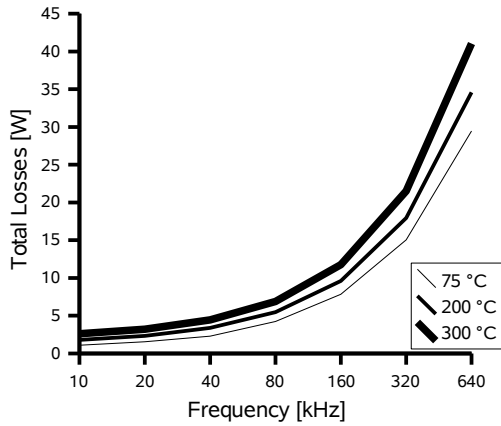


Fig. 6: Estimated total power losses of one JFET

5. Experimental converter

This time the converter is a buck converter aimed at accumulators powered power DC-bus for traction. The accumulators bank voltage is 600V, the DC-bus is 300V. A reversible converter is build around one inverter leg built with two JFET. For economical reasons and availability, very high temperature capacitors and interconnect is not used. Only the JFET and the inductor are cooled at 300°C using a hot air furnace. The rest of the circuit is at room temperature. The schematic is presented at Fig.6, dashed rectangle indicates components cooled at 300°C.

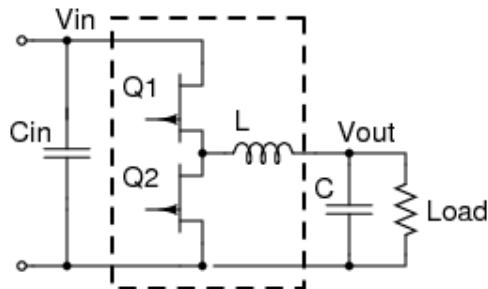


Fig. 7: Reversible buck converter

A close-up picture of the converter is at Fig. 8. Top from left to right: Inductor L (the white wound component), Q1 and Q2 SiC JFETs from SiCED sitting just outside the hot air furnace outlet. Printed circuit (Insulated Metal Substrate) is visible on the bottom side of the picture, holding the ceramic tank capacitor Cin. Load and load capacitor C are not visible. Gate drivers are separate circuits connected to the power board by twisted pairs. Dead times, different at turn-ON and turn-OFF, are generated by a programmable gate array circuit. Optical fibres transmit switching signals to the drivers.

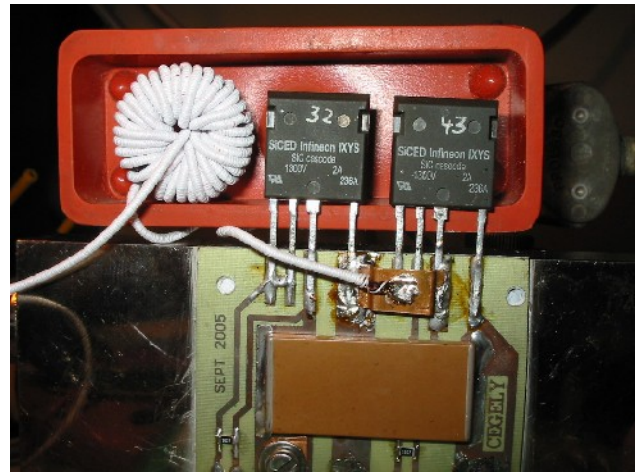


Fig. 8: A torus inductor and two JFET just outside the hot air outlet. Tank capacitor lies below, on the SMI substrate. A cold plate is used to maintain solder joints and capacitor at reasonable temperatures.

6. Testing the converter

The converter is tested at a cooling temperature of 300°C with an input voltage of 600V (breakdown voltage/2). Switching frequency is 300KHz and duty cycle 0.5. The load draws an average 0.4A.

Fig. 9 is an oscilloscope screen showing the converter's operation. Gate signal is a 0/-20V square wave at 300KHz. Inductor peak current is 0.5A, a value quite close to the saturation current of the JFET at 300°C. Current ripple is 0.2A. JFET Drain-Source voltage is a 600V square wave with 150ns rise/fall time. Variation of Drain-Source voltage during conduction is visible, it is due to the relative high value of Drain current in respect with saturation of the JFET.

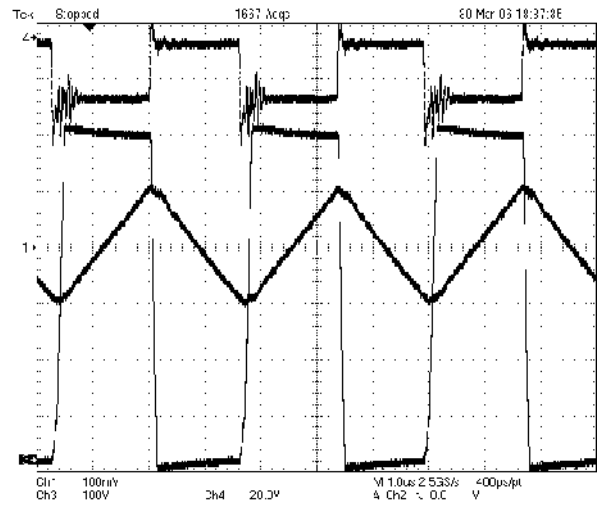


Fig. 9: Overview of the converter's operation

Top trace: gate voltage, centre trace: inductor current, bottom trace: Drain-Source voltage of JFET, Q2

The inductor is made of a special high temperature magnetic core from *Magnetics* [12], wound with a 1mm diameter copper wire insulated by two crossed layers of Teflon thread. Long term stability is not tested.

7. Conclusion

High temperature operation of a SiC JFET switching cell with inductor at 300°C is demonstrated. Operating frequency is 300kHz, input voltage is 600V, current is 0.5A limited by device size and technology version. The internal diode of JFET is used as a free wheeling diode. The effect of temperature is mainly an increase of conduction losses as ON-resistance is very temperature dependent (a 4.5 ratio on the 30-to-300°C range) Switching losses are slightly reduced by temperature increase due to the reduction of peak current during diode recovery (an average 0.75 ratio on the 30-to-300°C range). High temperature inductor is build using commercially available core and materials. The tank capacitor and solder interconnections still have to be operated at room temperatures.

Acknowledgements

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References

- [1] Björn °Allebrand and Hans-Peter Nee, "On the choice of blanking times at turn-on and turn-off for the diode-less SiC-JFET inverter bridge", in Proceedings of the 9th Conference on Power Electronics and Applications, EPE '2001, Graz, Austria, 2001
- [2] Dominique BERGOGNE et al. : "300°C operating junction temperature inverter leg investigations" in Proceedings of the 11th Conference on Power Electronics and Applications, EPE '2005. Dresden, 2005
- [3] Ahmed Elasser John Park A. William Clock Dick Herbs Eric Jacobson GE Corporate R&D, Niskayuna, "Silicon Carbide Devices and Applications : Gate Turn-Off Devices Hybrid Si/SiC Inverter Power Systems Applications", NY DARPA/EPRI Megawatt Review October 17-18, 2000 Alexandria, VA
- [4] Björn °Allebrand and Hans-Peter Nee, "On the possibility to use SiC JFETs in Power Electronic circuits", in Proceedings of the 9th Conference on Power Electronics and Applications, EPE '2001, Graz, Austria, 2001
- [5] Björn °Allebrand and Hans-Peter Nee "Minimizing

oscillations in the Diode-Less SiC JFET Inverter Bridge" in Proceedings of the Nordic Workshop on Power and Industrial Electronics (NORPie), Stockholm, Sweden, August 2002

- [6] Johnson, R.W. Evans, J.L. Jacobsen, P. Thompson, J.R. Christopher, M. "The changing automotive environment : high-temperature electronics", IEEE Transactions on Electronics Packaging Manufacturing, July 2004, Volume: 27, Issue: 3 page(s): 164- 176
- [7] Madhu Sudhan Chinthavali, Burak Ozpineci, Leon M. Tolbert, "High Temperature and High-Frequency Performance Evaluation of 4H-SiC Unipolar Power Devices", Proceeding of the APEC conference. 2005
- [8] Jared HORNBERGER, Alexander LOSTETTER "High-Temperature Integration of Silicon Carbide (SiC) and Silicon-on-Insulator (SOI) Electronics in Multichip Power Modules (MCPMs)", in Proceedings of the 11th Conference on Power Electronics and Applications, EPE '2005, Dresden, 2005
- [9] D. Domes , W. Hofmann¹, J. Lutz, "A First Loss Evaluation using a vertical SiC-JFET and a Conventional Si-IGBT in the Bidirectional Matrix Converter Switch Topology", in Proceedings of the 11th Conference on Power Electronics and Applications, EPE '2005. Dresden, 2005
- [10] Bjorn Allebrand and Hans-Peter Nee "Comparison of commutation transients of inverters with silicon carbide JFETs with and without body diodes", in Proceedings of the NORPIE conference. 2004
- [11] Dethard Peters, Heinz Mitlehner, Rudolf Elpelt, Reinhold Schörner, Dietrich Stephani "The Industrial Utilization of SiC Power Devices Aspects and Prospects", EPE2003, European Conference on Power Electronics and Applications, 2-4 Sep 2003 - Toulouse
- [12] *Magnetics, inc.* 111 Zeta Drive Pittsburgh, PA 15238-0422. www.mag-inc.com/

