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Towards an integrated inverter based on lateral JFET SiC

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Abstract

The feasibility of a hybrid inverter based on commercial silicon carbide vertical JFETs was tested. The Ron-resistance, mainly due to the vertical channel, increases with the temperature, from 1.1 Ω measured at RT to 2.98 Ω at 300°C. These devices can drive current in both forward and reverse direction, eliminating the need for an external anti-parallel diode. A transient current-limited short circuit is observed with duration of 100 ns in turn-on. The power losses estimated involve for the hybrid inverter a working frequency up to 300 kHz. Good results obtained for hybrid inverter predict a SiC monolithic inverter realization. For this propose, SiC lateral JFETs (LJFETs) were studied and designed by finite-element method. A double RESURF structure is retained for the SiC LJFET, in order to reduce the on-resistance and to improve the blocking voltage. The obtained Ron-resistances are one order of magnitude lower than in vertical SiC JFETs. This result is obtained thanks to the high doping lateral channel and RESURF structure. Switching times of the LJFETs during turn-off and turn-on, are obtained in the 20 to 30 ns range. Eight levels of masks are designed to fabricate these devices. The masks structures were optimized in order to minimize both the Ron-resistance and the device size by utilizing inter-fingers structures.

1 INTRODUCTION

The development of power electronics applications involves the realization of specific devices which must work in harsh environment (high temperature >200°C, high voltage, 600 V for domestic applications).

Hybrid approaches suffer from interconnection reliability. Monolithical integration seems to be a more effective method to assemble power devices and passive components.

Due to their physical properties, semiconductors with large bandgap are very interesting in this case compared to the classical silicon, the material usually utilized in power device fabrication. Among the spectra of large bandgap semiconductors, silicon carbide (SiC) is the semiconductor material presenting the most advanced device technology [1-2].

SiC is known to exist in many different crystallographic structures (polytypes). To develop high temperature and/or high voltage devices, 4H-SiC and 6H-SiC are most frequently utilized. In the case of these polytypes, the breakdown critical electric field is an order of magnitude higher compared to silicon and the thermal conductivity is three times higher.

Thus the use of 4H or 6H-SiC allows to reduce the size (by a factor of 10 to 100), the number of devices and to increase their operating temperature.

Diminishing the size of elemental devices is an additional factor that commonly with the monolithic integration allows a significantly decrease of the switching power losses during the inverter operation. Inverters are currently based on silicon IGBTs for medium and large power applications. Because it can not conduct current in reverse direction, an anti-parallel power diode is needed. The most favorable SiC switch (technologically available) is the JFET [3,4].

Compared to the IGBT, this is a normally-on switch and presents a reversible behavior with a conducting current in forward and reverse bias. Thus, for the inverters based on SiC JFET, the anti-parallel power diodes are no more necessary. Furthermore, to turn the SiC JFET off, a negative gate voltage is required at values that may be superior than in IGBT based inverters with probably superior gate capacitances also.

Firstly this paper presents an experimental validation of a high temperature operating inverter based on commercial discrete Vertical-JFET (VJFET) in SiC. The experimental results enable to consider the design of an integrated inverter in SiC. This integrated system based on the design of SiC lateral JFETs (LJFET) with a breakdown voltage of 900V is presented in the second part of this paper.

2 FEASIBILITY

The feasibility of an inverter based on silicon carbide JFETs was tested. Figure 1 presents the forward on-state and blocking characteristics of commercial SiC VJFET purchased from SiCED [5]. The current - voltage measurements were performed in air from room temperature (RT) to 300°C with a Keithley 2410 Source Measurement Unit and Tektronix 370, by a four point method in order to eliminate the resistances from the wire connections. The on-resistance, mainly due to the vertical channel, increases with the temperature, from 1.1 Ω measured at RT to 2.98 Ω at 300°C. Usual mobility majority carrier behavior is involved.

In a vertical configuration the on-resistance of JFETs are limited by the length of the channel which corresponds to the thickness of the low-doped SiC epitaxial layer. Its thickness value (a tenth micron) is directly related to the JFET blocking voltage in off-state (e.g.: a SiC tenth micron with $5 \times 10^{15} \text{ cm}^{-3}$ doping corresponds to 1500V blocking voltage).

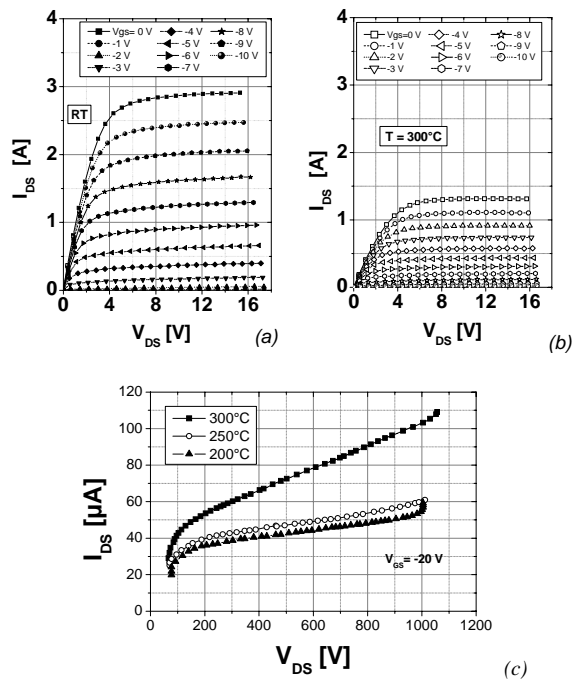


Fig. 1 I_{DS} - V_{DS} of SiC commercial VJFET in the forward on and off-state: on-state at RT (a), on-state at 300°C (b) and off-state from 200°C to 300°C (c)

In the off-state (V_{GS} at -20 V), the I-V measurements of SiC VJFETs (Figure 1c) show a blocking voltage limited to about 1 kV with a leakage current increasing with temperature.

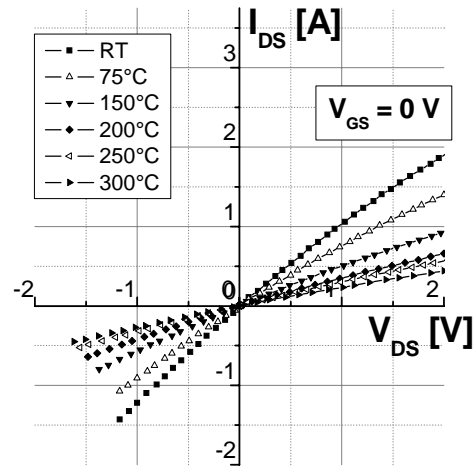


Fig. 2 Reversible behavior of the SiC VJFET in forward and reverse bias for ambient temperatures varying from RT to 300°C..

These experimental investigations show also that these devices can conduct current in both forward and reverse direction (Figure 2), eliminating the need for an external anti-parallel diode.

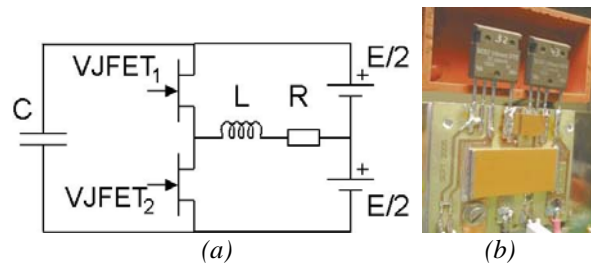


Fig. 3 Schematic (a) and picture (b) of the hybrid inverter with two SiC commercial VJFET

Two SiC VJFETs were put together to realize a hybrid inverter, from which a schematic and picture are presented in Figure 3. Due to the reversible behavior of the SiC JFETs, anti-parallel diodes were not employed. These devices are maintained in a hot air furnace with a controlled temperature which was varied from RT to 300°C. JFETs are placed vertically at the cost of increase the wiring inductance but this allows a thermal shield to be placed in front of the printed circuit board. High temperature solder is used to connect the devices. Inverter solder side is cooled by RT forced convection air. SiC VJFETs are driven by ordinary 0-15V IGBT drivers.

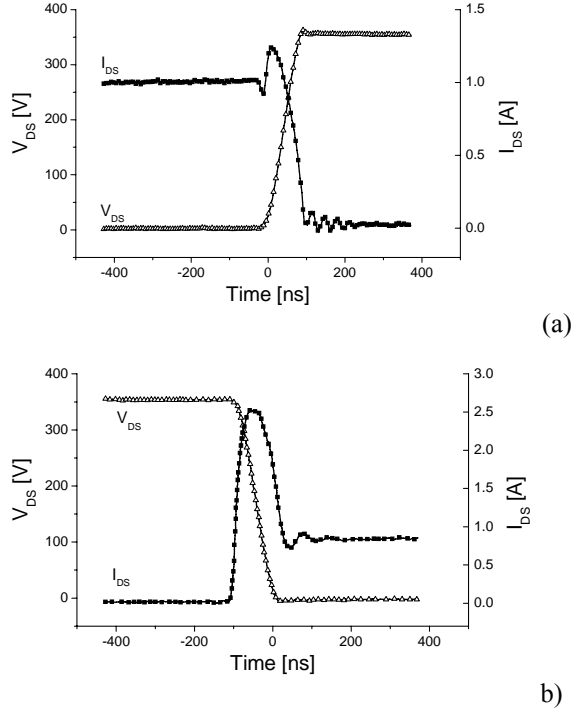


Fig. 4 Drain-source voltage and current for VJFETs on turn-off (a) and turn-on (b) switching sequence performed at RT

Figure 4 presents drain-source voltage and current for VJFETs at turn-off and turn-on switching sequence performed at RT. A transient current-limited short circuit is observed with duration of 100 ns in turn-on. Waveform qualities are due to the used inductor in the current source and to a not so small gate resistor of 47Ω.

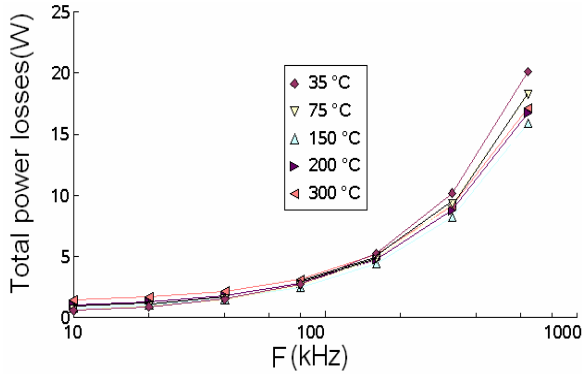


Fig. 5 Estimated total power losses per VJFET with junction temperature as a parameter

Losses from the inverter were estimated from electrical measurements for RT to 300°C operation. Total power losses as a function of frequency are presented in Figure 5. The performance of this circuit predicts the possibility to construct an integrated inverter with a working frequency up to 300 kHz.

3 INTEGRATED INVERTER DESIGN

3.1 Approach - design method

A monolithically integration of SiC JFETs allows to reduce considerably the switching time and to eliminate losses and parasitics related to the device inter-connections. Lateral devices are in need in this case because the silicon carbide technology is mainly developed only in the Si face. The substrate doping is still elevated to realize power devices by doping the substrate and the growth of epitaxial layers in the C face is also technologically difficult.

Reduced Surface Field (RESURF) technique is one of the most widely used method to realize the design of lateral high voltage devices in power integrated systems [6-7]. This method allows to integrate different power devices such as bipolar and MOSFET transistors with high voltage diode.

The RESURF technology consists to introduce layers in the devices structures that are defined by their geometric dimensions (thickness and length), the type of semiconductor and the doping concentration. By dimensioning these parameters, the presence of these layers will generate a more homogenous distribution of the electric field in the device structures and thus will increase breakdown voltage.

The RESURF method is applied here in order to reduce the on-resistance and to improve the blocking voltage of the SiC LJFETs.

Param eters	Values	Models
$\mu_{n,MAX}$	$947 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$	$\mu_{n,p}(x,y) = \mu_{n,p,MIN} + \frac{\mu_{n,p,MAX} \left(\frac{T}{300}\right)^{X_{Lnp}} - \mu_{n,p,MIN}}{1 + \left(\frac{T}{300}\right)^{X_{Lnp}} \left(\frac{N_{total}(x,y)}{N_{REFn,p}}\right)^{\xi_{n,p}}}$
$\mu_{n,MIN}$	$0 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$	
NU_n	-1,962	
XI_n	0	
ξ_n	0.61	$\mu_{n,p}(x,y) = \frac{\mu_{n,p0}}{\left[1 + \left(\frac{\mu_{n,p0} \cdot E_p(x,y)}{v_{satn,p}}\right)^{\beta_{n,p}}\right]^{\frac{1}{\beta_{n,p}}}}$
N_{REFn}	$1.94 \times 10^{17} \text{ cm}^{-3}$	
$\mu_{p,MAX}$	$124 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$	
$\mu_{p,MIN}$	$15.9 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$	
NU_p	-1.434	$N_D^+ = \frac{N_D}{1 + GCB \exp\left(\frac{E_{FN} - E_D}{kT}\right)}$
XI_p	0	
ξ_p	0.34	
N_{REFp}	$1.76 \cdot 10^{19} \text{ cm}^{-3}$	
μ_{n0}	$500 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$	$N_A^- = \frac{N_A}{1 + GVB \exp\left(\frac{E_A - E_{FP}}{K_T}\right)}$
μ_{p0}	$167 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$	
τ_{n0}	50 ns	
τ_{p0}	50 ns	
N_{SRHn}	10^{30} cm^{-3}	$\tau_{n,p}(x,y) = \frac{\tau_{n,p0}}{\left(1 + \frac{N(x,y)}{N_{SRHn,p}}\right)}$
N_{SRHp}	10^{30} cm^{-3}	
$n_{,IONIZA}$	$4.08 \cdot 10^5 \text{ cm}^{-1}$	$\alpha_{n,p}(x,y) = n_{,IONIZA} \cdot e^{\left(\frac{E_{cn,p}}{E_{para}(x,y)}\right)}$
$p_{,IONIZA}$	$1.63 \cdot 10^7 \text{ cm}^{-1}$	
E_{cn}	$1.67 \cdot 10^7 \text{ V}\cdot\text{cm}^{-1}$	
E_{cp}	$1.67 \cdot 10^7 \text{ V}\cdot\text{cm}^{-1}$	

Table 1. SiC parameters and analytical models utilized in finite-element MEDICI simulations: (a) mobility, (b) incomplete ionization, (c) carrier life time and (d) ionization coefficients.

SiC LJFETs, targeting inverter structure integration, were studied and designed by finite-element method simulation with MEDICI software tool. Semiconductor device behaviours are obtained by simulating of internal parameters in the device structure such as the distribution of potential, the density of carriers, the density of current, and the propagation of electric field. The device structure is composed of different areas (semiconductor, oxide, metal). A schematic SiC LJFET structure is illustrated in Figure 6.

In each area, different parameters are defined such as doping profiles. A grid with a great number of nodes is realized on all the device structure. The equations of the physic of semiconductor such as equation of continuity and Poisson's equation are solved for each node. SiC physical parameters and analytical models are utilised for the mobility, incomplete ionization, life time of carriers and coefficients of ionization (Table 1).

In the surface, for the different structure layers, realistic doping profiles were introduced. These profiles were obtained by Monte-Carlo ion implantation simulation or from SIMS preliminary analyses of implanted SiC samples.

Drain, source, gate and the channel were designed as to be ion implanted in a low doped epitaxial p-type layer with a uniform doping concentration.

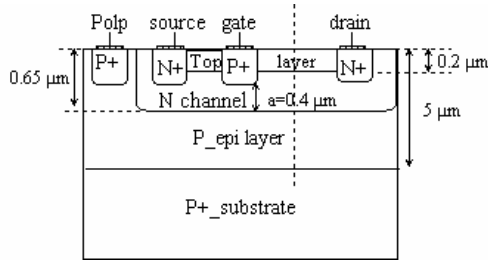


Fig. 6 Schematic presentation of the SiC LJFET with a double RESURF structure

A double RESURF structure is retained for the SiC LJFET. This is realized by the epitaxial layer forming a junction below the n-type channel (active layer) and by adding a top layer between the gate and the drain. The doping profile of the p-type top-layer is also controlled by ion implantation.

In blocking state, the vertical electric field distribution is defined principally by the thickness and the doping of the p-type epitaxial and the ratio with the active layer doping. The low value of the epitaxial layer doping by its depletion allows a vertical distribution of the electric field inside the structure. But the ratio between the channel doping and the epitaxial layer doping must be kept low enough in order to deplete the channel active layer by its junction with the epitaxial layer. The channel depletion by this vertical SCR (space charge region) must occur before the lateral depletion of the channel by the lateral diode formed between the drain and the gate.

The presence of the p-type top layer constitutes the second RESURF structure. In blocking state this layer must be depleted vertically in order to extend the SCR towards the top junction before the lateral depletion of the n-type active layer and the p-top layer itself.

Keeping a high breakdown voltage by improving electric field distribution, the RESURF technique provides also better lateral on-state conduction in JFETs. It allows to obtain a JFET with higher channel doping concentration, a small length and so a lower on-resistance.

3.2 Results and discussion

The lateral electric field distribution of the double RESURF JFET structure is shown in Fig. 7 for different doping concentration of the top layer. The doping concentration of the channel is fixed to $2.10^{17} \text{ cm}^{-3}$. A low doping concentration of the top layer compared to channel doping supports the lateral depletion, and involves a high concentration of the electric field close to the gate. The potential lines are distributed mainly close to the device surface. The breakdown of junction is established between the top layer and the channel.

The presence of top layer with a high doping concentration ($5.10^{17} \text{ cm}^{-3}$) will make difficult the depletion of this layer. The SCR extends mainly through the channel and the P-epi layer. The maximum value of electric field is obtained close to the drain where the potential lines are concentrated that involves the device to reach prematurely the breakdown voltage (V_{BR}).

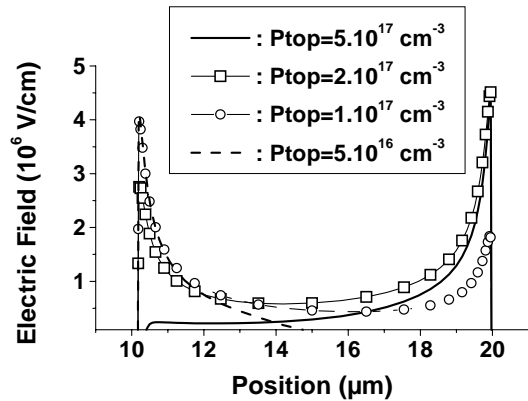


Fig. 7 : Distribution of the lateral electric field of the JFET RESURF structure

The lateral electric field distribution is optimised when the doping concentration of the top layer allows obtaining a trapezoidal electric field between the drain and the gate.

The optimum potential distribution for this structure is obtained for a doping concentration of the top layer included between $1.10^{17} \text{ cm}^{-3}$ to $2.10^{17} \text{ cm}^{-3}$. In this range, maximum values of the electric field are reached both at the drain and at the gate side of the structure, respectively. The SCR surface is wider,

developed in the epi-layer, which increases the breakdown voltage of the JFET.

The figure 8 shows the breakdown voltage as a function of doping concentration of top RESURF layer. The maximum value of breakdown voltage reach 1kV with doping concentration of top layer equal to the doping concentration of channel.

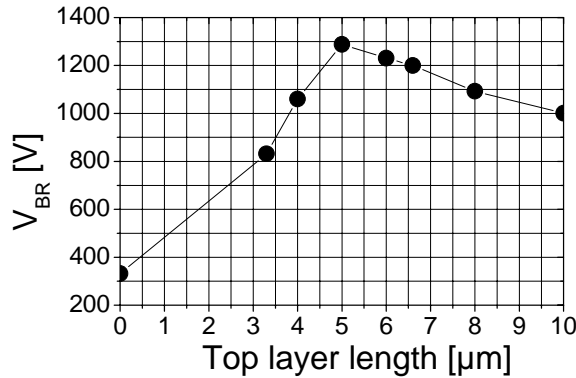


Fig. 12: Breakdown voltage as a function of the top RESURF layer doping concentration with the active layer $= 2.10^{17} \text{cm}^{-3}$

The doping concentration of the top layer is fixed to 2.10^{17}cm^{-3} . Fig.13 shows the doping profile for the cut line indicated in Fig 6.

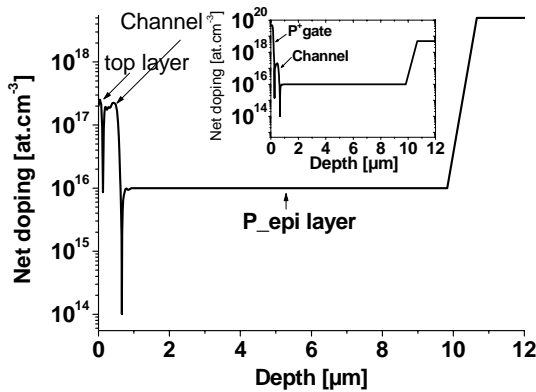


Fig. 13: Vertical doping profile in the lateral device.

The forward characteristics of SiC lateral JFETs are related to a technological limit (the minimum distance between two successive lateral layers). Figure 14 presents the spectra for a technological limit of $3 \mu\text{m}$. The device surface area is 1.5mm^2 .

The high conduction level is mainly due to the low value of the on-resistance thanks to the high channel doping.

Fig. 15 shows the evolution of Ron-resistance as a function of length of channel and the area of device. The length of channel is defined by the technological limit (L_T).

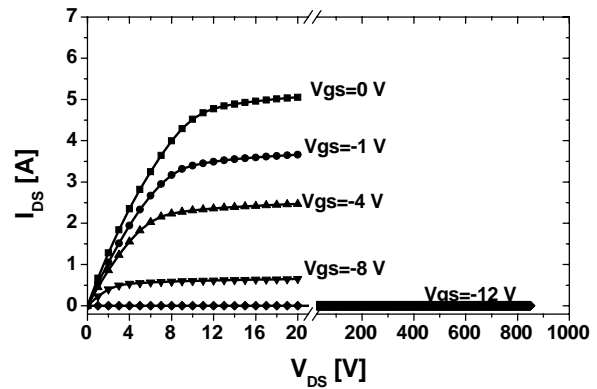


Fig. 14 : i-v characteristics of SiC lateral JFET

The Ron-resistance is estimated to 0.3Ω , by using an area device of 1.5mm^2 with technology limit of $3 \mu\text{m}$. The Ron-resistance can reach a value lower than 0.1Ω , by using an area of device of 2mm^2 with technology limit of $0.5 \mu\text{m}$. To obtain a value of 0.05Ω with a technological limit less advanced such as $1 \mu\text{m}$, the area of SiC LJFET must be larger than 5.5mm^2 .

These values are one order of magnitude lower than in vertical SiC JFETs. This result is obtained thanks to the high doping channel and the dissociation in the lateral JFET between the layers for the lateral conduction in on-state and the layers for the voltage sustain in off-state.

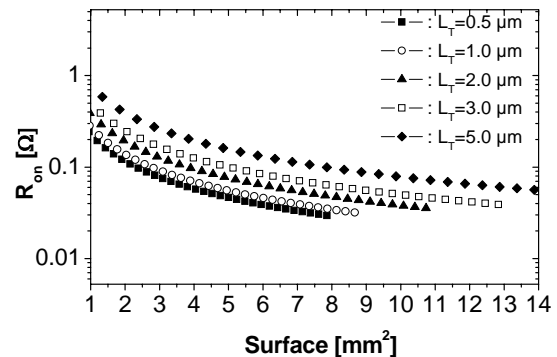


Fig. 15: R_{on} resistance as a function of the area of SiC lateral JFET.

For the moment, SiC devices size seems to be limited by the defects densities of the available wafers. Nevertheless a considerable effort was done these last years to decrease the micropipe and dislocation densities in SiC substrates.

The optimisation of this resistance is important in order to increase the courant in on-state and to decrease the voltage over the LJFET in off-state (limiting the power losses in switching mode).

The SiC LJFETs are principally designed in order to be utilised in power converters, like inverter modules. The static performances show that the SiC RESURF JFET can be used as a lateral switching device with a breakdown voltage over 600V. A simple structure

with a resistor and an inductive load (100nH) was realized for evaluating the switching performances of lateral JFETs. The dc-link voltage was 450 V and the load current was 2 A. A gate signal with amplitude of 450V was applied with a resistance of 220 Ω .

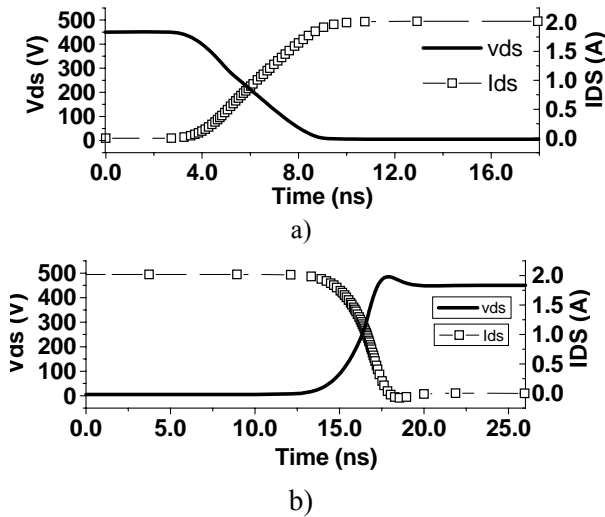


Fig. 16 Switching characteristic of the SiC lateral JFET with double RESURF structure, a) turn-off, b) turn-on

Figure 16 presents the switching characteristics of the LJFETs during turn-off and turn-on. Switching times in the 20 to 30 ns range are obtained.

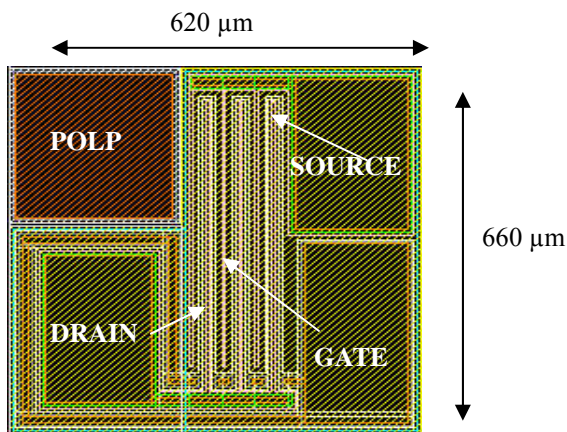


Fig. 17 Top view of the SiC lateral JFET mask layout with eight levels superposed.

Eight levels of masks are necessary to fabricate this device (Fig.17). The masks structures were optimized in order to minimize both the Ron-resistance and the device size by utilizing inter-fingers structures. Three different channel lengths, 3, 6 and 9 μm have been considered. The distance between the gate and the drain areas was fixed to 10 μm .

The device fabrication process is currently under completion. Planar structures are privileged utilizing ion implantation to form box profiles. The number of

epitaxial layers is reduced and the technology process excludes the use of plasma etching that generates significant surface defects.

4 Conclusion

The experimental results obtained from the realization of a hybrid inverter based on commercial SiC vertical JFETs enable to consider the design of a SiC monolithically integrated inverter. For this, SiC lateral JFETs structures were studied and designed by finite-element method. The Ron-resistances and switching times were improved by one order of magnitude versus vertical SiC JFETs. These results are obtained thanks to the optimized double RESURF structures where high doping channel is present. In this structures also are dissociated the lateral conduction layer in on-state from the layers sustaining the high voltage in off-state. Eight levels of masks are designed to fabricate these devices by utilizing inter-fingers structures in order to minimize both the Ron-resistance and the device size. Integration compatible planar structures are privileged by utilizing ion implantation to form box doping profiles. The device fabrication process is currently under completion.

5 Acknowledgements

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