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Fabrication of polycrystalline silicon nanowires using conventional UV lithography

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Abstract. Silicon nanowires are processed by using the sidewall spacer formation technique. This technique uses craftily a drawback of anisotropic etching to go beyond optical limits with conventional UV lithography for precision patterns. The final width of the spacer is controlled by the steepness of the etching side and by the uniformity of the wall recovering layer. In our process, a polysilicon layer is deposited by low pressure chemical vapour deposition technique on SiO₂ wall network patterned by conventional UV lithography technique. Accurate control of the etching rate of the polysilicon leads to the formation of nanometric size sidewall spacers with a curvature radius below 100nm. Networks of such parallel polysilicon nanowires were electrically tested in function of temperature (530K<T<200K). Results show that conductivity of undoped polysilicon nanowire is thermally activated at high temperature (T >300K) with thermal activation $E_A \sim 0.3$ eV

1. Introduction

Owing to their physical and electrical properties, SiNWs (silicon nanowires) represent a promising material with strong potential for a large variety of applications. They are currently attracting much attention as promising components for future nanoelectronic devices such as nanowire field effect transistors [1], photonic and optoelectronic devices [2], and as chemical or biological sensors [3, 4]. SiNWs present large advantages: high surface to volume ratio, giant piezoresistivity, surface functionalization, synthesis compatible with large area technology, leading to the development of innovative electronic devices. SiNWs development could significantly impact areas of electronics, genomics, biomedical diagnostics, drug discovery.... They can be prepared by the top-down approach, using various advanced methods such as e-beam [5], AMF [6] or deep UV [7] lithography. The main disadvantage of these advanced lithographic tools with nanometer size resolution rests on the high cost generated. The bottom-up approach usually employs metal catalytic growth for preparation of SiNWs [8]. Thus, VLS (Vapour-Liquid-Solid) growth technique uses metallic nanoparticles as aluminium, nickel, gold... This approach suffers both from metal contamination and the difficulty in precisely positioning the device location.

In this work SiNWs are synthesized by using a well known and low cost technique commonly used in microelectronic industry: the sidewall spacer formation technique. With this preparation, low cost and compatible with silicon technology, SiNWs devices are favourable for many applications. These devices are fabricated by using a polysilicon layer from which SiNWs (more exactly poly-SiNWs) are synthesized.

2. Experimental details

The sidewall spacer formation technique exploits a combination of conventional UV photolithography, anisotropic etching and the excellent homogeneity and reproducibility of conformal CVD processes. This technique results in a well defined spacer of nanometric size. In such case one can define directly nano scale silicon line as poly-SiNWs. The key nanowire fabrication steps are illustrated on the figure 2.

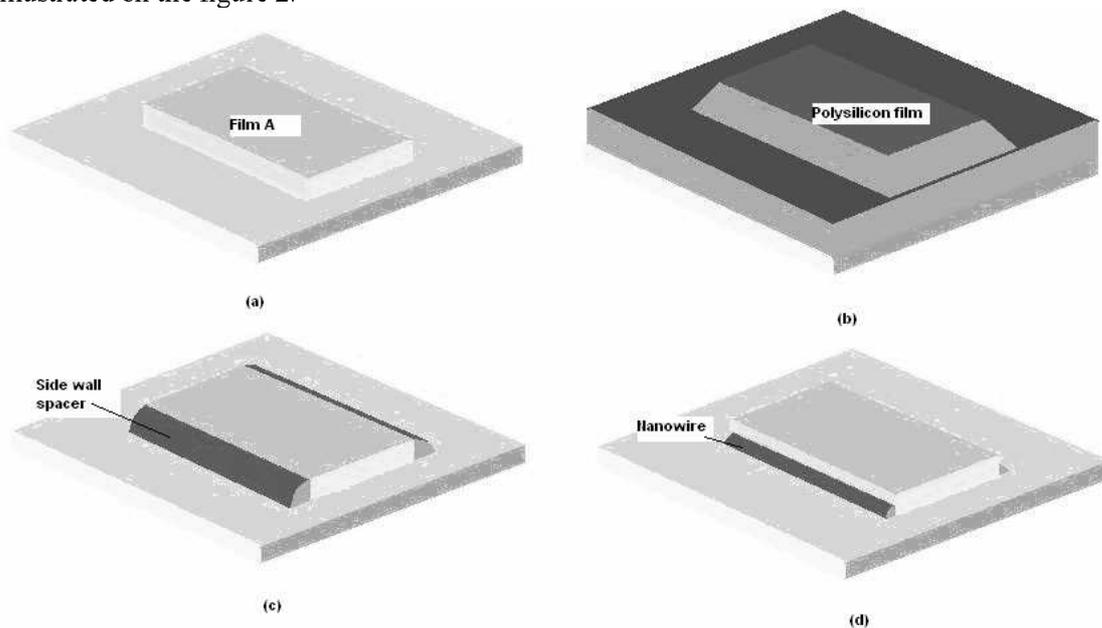


Figure 2: Fabrication steps of SiNWs by the sidewall spacer formation technique

At first a dielectric film A is deposited and patterned into islands by conventional UV lithography (a). An amorphous silicon layer is deposited by LPCVD (low pressure chemical vapour deposition) technique at 550°C (b), and then crystallized by a thermal annealing at 600°C during 12 hours. A Reactive Ion Etching (RIE) of the polysilicon layer leads to wastes of this material on the lower sides of the patterned film A (c). Accurate control of the etching rate leads to the formation of nanometric size sidewall spacers that can be used as nanowires (d). SEM observations were performed to show the shape of the nanowires.

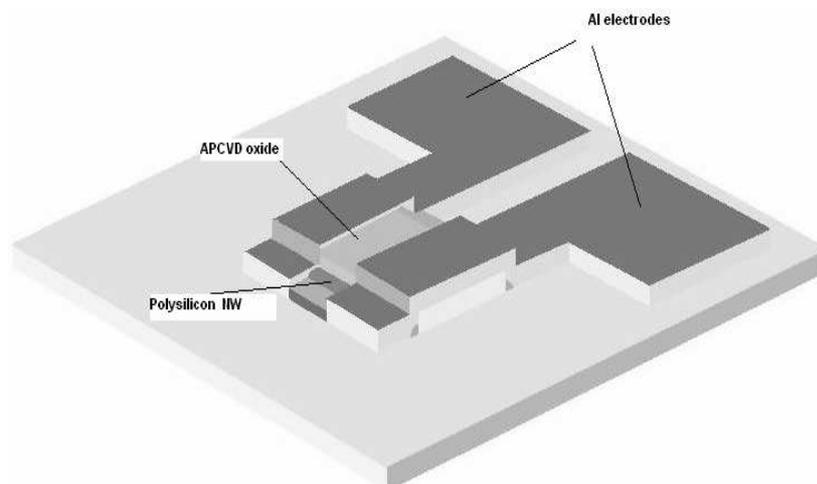


Figure 3 : Polysilicon NWs integrated resistors

Such undoped polysilicon NWs are integrated into resistors (fig. 3) for electrical characterization. In this way, the nanowires were capped by a SiO₂ layer deposited by atmospheric pressure chemical vapour deposition (APCVD) technique at 390°C and contact openings are wet etched. Aluminium was then thermally evaporated and electrodes defined by wet etching.

Static electrical characteristics I(V) are collected at room temperature by using a HP 4155 B semiconductor parameter analyzer. For temperature measurements from 200K to 530K, samples are placed in a cryostat under vacuum (10⁻⁶-10⁻⁵ Pa) and dark current is measured by using a Keithley 617 electrometer.

3. Results

Figure 4 shows SEM micrographs of the cross section of undoped polysilicon NWs obtained by for four increasing over etching durations ($t_1 < t_2 < t_3 < t_4$) of the polysilicon layer wastes. Polysilicon nanowires with a curvature radius below 100nm can be processed by an accurate control of the etching rate of the polysilicon waste. These results highlight the feasibility of this technological step.

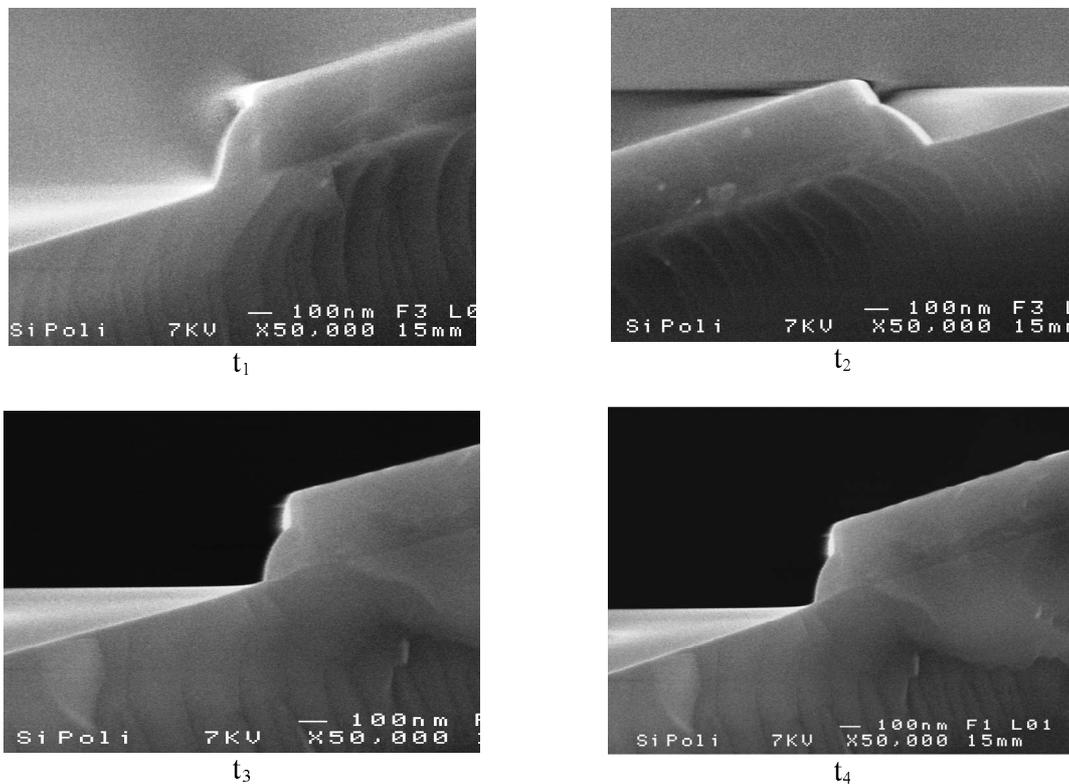


Figure 4 : SEM micrographs of polysilicon NWs obtained for increasing etching duration of polysilicon waste.

On the figure 5 are displayed typical I(V) characteristics of polysilicon NWs resistors (fig. 5 (a)) and plot in semi-logarithmic scale of I versus 1000/T (fig. 5 (b)). Dependence on temperature of the current through a resistor made on polysilicon layer is also given as reference. Results show that the conductivity is thermally activated at high temperatures (230°C < T < 60°C) with a lower activation energy for polysilicon NWs ($E_A \approx 0.3\text{eV}$ against 0.4eV). This electrical behaviour is related to the domination of the thermoionic emission of (trapped) carriers from deep level into the band gap associated with residual impurities and/or structural defects mainly located at the grain boundaries.

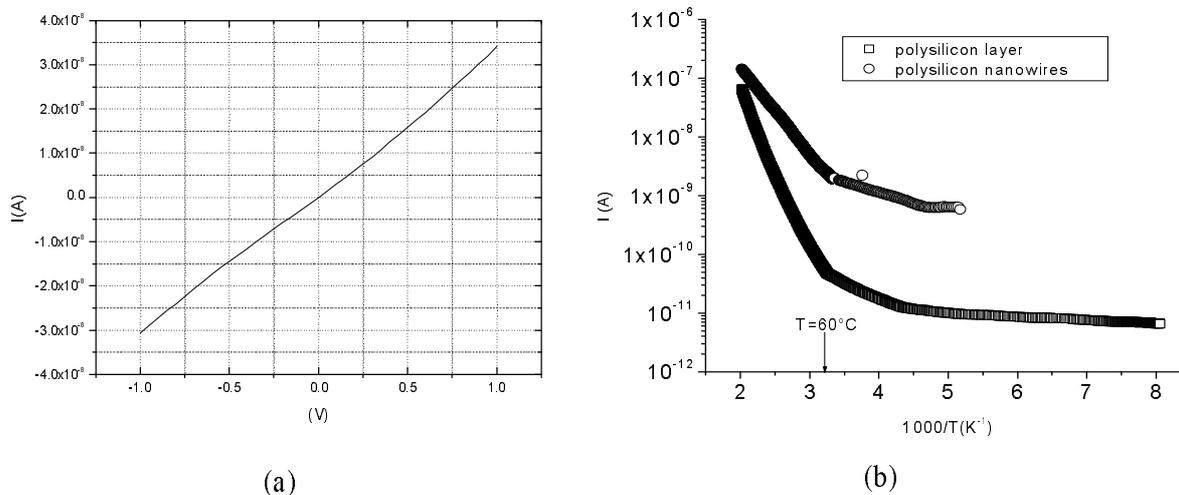


Figure 5: I(V) characteristics of integrated polysilicon NWs resistors (a), Arrhenius plot of the current of the polysilicon NWs (b).

However, for both resistors plots deviate from arrhenius diagram with a weaker dependence at low temperatures. This can be explained by the conduction in localized states [9] usually observed in this range of temperatures for disordered materials. In the case of polysilicon NWs, these states are associated with a higher defect density than in the bulk of a polysilicon layer, located either in the lower part of the polysilicon layer constituting the nanowire and/or at the surface of the wire.

4. Concluding remarks

A good control of both deposited polysilicon film thickness and etching rate can create wastes with very thin width allowing the feasibility of arrays of parallel horizontal polysilicon nanowires by using conventional UV lithography. Electrical properties of these polysilicon nanowires are quite similar to those of corresponding polysilicon layers.

This patterning method represents a simple and manufacturable process of polysilicon nanowires with a high aspect ratio (height/width) that can be used as promising candidates for integrated electronic devices (sensors) applications.

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