Platform Technology For Form Factor Equivalent Microsystems Derived From COTS Components

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Abstract

Recent years have shown the tremendous growth of electronic use in medical devices. Especially active implants and hearing aids have driven that trend to today´s ultra-small devices embedded into the body. While the integrated circuits´ features a ever-decreasing critical geometries and surging performance numbers, the delivery format of such advanced chips is seldom providing the engineering teams with a fully tested, bare die. Miniature implanted devices are hindered in their proliferation by the use of COTS devices, which fail to meet the miniaturization requirements, while on the other hand a dedicated chip run or the procurement of a KGD tested bare die is often cost prohibitive for single and multi chip devices. This paper describes a miniaturization approach using advanced packaging techniques for the electronic system using the example of a miniature camera system (bare die assembly in stack-wirebond and flip chip) suitable for medical imaging. For prototypes, some electronic bare dice are mimicked by de-capsulating the IC from the plastic housing and re-bumping it for use as flip chip. This prototype platform allows to create form factor equivalent circuits with known good chips enabling the demonstration and qualification of miniature devices. In addition, the approach can be used to create 3D stacked systems – this approach is depicted as well.

I. INTRODUCTION

New visual imaging technologies are not driven only by the race to score the highest number of pixels (also known as the "mega-pixel hype") but also by the miniaturization of the associated electronics and optical systems. While consumer cameras in mobile phones boast now 5MP, the optical system so far has been limited to fixed focus or (very recently) to sophisticated zoom mechanisms with limited miniaturization capabilities. Getting the entire sensor-electronic-optical system down to a couple of mm instead of cm could enable next generation high quality mobile devices with visualization capabilities.

First steps using liquid lenses (e.g., byLucent and Varioptic use of electrowetting effect) have been endorsed by OEM manufacturers /1, 2, 3/ in evaluation stages. However, that approach requires some sophisticated control circuitry and needs to retain the position of the optical element actively by applying a continuous electrical field.

A MEMS based camera with self-locking mechanism could overcome the associated energy consumption issue. Electronic signal processing on-chip has gone a long way since camera chips have evolved. Still, additional active and passive circuitry is required to form a fully functional camera system. A side-to-side concept requires much real estate on the substrate of a mobile device. 3D integration is therefore a direct pathway to minimize the impact of this issue.

The first section describes the final goal of a 3D integrated vision system based on 3D assembly techniques and a MOEMs optical system. It highlights the current shortcomings / availability issues for a full integration and describes an intermediate implementation path pursued in this paper. The second section discusses the used components, system design and implementation.

2. VISION OF A CAMERA SYSTEM

A fully integrated camera system as depicted in Figure 1, (recent publication in /[4]/) has been described nearly ten years ago, lacking at that time the implementation technologies required.

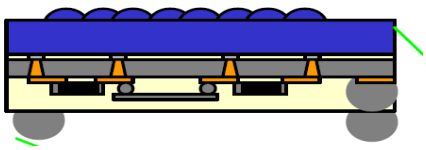

Figure 1: Vision of a fully integrated camera system, depicting a fly-eye micro lens arrangement

Schott has created a through silicon via technology (TSV) /[5]/ for their Opto-CSP that lends itself directly to the respective system design, minus the optics. Together with a MEMS based lens control system incorporating an iris and a tunable lens /[6]/, using wafer/chip stacking, and on.chip rerouting of the contacts, the highest integration level could be achieved therewith [Figure 2]. However, such an optical system will require holographic elements to maximize N.A. and would not easily be adapted to changes in either product chip.

As many of the techniques to manufacture such a maximally integrated system are not readily available, protected by licenses or just not feasible for a prototype phase due to unavailability of full wafers required for through-silicon

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via fabrication, an intermediate approach compiling today´s mainstream packaging technologies (ie. Fine pitch wirebonding and flip chip) with advanced substrate manufacturing was choosen for the current research work. This approach can result in nearly the same dimensions as achievable with the most sophisticated approach as depicted.

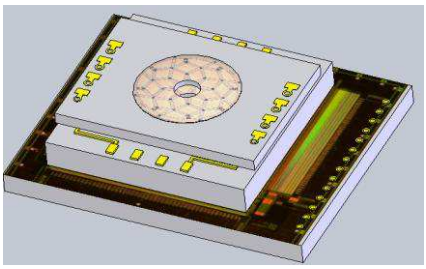

Figure 2: MOEMS enhanced camera system (concept based on 3D TSV and BCB re-routing technology)

Based on a CMOS 768 x 576 pixels ACC sensor /[7]/, a full camera system was designed, providing a IEEE 1394 output. The implementation focused on establishing the interface electronics on a footprint smaller than the actual sensor and mounting the circuitry on the backside of the sensor chip.

3. COMPONENTS

The camera system is comprised of three major functional blocks:

- Image sensor
- Optical system
- Processing and interface electronics

Their specifications and details are given below:

3.a) CMOS Image Sensor

The image sensor was taken from a previous production run by Fraunhofer IMS, Duisburg, and was delivered on a non-diced 6" wafer. The characteristics are given in table 1.

Table 1: Specifications of CIF image sensor

Acquisition	Progressive scan, rolling shutter
Sensitive area	768 x 576 pixels
Total # of pixels	796 x 604
Pixel size	10 µm x 10 µm
filling factor	50 %
total chip area	90 mm^2 (0,5 µm CMOS)
Power supply	3.3 V
Power consumption	typ. 120 mW
Full frame-rate	(20 ms integration time) 50/s
Maximum frame rate (full frame)	66/s
Pixel clock	16 MHz
on chip gain	6

3.b) MEMS Iris and Lens

The MEMS device had been designed by our partnering research institute, The University of Utah, and fabricated in a SUMMiT--V™ run provided by Sandia.

The principle is based on a macro-scale structure /8,9/ for a concentric joint mechanism [Figure 3]. The deployment of the moving structures was based on electrostatic actuation, providing a full open/close cycle in <5° of rotation within a ~10ms time. The actuation principle via the gearwheel mechanism ensures a self-locking in the desired position. Figures 4 and 5 depict details of the MEMS mechanism used for iris actuation.

In addition, using elastic materials like PDMS, deformable lenses can be implemented, allowing variable focal length via the actuation controller.

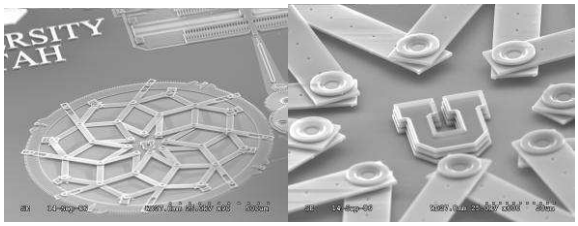

Figure 3: MEMS structure with electrostatic actuation, opening and closing the inner retainer structures by <5° of rotation of the external control wheel

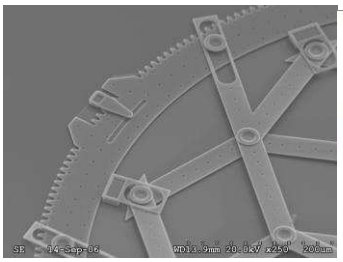

Figure 4: Detail of external wheel hinged lever structures

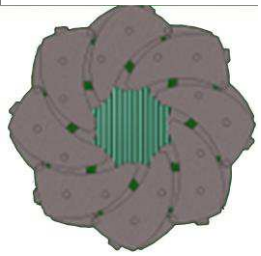

Figure 5: Schematic of iris implementation for aperture control

3.c) Electronic Components

The selection of electronic components was driven by minimizing the total components and utilizing smallest (0201 and 0402) SMD components. Table shows the used integrated circuits and their role in the system

Table 2: Integrated circuits used and delivery format

U1	DS3904	Nonvolatile Digital Potentiometer to fix the bias voltage of camera chip and operating range of ADC	Packaged
U2	CIF	Image Sensor	Bare die
U3	LPV324MT	Op-Amplifier for bias and reference voltage	Packaged
U4	MAX6120ESA	Reference voltage	Packaged
U5	TLC5540	Analog digital converter (ADC) for image data	Packaged
U14	XCR3128xl	CPLD for row-column adressing and serialization of image data	Packaged

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The IC´s –except for the CIF sensor- were procured through standard distribution channels, none of them was available as bare die. From a designer´s perspective, this is a quite normal situation – for small numbers/prototypes, usually the procurement of full wafers is prohibitive due to the associated cost.

4. SYSTEM DESIGN AND IMPLEMENTATION

4.a) Building a library for bare die

The development target was now to realize a subminiature camera module slightly larger in x/y dimensions than the actual image sensor. While previously discussed techniques using Through Silicon Vias (TSV) were at this prototype stage prohibited by cost and material´s availability (i.e. only the sensor was available in wafer format) the principal vision as of figure Figure 1 and Figure 2 was still retained.

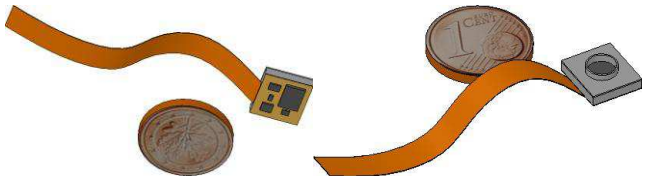

Figure 6: Subminiature camera module - 3D representation

To reach this goal, firstly the required electronic components needed to be converted in a bare die format. For this, a technique developed at IZM was utilized, which foregoes all issues with respect to chemical or plasma etching of hard-to-etch mold compounds or sensitive/predamaged bond pads.

High precision mechanical micro milling (x-y-z precision ~5µm) was employed to remove all mold material from back- and frontside, exposing the bare silicon (backside) and the gold bonds ("nailheads") on the frontside, respectively [Figure 7].

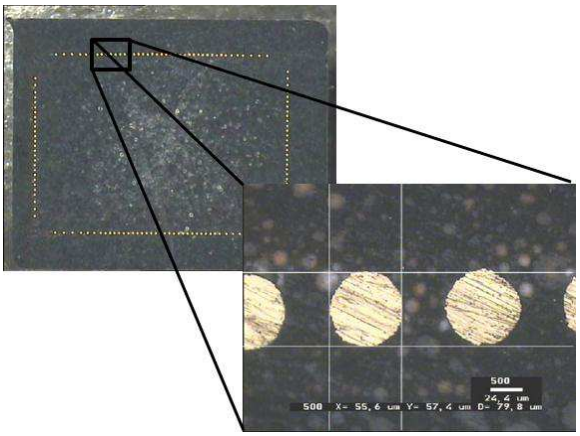

Figure 7: Gold bond heads embedded in mold compound after micro milling exposure

Carefully measuring the chip pad positions using a Jenoptik OKM coordinate machine, for all ICs a library with pad position and allocation was established and used to derive from the circuitry schematics a physical layout.

4.b) Preparing the chips for assembly

On the exposed gold an additional gold stud bump was bonded to create a defined starting point for subsequent processes [Figure 8].

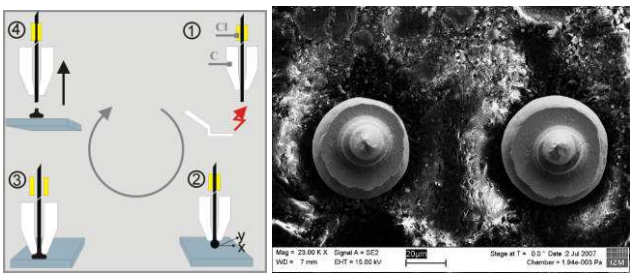

Figure 8: Ball bumping process and bumped exposed chip pads

The exposed and bumped chip, being ~20x smaller and 5x thinner than the COTS package with respect to the microcontroller [Figure 9], could now be used in a CSP/FC like fashion. The other dies had die-to-package footprint ratios of 3 (ADC) .. 36 (CPLD) and 15…150x volume ratio, respectively. This clearly shows that the size advantage of bare die vs. COTS component becomes more significant when dealing with high-pincount IC´s. As a caveat, this advantage (retained also over COB assembly) comes at the price of increased challenges at the substrate level – see next section.

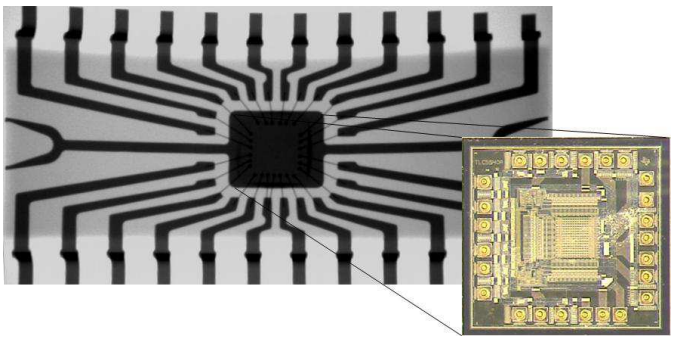

Figure 9: Exposed bare die vs. package outline (µController)

5.PHYSICAL LAYOUT & SUBSTRATE FABRICATION

Using the properties of the Xilinx CPLD, routing could be minimized by selecting the pin in/out´s of this component in an optimized fashion. Still, the resulting design came out with DRC violations even for advanced HDI flexprints (60µm lines/spaces). After careful optimization and leveraging the pad-to-bump overlap size provided by the flip chip assembly process to accommodate for +/-10µm misalignment, the DRC errors could be removed, sacrificing tolerances in the subsequent placement process [Figure 10].

The flexprint itself was a two layer PI (50µm) with 25µm coverlay. The electronic´s site had a 0,25mm thick FR4 stiffener included, providing a mounting basis for the image sensor, which was attached to the frontside via gold-wirebonding. These contacts were routed using drilled (150µm) through-vias to the flex. The entire substrate was prefabricated

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on a FR4 frame to prevent coiling and warping of the flex tail during the thermal processes.

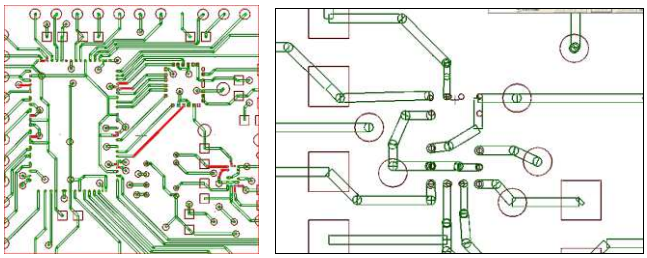

Figure 10: DRC violations (red) and improved situation (detail) after careful pad relocation on the flexpring backside

With the reduced tolerances due to the design, anisotropic conductive adhesive (ACA) interconnects were selected as assembly technology for the signal conditioning and interface electronics on the backside of the flexprint. The dies were all prepared according to the previous description, the SMD´s were mounted into pre-dispensed solder deposits prior ACA assembly.

6. BUILDING THE CAMERA

Having all components in place, firstly the SMD´s were mounted. With a 30gauge (0.16mm) ID needle, solder deposits (SnAgCu0.5) were dispensed via time-pressure controlled dispense system. A Fineplacer manual pick&place equipment providing ~5um accuracy by microscope assisted alignment was used to put the SMD components in place. Reflow soldering was done using a five zone convection oven with a peak temperature of 250°C

For the ACA assembly process of the bare dies, ACA foil was precut with ~100um overlap and positioned using the Fineplacer again on the mounting sites of each flip chip.

A FC150 bond system from Suss providing a sub-µm precision and simultaneously allowing to excert force and temperature to the interconnects was used to bond the chips to the substrate. The ACA film melts during the process, allowing the gold stud bumps to penetrate down to the substrate´s gold protected pads. The thermoset adhesive cures during the assembly process and thereby fulfils three tasks:

a) providing mechanical contact
b) stabilizing the established electrical contact and
c) protecting the assembly from thermal stress
(similar to an underfiller)

The backside was not protected by a molding, as in a final goal the entire assembly was planned to be put into a polymeric, protective camera holder anyway [Figure 11].

After full curing, the assembly was turned around and the CIF sensor was prepared for chip&wire assembly.

As the contact pitch for this die is moderate, no specific challenges were noted. Die-bonding was done at 150°C and gold-ball-wedge bonding connected the CIF sensor to the contact pads, which were routed by through via holes to the populated electronics side.

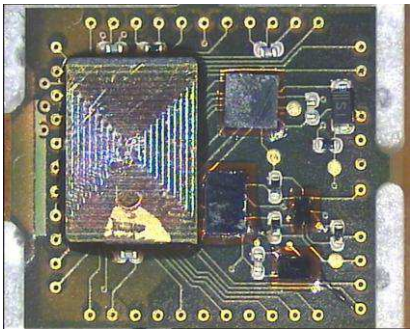

Figure 11: Compleded backside of the micro camera module with ACA assembled circuits

Specifically for the CIF Sensor, protecting the contact wires from any damage required a two-fold dam-and-fill process for the glob top protection [Figure 12].

First, a medium viscosity material with good shape retaining properties was used to dispense a frame close to the gold bond nailheads on the chip (inner frame) and directly adjacent to the substrate bonds on the flex (outer frame). This left the sensitive area of the CIF sensor completely untouched.

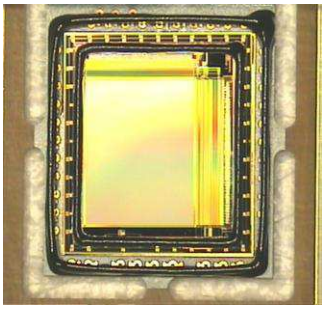

Figure 12: Dual dam approach, leaving the sensor area exposed

With a low viscosity material, the created trench was filled to level, safely enclosing the wires into the epoxy filler. The resulting epoxy bar had a +/-10um surface topography due to the dispense process and flow properties [Figure 13].

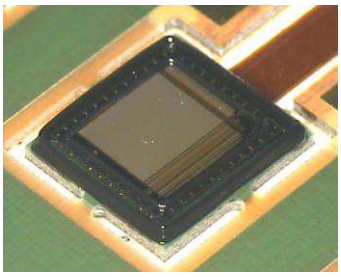

Figure 13: Trench fill process to protect the wirebonds and leave the sensor area exposed

The final (electronic) camera device had an overall dimension of 12.5x10.9x1.54mm versus the CIF sensor alone with 8,77x9.8x0.38mm. As clearly visible in [Figure 11], the additional footprint required is attributed to the through holes and the design requirement for the wire-

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bonding. Processing these as through silicon vias and using instead of the flex circuit a wafer level applied re-routing, another 30% of area could be saved.

7. PREPARING THE MEMS & OPTICAL ELEMENTS

The MEMS devices received from the SUMMiT-VTM process were in an "open iris" configuration and were still in need of through hole fabrication and MEMS release.

The enacted concept uses a laser to drill mill a cavity from the backside and subsequently drill a centered hole through the optical axis of the MEMS device. After release, all contaminations are as well removed from the mechanically moving levers.

Bonding the MEMS dice on top of each other requires a high precision and would need to exclude any mechanical handling of the surface (ie. no flat vacuum pipette would be allowed). To overcome these issues, a design for a suction tool keeping the sensitive areas untouched was made.

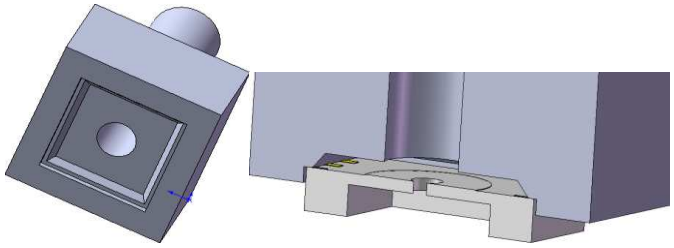

Figure 14: Manipulator for MEMS device with cavity

The cavity is designed to accommodate both the 3x4 and 4x4mm MEMS chips. Applied vacuum drag will retain the chips in position during the bond procedure, without doing any damage to the surface.

Bonding of the MEMS chips on each other with a precision of better than 5µm (i.e. ~1% of the overall opening) is achieved using aligned camera vision on a FC 950 Suss Flip Chip bonder. A thin (~10µm) adhesive layer is spread and the top chip is with its backside "dipped" into the reservoir, taking a minute amount of adhesive to the rim of the cavity. This is sufficient to ensure mechanically stable bonding.

As the used adhesive is not thermally stable, all wire-bonding steps are done with Al wire at room temperature.

A significant challenge encountered was the optical spacer required to allow a full image projection from the iris down to the sensitive area of the sensor chip. While the mechanical contour of the lens holder [see detail in Figure 6] can easily be realized in a stereo-lithographic (STL) prototype process, assembling and interconnecting of the sensitive structures into a 3D element with ~15µm required precision posed a significant challenge and needs further development.

The STL process allows to mimick the high precision of modern molded interconnect devices (MID) without their built in electrical routing functionality. However, using MID as a high volume capable process, a schematic assembly capable of low cost manufacturing can be envisioned and is proposed [Figure 15].

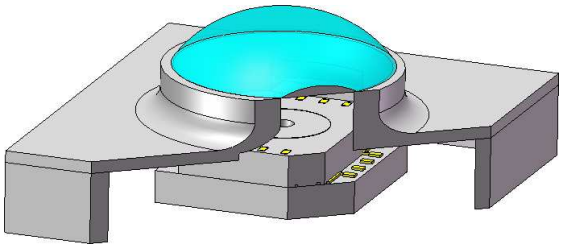

Figure 15: Schematic of a MID integrated optical system holder with MEMS elements und corneal lens cap. Excisions in the holder for the corneal lens allow the wirebonds to stay untouched.

8. CONCLUSION AND NEXT STEPS

Based on COTS devices and a MEMS optical system, a concept for a subminiature camera has been demonstrated. Features not available without sophisticated processes like full wafer TSV´s could be demonstrated by de-capsulating the COTS devices and using high density flex circuitry, creating a 10x10x2mm thick electronic camera system. A MEMS type of optical system featuring a fixed corneal lens, a deployable iris and a variable focus, flexible polymer lens

9. ACKNOWLEDGMENT

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