



HAL
open science

Undulation of sub-100 nm porous dielectric structures: A mechanical analysis

Maxime Darnon, T. Chevolleau, O. Joubert, S. Maitrejean, J.C. Barbe, J.
Torres

► **To cite this version:**

Maxime Darnon, T. Chevolleau, O. Joubert, S. Maitrejean, J.C. Barbe, et al.. Undulation of sub-100 nm porous dielectric structures: A mechanical analysis. Applied Physics Letters, 2007, 91 (19), 10.1063/1.2805774 . hal-00397092

HAL Id: hal-00397092

<https://hal.science/hal-00397092>

Submitted on 15 Jan 2024

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Undulation of sub-100 nm porous dielectric structures: A mechanical analysis

M. Darnon, T. Chevolleau,^{a)} and O. Joubert

LTM/CNRS, CEA-LETI, 17 rue des Martyrs, 38054 Grenoble Cedex 09, France

S. Maitrejean and J. C. Barbe

CEA/LETI/Minatoc/D2NT, 17 rue des Martyrs, 38054 Grenoble Cedex 09, France

J. Torres

STMICROELECTRONICS, Central R&D, 850 rue J. Monnet, 38926 Crolles Cedex, France

(Received 12 June 2007; accepted 16 October 2007; published online 6 November 2007)

In microelectronics technologies, patterning of sub-100 nm width ridges capped with a titanium nitride mask can lead to undulations of the ridges detrimental to performances. This phenomenon is observed with highly compressive residual stress into the mask (>2 GPa), with dielectrics with low elastic properties ($E < 2$ GPa) and with high dielectric ridge heights (>230 nm). Experiments and simulations show that undulations can originate from buckling which allows the release of the strain energy initially stored in the mask. Simulations predict that the dielectric material undulations can become an issue for porous dielectrics integration in the next generations of integrated circuits (2016 and later). © 2007 American Institute of Physics. [DOI: 10.1063/1.2805774]

In microelectronics technologies, transistors are connected by interconnects. To improve interconnect performances, an insulating material with a dielectric constant lower than SiO_2 is required. A dielectric constant lower than 2.9 is obtained by introducing porosity in a methyl silsesquioxane material (porous SiOCH). Those thin films are currently named low k .¹ During interconnect building, a porous SiOCH film is first deposited. It is capped with SiO_2 and a titanium nitride (TiN) mask. Trenches are defined by lithography and patterning processes in the TiN. Then, trenches are etched by plasma using TiN as a mask.^{2,3} The different chemical nature between TiN and porous SiOCH provides a good etch resistance during the exposure to plasmas used for porous SiOCH etching.⁴ We have observed that the etching of dielectric trenches overlaid by a TiN mask can lead to undulations of the masked dielectric ridges (the so-called wiggling phenomenon) when the width of the ridge is lower than 100 nm.⁵ Even if this phenomenon is put in evidence for microelectronics purpose in this letter, it concerns the whole scientific community interested in nanopatterning. The origin of the undulations is still unclear but the shape of the deformed ridges is typical of a buckled structure.⁶⁻⁸ To study the origin of the wiggling, structures with different materials and different sizes have been etched using the following stack: on a silicon wafer, 250 nm thick porous or dense methyl silsesquioxane (SiOCH) is deposited, then 40 nm thick SiO_2 capping is deposited by plasma enhanced chemical vapor deposition and 45 nm thick TiN mask is deposited by physical vapor deposition. Porous and dense materials have been chosen for their similar chemical nature and their dissimilar mechanical behavior, i.e., different elastic properties. The wafers are patterned by direct electron beam lithography in order to achieve structures with ridge widths varying from 100 to 50 nm. The TiN mask is etched in a Cl_2 -based plasma, and the SiO_2 capping layer and the SiOCH are etched with a CF_4 -based plasma. The height of the dielectric

ridge after etching is controlled by adjusting the etching time. Figure 1 represents tilted scanning electron microscopy (SEM) views of the structures after the opening of the TiN mask and after the etching of the dielectric. Figure 2 shows a SEM top view of ridge arrays with porous and dense dielectric materials for different heights and widths of ridges. The wiggling of the porous SiOCH dielectric ridges masked by the TiN mask is observed for sub-100 nm width ridges, with an etch depth of 230 nm and for width lower than 75 nm for the 130 nm height ridges. For the 230 nm height structures with dense SiOCH, the dielectric ridge undulations appear for a ridge width lower than 75 nm. It has to be noticed that the porous SiOCH exhibits a lower Young modulus than the dense SiOCH (see Table I). The undulations of the dielectric structures are observed for a larger ridge width when the ridge height increases (for a ridge height of 130 nm, the wiggling is observed for a ridge width lower than 60 nm).

This demonstrates that the wiggling phenomenon depends on the structure geometry (ridge width and height). Furthermore, we have shown that undulations of sub-100 nm porous SiOCH structures are not observed with a carbon-based mask which presents a lower residual stress than the TiN mask (not presented here).⁵ These results suggest that the dielectric ridge undulations are attributed both to the compressive residual stress of TiN and the weak elastic properties of the narrow dielectric structures. To explain the origin of these undulations, experimental results and mechanical simulations are confronted. The simulations are

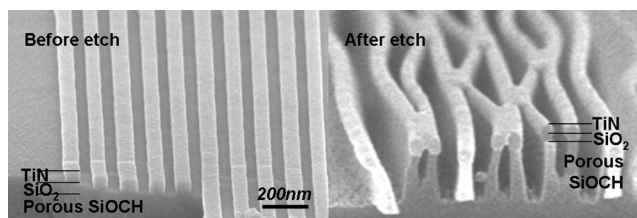


FIG. 1. Tilted SEM view of porous SiOCH/ SiO_2 /TiN stack (left) after the etching of the TiN and (right) after the etching of the porous SiOCH.

^{a)}Electronic mail: thierry.chevolleau@cea.fr

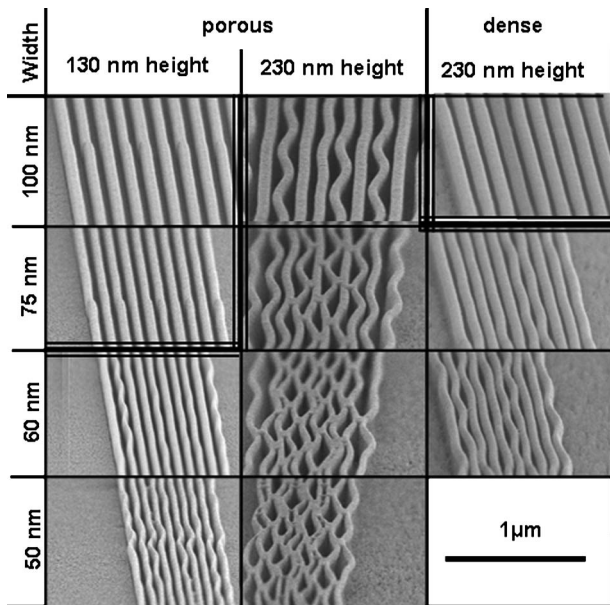


FIG. 2. SEM top view of arrays of dielectric ridges (width=space: 100, 75, 60, 50 nm). Left-hand side: porous SiOCH with a ridge height of 130 nm; middle: porous SiOCH with ridge height of 230 nm; right-hand side: dense SiOCH with an etched depth of 230 nm. Undulations are observed for widths ≤ 60 nm (respectively ≤ 100) with a height of 130 nm (respectively 230 nm) of porous SiOCH ridges and for widths ≤ 75 nm with a height of 230 nm of dense SiOCH ridges.

performed using the commercial mechanical finite element analysis code ANSYSTM. The buckling analysis is for bifurcation buckling using a linearized model of elastic stability. Bifurcation buckling refers to the unbounded growth of a new deformation pattern. The buckling problem is formulated as an eigenvalue problem: $([K] + \lambda_i[S])\{\Psi\}_i = \{0\}$, where $[K]$ is the matrix of stiffness, $[S]$ is the matrix of stress stiffness, λ_i is the eigenvalue, and Ψ_i is the eigenvector of displacement.⁹ The method of eigenvalue extraction is based on subspace method which is described in detail by Bathe.¹⁰ The simulated structure used for buckling analysis consists in a 1 μm long line (porous SiOCH/SiO₂/TiN) on a silicon substrate. All the substrate displacements are constrained, whereas the other material displacements are only constrained along the longitudinal direction on the two ends of the line to simulate an infinite structure. The mechanical properties and residual stress of each layer are given in Table I. Reduced moduli are obtained by nanoindentation using a procedure described in a previous work,¹¹ Poisson coefficients are determined by Brillouin Light Scattering or extracted from literature,¹² and the residual stress is determined using the wafer curvature method.¹³ The whole measurements (see Table I) indicate weaker elastic properties for the

TABLE I. Mechanical properties and residual stress of materials used in our structure.

| Material | E (GPa) | Poisson coefficient | Stress (MPa) |
|------------------|---------|---------------------|--------------|
| TiN | 79 | 0.25 | -2400 |
| SiO ₂ | 75 | 0.17 | 200 |
| Porous SiOCH | 1.9 | 0.23 | 0 |
| Dense SiOCH | 2.8 | 0.23 | 0 |
| Si | 165.7 | 0.218 | 0 |

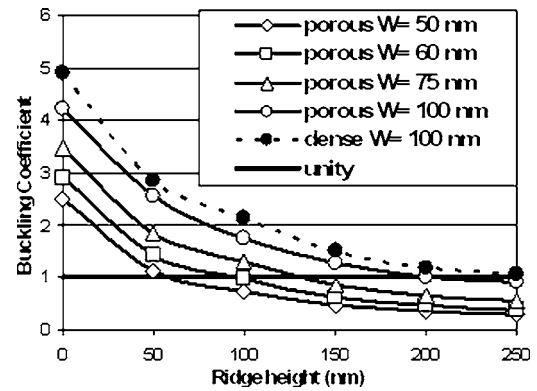


FIG. 3. Evolution of buckling coefficient calculated from the simulation for different height and width of ridges with a porous SiOCH (line) and a dense SiOCH (dots). A Buckling coefficient lower than unity leads to a buckled structure.

porous SiOCH compared to the dense SiOCH and a residual stress which is highly compressive into the TiN layer. The matrix of stiffness and the matrix of stress stiffness are calculated from this structure based on iterative calculation of equilibrium state.

From buckling analysis, we can extract the coefficient by which we have to multiply the matrix of stress stiffness $[S]$ to reach the first buckling eigenmode. This coefficient, the so-called *buckling coefficient*, is critical when it lies under unity.⁹

Figure 3 shows the evolution of the buckling coefficient calculated for different widths and heights of ridges with both dielectric materials. Simulations are in good agreement with the experimental results presented in Fig. 2: when the buckling coefficient is found to be higher than 1, no wiggling is experimentally observed, whereas undulations are experimentally observed when the buckling coefficient is lower than 1. These results point out that buckling can be the mechanical phenomenon leading to structure undulations. Both simulations and experimental results show that the wiggling depends on the compressive residual stress into the TiN mask, the weak elastic properties of the dielectric, and the geometry of the structure. These undulations occur when the elastic properties of the narrow dielectric ridge cannot prevent the release of the residual stress of the TiN mask. The wiggling phenomenon is explained by the residual stress of TiN which releases and deforms the shape of the ridge of porous SiOCH (which exhibits a lower stiffness). This leads to a buckled structure.

This work shows that ridge undulations are emerging as a physical limitation to pattern sub-100 nm dielectric features. This limitation can become an issue in microelectronics for the integration of porous low k dielectrics in the next generations of integrated circuits. We have simulated the mechanical behavior of the dielectric structures using the lowest height and width of dielectric ridges required for the next generations of integrated circuits (Table II). The ridge dimensions are defined by the International Technological Roadmap for Semiconductor (ITRS) industry for the first level of interconnects in microprocessor units.¹⁴ In our simulations, the Young modulus is varied from 0.5 to 10 GPa, which is representative of a wide range of Young moduli experimentally measured for porous SiOCH.^{1,11,15} The mask residual stress ranges from a highly compressive stress (-2.4 GPa) to 0 GPa corresponding to a fully relaxed mate-

TABLE II. Geometrical dimensions recommended by the 2006 International Technological Roadmap for Semiconductor (ITRS) industry for the first level of metal in microprocessor units. Those generations of integrated circuits are supposed to be integrated in 2010, 2013, 2016, and 2019 (Ref. 14).

| Year of integration | 2010 | 2013 | 2016 | 2019 |
|---------------------|------|------|------|------|
| Ridge height (nm) | 81 | 61 | 44 | 32 |
| Ridge width (nm) | 45 | 32 | 22 | 16 |

rial. Other parameters such as TiN thickness are kept constant. Figure 4 gives the map of buckling coefficient as a function of the residual stress of the mask and Young modulus of the dielectric, for the ridge dimensions required in the microelectronics roadmap [ITRS (Ref. 14).] for the years 2010, 2013, 2016, and 2019. The curve plotted for each generation of integrated circuits defines the limit between the domain of stability and the domain in which the wiggling phenomenon occurs: at lower mask residual stress and higher dielectric Young modulus, structures are stable and will not undulate (buckling coefficient greater than unity), whereas at higher residual stress and lower Young modulus, the buckling phenomenon will occur. Thanks to those simulations, we can predict the ridge undulations for each generation of integrated circuits according to the mechanical properties of the porous dielectric and to the residual stress into the mask. For example, in our experimental conditions (residual stress

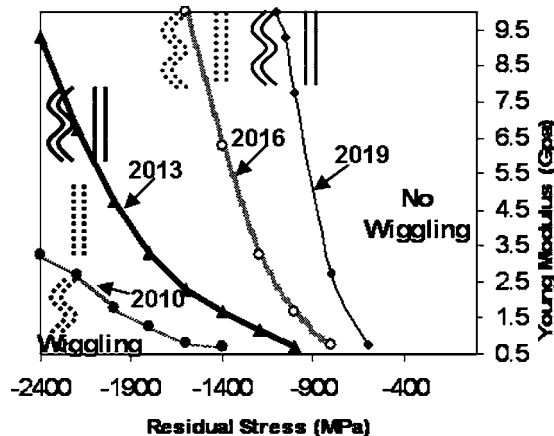


FIG. 4. Map of buckling coefficient thresholds as a function of dielectric Young modulus and mask residual stress plotted for the geometrical dimensions corresponding to ridges dimensions of the next integrated circuits integrated in 2010, 2013, 2016, and 2019. Each curve shown in this graph corresponds to a buckling coefficient of 1 and separates the residual stress/Young modulus plan into two areas. For each generation of integrated circuits, the left part of the plan delimited by the curve corresponds to a buckling coefficient lower than 1 (wiggling), while the right part corresponds to a buckling coefficient higher than 1 (no wiggling).

of -2.4 GPa and Young modulus of 1.9 GPa), no mechanical limitation is expected before 2013 for the ridge dimensions defined in the ITRS. Based on this simulation, Fig. 4 highlights that the development of mask materials presenting a low residual stress is the key point to prevent the wiggling phenomenon for the most advanced generations of integrated circuits (2016 and after).

In this letter, mechanical simulations show that the undulations of narrow structures of porous dielectric can result from a buckling phenomenon. These results are in agreement with the experimental data, and the structure undulations are explained by the release of the residual stress of TiN which deforms the less-stiff porous SiOCH leading to a buckled structure. For the next generations of integrated circuits in microelectronic industry, our results can predict structure undulations knowing the dielectric material Young modulus and the residual stress into the mask. The development of masks with a low residual stress will be the key point to prevent structure undulations for the most advanced generation of integrated circuits (2016 and after).

- ¹K. Maex, M. R. Baklanov, D. Shamiryan, F. Iacopi, S. H. Brongersma, and Z. S. Yanovitskaya, *J. Appl. Phys.* **93**, 8793 (2003).
- ²M. Fayolle, G. Passemard, O. Louveau, F. Fusalba, and J. Cluzel, *Microelectron. Eng.* **70**, 255 (2003).
- ³O. Hinsinger, R. Fox, E. Sabouret, C. Goldberg, C. Verove, W. Besling, P. Brun, E. Josse, C. Monget, O. Belmont, J. Van Hassel, B. G. Sharma, J. P. Jacquemin, P. Vannier, A. Humbert, D. Bunel, R. Gonella, E. Mastromatteo, D. Reber, A. Farcy, J. Mueller, P. Christie, V. H. Nguyen, C. Cregut, and T. Berger, *Tech. Dig. - Int. Electron Devices Meet.* **2004**, 317 (2004).
- ⁴M. Darnon, T. Chevolleau, D. Eon, L. Vallier, J. Torres, and O. Joubert, *J. Vac. Sci. Technol. B* **24**, 2262 (2006).
- ⁵M. Darnon, T. Chevolleau, T. David, D. Perret, J. Torres, and O. Joubert, presented at The 16th International Workshop on Materials for Advanced Metallization, Bruges, Belgium, 5–7 March 2007 (unpublished).
- ⁶X. D. Zhu, K. Narumi, and H. Naramoto, *J. Phys.: Condens. Matter* **19**, 236227 (2007).
- ⁷N. Bowden, S. Brittain, A. G. Evans, J. W. Hutchinson, and G. M. Whitesides, *Nature (London)* **393**, 149 (1998).
- ⁸J. Kim, Y. S. Chae, W. S. Lee, J. W. Shon, C. J. Kang, W. S. Han, and J. T. Moon, *J. Vac. Sci. Technol. B* **21**, 790 (2003).
- ⁹ANSYS documentation, release 10.0.
- ¹⁰K. J. Bathe, *Finite Element Procedures* (Prentice Hall, Englewood Cliffs, NJ, 1996).
- ¹¹F. Ciaramella, V. Jousseume, S. Maitrejean, M. Verdier, B. Remiat, A. Zenasni, and G. Passemard, *Thin Solid Films* **495**, 124 (2006).
- ¹²G. Carlotti, N. Cherault, N. Casanova, C. Goldberg, and G. Socino, *Thin Solid Films* **493**, 175 (2005).
- ¹³W. D. Nix, *Metall. Trans. A* **20A**, 2217 (1989).
- ¹⁴http://www.itrs.net/Links/2006Update/FinalToPost/09_Interconnect2006Update.pdf, ITRS 2006 update-Interconnect, downloaded 13 April 2007.
- ¹⁵C. Murray, C. Flannery, I. Streiter, S. E. Shulz, M. R. Baklanov, K. P. Mogilnikov, C. Himcinschi, M. Friedrich, D. R. T. Zahn, and T. Gessner, *Microelectron. Eng.* **60**, 133 (2002).