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On the interest of carbon-coated plasma reactor for advanced gate stack etching processes

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In integrated circuit fabrication the most wide spread strategy to achieve acceptable wafer-to-wafer reproducibility of the gate stack etching process is to dry-clean the plasma reactor walls between each wafer processed. However, inherent exposure of the reactor walls to fluorine-based plasma leads to formation and accumulation of nonvolatile fluoride residues (such as AlF_x) on reactor wall surfaces, which in turn leads to process drifts and metallic contamination of wafers. To prevent this while keeping an Al_2O_3 reactor wall material, a coating strategy must be used, in which the reactor is coated by a protective layer between wafers. It was shown recently that deposition of carbon-rich coating on the reactor walls allows improvements of process reproducibility and reactor wall protection. The authors show that this strategy results in a higher ion-to-neutral flux ratio to the wafer when compared to other strategies (clean or SiOCl_x -coated reactors) because the carbon walls load reactive radical densities while keeping the same ion current. As a result, the etching rates are generally smaller in a carbon-coated reactor, but a highly anisotropic etching profile can be achieved in silicon and metal gates, whose etching is strongly ion assisted. Furthermore, thanks to the low density of Cl atoms in the carbon-coated reactor, silicon etching can be achieved almost without sidewall passivation layers, allowing fine critical dimension control to be achieved. In addition, it is shown that although the O atom density is also smaller in the carbon-coated reactor, the selectivity toward ultrathin gate oxides is not reduced dramatically. Furthermore, during metal gate etching over high- k dielectric, the low level of parasitic oxygen in the carbon-coated reactor also allows one to minimize bulk silicon reoxidation through HfO_2 high- k gate dielectric. It is then shown that the BCl_3 etching process of the HfO_2 high- k material is highly selective toward the substrate in the carbon-coated reactor, and the carbon-coating strategy thus allows minimizing the silicon recess of the active area of transistors. The authors eventually demonstrate that the carbon-coating strategy drastically reduces on-wafer metallic contamination. Finally, the consumption of carbon from the reactor during the etching process is discussed (and thus the amount of initial deposit that is required to protect the reactor walls) together with the best way of cleaning the reactor after a silicon etching process. © 2007 American Vacuum Society. [DOI: 10.1116/1.2464126]

I. INTRODUCTION

With the ongoing tremendous scaling down of integrated circuit (IC) dimensions to enhance microprocessor working speed, new technological challenges are regularly raised. In front-end processes, a major concern is laid on the gate critical dimension control. The allowable total variability is less than 12% of the final gate size,¹ meaning that nanometric linewidth control must be achieved across large-size wafers, from lot to lot. Thus wafer-to-wafer reproducibility becomes more and more critical. With regard to gate stack plasma etching, changes in the reactor wall conditions (e.g., chemical composition, erosion, and roughness) are clearly identified as important causes of process drifts.²⁻⁴ Examples of these changes are changes in etch rates, etching selectivity,

and etching profiles. In the high-density low-pressure plasmas typically used to pattern gate transistors, the diffusion rate of atoms and radicals to the reactor walls is much larger than the rate of chemical reactions in the gas phase. Therefore, the overall plasma chemistry is determined by (1) chemical processes occurring at the reactor walls and (2) electron impact dissociation of molecules in the gas phase. This explains why wafer-to-wafer etch process reproducibility became an issue.

Indeed, in IC fabrication, plasma reactors were traditionally seasoned by etching dummy wafers so that reactor walls get coated with the same material that is deposited during the etching process. By doing so, chemical composition of the reactor walls remains roughly unchanged, but the buildup of etch products (or parent-gas fragments) on the inner parts of the reactor might lead to process drifts because the reactor conditions are never exactly reproducible. In particular, pro-

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cess drifts are expected due to changes in the coupling efficiency between the rf coil and the plasma⁵ and thus in the electron energy distribution function. But the main drawback of this strategy is that the polymer coated on the reactor walls starts to flake off when it becomes too thick, generating particles. The reactor must then be opened and stopped for a long period, and with such a strategy the mean time between reactor wet cleans (MTBC) is thus reduced.

In addition, new materials are introduced in the gate stack (metals and high- k gate dielectrics) to improve the electrical performance of the transistor. As a result, the number of process steps required to pattern a gate stack is increasing, and the same reactor is exposed to the etching of a wide variety of materials using different plasma chemistries. Managing the reactor walls to get a good wafer-to-wafer reproducibility under such condition becomes an art.⁶ The most wide spread strategy used in the industry to reach this goal is to dry-clean the reactor after each wafer etched. This approach allows, in principle, the etching process to always start under reproducible reactor wall conditions, thus preventing process drifts. For example, after a silicon etching process in typical $\text{HBr}/\text{Cl}_2/\text{O}_2$ chemistries, which tends to form silicon oxychloride layers on the reactor walls,⁷⁻⁹ the reactor dry-cleans can be achieved in fluorine-based chemistries.⁸

However, it has been shown,^{10,11} that repeated exposure of Al_2O_3 reactor walls to fluorine-based plasmas results in the formation and accumulation of nonvolatile AlF_x materials on the reactor walls. This slow AlF_x buildup is responsible for process drifts (due to the uncontrolled release of F atoms during the etching process)¹² and flake-off of AlF_x particles.¹³ To prevent these issues, two possibilities can be explored: (1) changing the reactor wall material and (2) coating the Al_2O_3 walls by a protective layer between each wafer to prevent their exposure to F atoms.

Recently, both Singh *et al.*¹⁴ and Cunge *et al.*¹⁰ suggested a new cleaning/conditioning strategy to enhance process reproducibility and MTBC: this strategy consists in coating the reactor walls with a carbon-rich layer before the etching of each wafer. Cunge *et al.*¹⁰ suggested that F-deficient (ideally F-free) carbon-rich coatings protect the reactor walls from exposure to F atoms and at the same time provide a reproducible reactor condition. They showed that etching processes are highly reproducible with this strategy since they always start with the same carbon-coated reactor wall conditions. Etch by-products deposited during the etching process are then removed in a fluorine-based plasma and finally O_2 stripping is performed to remove the carbon coating without damaging the reactor walls. This multistep reactor dry cleaning protects the reactor walls from exposure to F-based plasmas, therefore preventing AlF_x formation and flaking off,¹¹ resulting in an increased mean time between reactor wet cleans (MTBC).

In contrast, Singh *et al.*¹⁴ suggested using a fluorine-rich fluorocarbon film to coat the reactor walls so that after a silicon etching process the $\text{SiOCl}_x\text{-CF}_y$ mixed layer present on the reactor walls can be cleared by an O_2 plasma before etching the next wafer. The coating can be formed, for ex-

ample, during the fluorocarbon etching of an oxide hard mask.¹⁵ However, they did not investigate in detail the impact of such coatings on process reproducibility and on etching characteristics, and it is not clear whether AlF_x formation is suppressed by using a fluorine-rich coating. Furthermore, uncontrolled F atoms released from the fluorine-rich CF_x coating can affect the etching characteristics (etch rate, selectivity, and anisotropy), a phenomenon that was already responsible for subtle process drifts in AlF_x reactors.¹²

Finally, the reactor walls can also be coated with a SiOCl_x layer before each process to enhance wafer-to-wafer reproducibility (this coating is removed from the walls in a SF_6 plasma after the etching process). This strategy has been used for years in our laboratory, and in the present work such SiOCl_x -coated reactors will be referred to as standard conditions (we never work in a clean reactor for the reason that the AlF_x -coated walls release F and Al atoms in the plasma). We underlined that in an Al_2O_3 reactor, this strategy does not prevent AlF_x formation and particles eventually flake off onto the wafers after a long plasma period. However, such a SiOCl_x coating (formed in a SiCl_4/O_2 plasma) may be an interesting conditioning strategy if the reactor walls are made from an Al-free material.

Since plasma etching processes are extremely sensitive to reactor wall conditions, the aim of this article is to discuss the impact of the carbon-coating strategy on advanced gate etching process performances, when compared to more conventional SiOCl_x -coated reactor walls. Surprisingly, we will show that the carbon-coating strategy can facilitate profile control of etched structures with only a minor modification of typical etching recipes. At the same time the carbon-coating strategy allows the reduction of silicon recess and metallic contamination of the wafer.

II. EXPERIMENTAL SETUP

Experiments are carried out in two different high-density inductively coupled industrial plasma sources accepting 200 mm diameter wafers: DPS from Applied Materials and Lam Research Corporation TCP 9400 etch reactors.

The DPS reactor consists of a ceramic dome (sintered alumina) around which is wrapped a three-dimensional coil. A radio-frequency (rf) inductive source power at 12.56 MHz is supplied to the antennae to create and sustain the plasma, while the bottom electrode, which controls the energy of the ions bombarding the wafer, is powered at 13.56 MHz (bias power). In all the experiments described below, the wafer temperature is kept at 50 °C by helium backside cooling (monopolar electrostatic chuck with polyimide coating), while the Al_2O_3 reactor walls (anodized aluminum) are kept at 80 °C and the dome at 60 °C. The reactor is equipped by real time reflectometry and is modified to be connected to an x-ray photoemission spectroscopy (XPS) system by a robotized vacuum transfer chamber allowing quasi *in situ* analysis.

The second inductively coupled plasma (ICP) reactor (Lam 9400) has a flat quartz roof on which lies the rf coil, powered at 13.56 MHz to excite the plasma, while the ion

TABLE I. Plasma operating conditions in the DPS reactor. Low O₂ gas flow rates (<5 SCCM) are obtained with a He(70%)–O₂(30%) mixture.

Plasma No.	Gas flow rates (SCCM)	Pressure (mTorr)	Source power (W)	Bias power (W)	Duration (s)
1	Cl ₂ (90)/O ₂ (10)	10	450	120	60
2	CH ₂ F ₂ (30)/HBr(200)	10	500	0	120
3	HBr(120)/Cl ₂ (40)/O ₂ (1.5)	4	250	120	...
4	HBr(180)/Cl ₂ (30)/O ₂ (5)	30	640	100	...
5	HBr(180)/O ₂ (1)	65	400	70	...
6	Ar (200)	4	800	100	8
7	HBr(100)/Cl ₂ (50)	10	500	15	...
8	HBr(50)/Cl ₂ (100)	10	500	15	...
9	BCl ₃ (100)	5	800	10	...

energy is independently controlled by a second, phase-locked 13.56 MHz rf source. The anodized aluminum walls of the reactor are kept at 50 °C, while the wafer temperature is kept at 65 °C. This reactor is equipped for a gas phase analysis by UV absorption spectroscopy,¹⁶ mass spectrometry,¹⁷ and an ion flux probe.¹⁸

The etching process of advanced gate stacks is developed in the DPS reactor. For this study, the metal gate stack used is composed of HfO₂ (3.5 nm, deposited by atomic layer deposition)/TiN (10 nm)/lightly *n*-doped polysilicon (50 nm) and a 50 nm thick SiO₂ hard mask. The pattern is obtained using direct electron beam lithography of a chemically amplified resist, which after development has been used to pattern the hard mask with a resolution down to 50 nm. As discussed before, in the so-called standard conditions the reactor walls are coated by a SiOCl_x layer. This layer is deposited on the reactor walls either by running the etch recipe of interest with a blanket silicon wafer on the chuck or, which is roughly equivalent,⁶ by etching a silicon wafer in Cl₂/O₂ chemistry (plasma 1 in Table I) before the etch process.⁷ Performances of this process (such as etch rate, selectivity toward gate oxide, and profile control) are compared with those achieved when the etch process is performed in a carbon-coated reactor. Deposition of the carbon coating on the reactor walls is performed in a CH₂F₂ chemistry, strongly diluted in HBr gas (plasma 2 in Table I) to reduce the fluorine content in the film (which should ideally be fluorine-free).¹⁰ This leads to the deposition of a carbon-rich film containing about 16% of Br and 11% of F (atomic concentrations measured by XPS). To complement the information obtained in the DPS reactor, gas phase analyses are performed in the Lam machine. To compare the results obtained in both reactors, the plasma parameters of the etch recipes are tuned to account for the different reactor geometries. In particular, injected rf source power is adjusted to keep the power density (W m⁻³) unchanged, and the CH₂F₂ gas used in the DPS reactor is replaced by a CH₄/CF₄ mixture in the Lam tool. It has been checked that similar process performances are obtained in both reactors and that composition and deposition rates of the carbon coating on the reactor walls are similar in both etching tools.

The information on the gate etching profile is obtained using high-resolution transmission electron microscopy (TEM) gate cross sections. The chemical nature of passivation layers formed on the gate sidewalls is derived from chemical topography XPS analyses.¹⁹ Briefly, by arranging a properly chosen array of etched lines perpendicularly to the axis of the electron analyzer, geometrical shadowing by adjacent features allows detection of photoelectrons coming from the top and sidewalls of the lines only. Separation between contributions originating from the insulating hard mask and the conducting silicon gate can then be achieved by electrostatic charging using a low energy electron flood gun. More details on this technique can be found elsewhere.¹⁹

XPS measurements are performed on a customized 220I spectrometer from VG Scientific, directly connected under vacuum to the DPS etching tool. The monochromatized Al K α x-ray source (1486.6 eV photons) is used at a constant dwelling time of 100 ms and a pass energy of 20 eV. Peak areas are determined after spectral deconvolution based on an iterative numerical fitting procedure (Levenberg-Marquardt algorithm). Individual line shapes are simulated with combinations of Lorentzian and Gaussian functions. A Shirley function is used to perform background subtraction. After correction of the spectrometer lens transmission factor, a relative concentration of detected elements is obtained by dividing calculated peak areas by the Scofield cross section corresponding to the core level analyzed.

Mass spectrometry experiments are carried out in the Lam reactor using a Hiden Analytical electrostatic quadrupole plasma analyzer. It consists of a differentially pumped extractor located on the reactor's sidewall, ionizer, energy filter, quadrupole mass filter, and detector. In the neutral detection mode, also called residual gas analysis (RGA), the extractor is positively biased to repel ions of the plasma, and neutrals sampled through the 50 μ m orifice are ionized by 70 eV electrons created by tungsten filament heating. To correct for fluctuations in the electron flux emitted by the filament, two signals (i.e., two different masses) are acquired simultaneously: one corresponding to species existing in the gas before the plasma is switched on (for example, SF₆), and the

other one to the neutral of interest created in the plasma (for example, SiF_4). For given plasma conditions the density of the first species (SF_6) before the plasma is struck is constant, and the measured signal intensity can thus be used to calibrate the second signal during the plasma ON period. This procedure allows a reliable comparison of relative density of neutrals for different plasma/reactor wall conditions.

In the ion analysis mode, the extractor is slightly negatively biased to give the ions a minimum energy, allowing their focusing in the transport system. Ion energy distribution functions (IEDFs) are first recorded for three ions having very different masses (for example, 27, 135, and 303 amu). If IEDF of these ions are single peaked around the same value, it is assumed that IEDF of all ions are single peaked around this energy (i.e., the dc value of the plasma potential). It is then valid to use this value as the optimum pass energy for the recording of ion mass spectrum.¹⁷ A Scientific System ion flux probe¹⁸ located at the reactor walls in a position symmetric to the entrance hole of the mass spectrometer provides the value of the total ion Bohm flux leaving the plasma. By equating this ion flux with the sum of all the mass peaks present in the ion mass spectrum, the latter can be converted from counts s^{-1} to mA cm^{-2} . Then, mass spectra obtained for different plasma/reactor wall conditions can be directly compared on an absolute scale.¹⁷ In the ion operating mode of the mass spectrometer, we also acquired IEDF at a given mass repeatedly at about 2–3 Hz. Integrated ion energy distribution then provides the time variation of the density of a specific ion.

For broadband UV absorption spectroscopy (BBUVAS) measurements,²⁰ the light from a 150 W UV-enhanced Xe arc lamp (Oriel) was passed through the Lam reactor just above the wafer. A 50 cm focal length monochromator (Acton500i) equipped with either a 600 or 1200 grooves/mm ruled grating disperses the UV light, which is then detected by a 1024-channel photodiode array (Oriel Instaspec II PDA). The details of UV absorption measurements, the absorption spectra of SiCl_x ($x=0-2$) radicals, and the way to deduce the absolute concentrations of these species have been presented in detail by Kogelschatz *et al.*¹⁶ The degree of dissociation of pure Cl_2 plasma is estimated by measuring the depletion of Cl_2 induced by the plasma from its weak absorption continuum between 250 and 400 nm using BBUVAS (Ref. 21) and laser absorption at 355 nm.²²

III. RESULTS AND DISCUSSION

A. Impact of carbon-coated reactor walls on the plasma chemistry

The impact of using a carbon-coated reactor (instead of a SiOCl_x -coated reactor) on the plasma chemistry has been investigated by BBUVAS and mass spectrometry in the Lam reactor. For the sake of simplicity pure Cl_2 plasmas have been used for this purpose.

To begin with, the density of Cl_2 molecules, $[\text{Cl}_2]$, has been measured by BBUVAS in a 68 mTorr Cl_2 plasma (700 W rf power, no wafer) operated either in a SiOCl_x or in

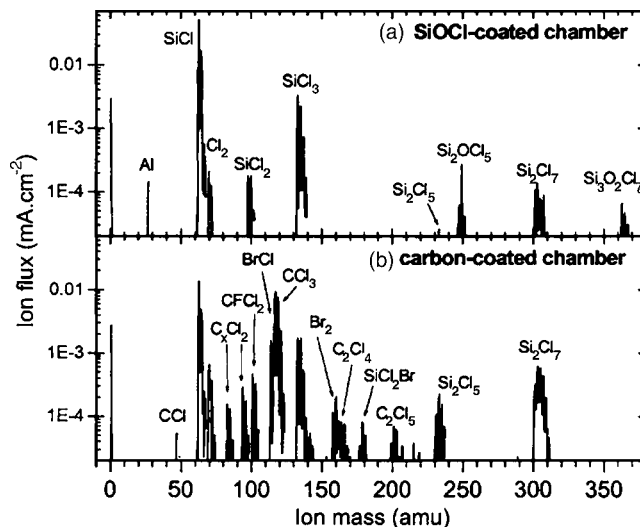


FIG. 1. Calibrated ion mass spectrum measured during the etching of a blanket silicon wafer in a 20 mTorr Cl_2 plasma (100 SCCM) with 300 W rf source power and 90 W rf bias power, operated either (a) in a SiOCl_x -coated reactor or (b) in a carbon-coated reactor. Both spectra are on the same scale.

a carbon-coated reactor. The percent dissociation $\alpha = 100 \times (1 - [\text{Cl}_2]/[\text{Cl}_2]^0)$ of the gas in these two different reactor wall conditions (where $[\text{Cl}_2]^0$ is the Cl_2 density without plasma) is measured. Cl_2 gas is dissociated at 82% in the SiOCl_x -coated reactor, while under the same conditions it is dissociated only at 35% in the carbon-coated reactor. At lower pressure (20 mTorr Cl_2 and 700 W rf power) laser absorption measurements show that $\alpha > 90\%$ in the SiOCl_x -coated reactor and $\alpha = 55\%$ in a chlorocarbon-coated reactor. Therefore, under identical plasma operating conditions Cl_2 gas is more dissociated in the SiOCl_x -coated reactor, which means that the Cl atom density is much higher in a SiOCl_x reactor than in a carbon-coated reactor.

This phenomenon can also be observed during silicon etching at lower pressures by using mass spectrometry to analyze the chemical nature of the ion flux impinging on the reactor walls. Figure 1 compares the ion mass spectrum measured during the etching of blanket silicon wafers in a 20 mTorr Cl_2 plasma (300 W source power/90 W bias power) in either SiOCl_x or carbon-coated reactors. Figure 2 shows the same result in a 5 mTorr Cl_2 plasma. Both Figs. 1 and 2 show that the Cl_2^+ ion density is much higher in the carbon-coated reactor, in good agreement with BBUVAS measurements. Figure 2 shows that at low pressure the $\text{Cl}_2^+/\text{Cl}^+$ density ratio is about 30 times higher in the carbon-coated reactor than in the SiOCl_x reactor. The explanation for this decrease of the Cl atom density in the carbon-coated reactor lies on two phenomena:

1. The recombination coefficients of atomic halogens on surfaces exposed to the plasma are strongly surface material dependent. Indeed, homonuclear recombination rates of Cl atoms²³ and Br atoms^{3,24} are greater on carbon-based surfaces than on SiO-like surfaces, explaining the higher Cl_2 to Cl density ratio measured in the carbon-coated reactor.

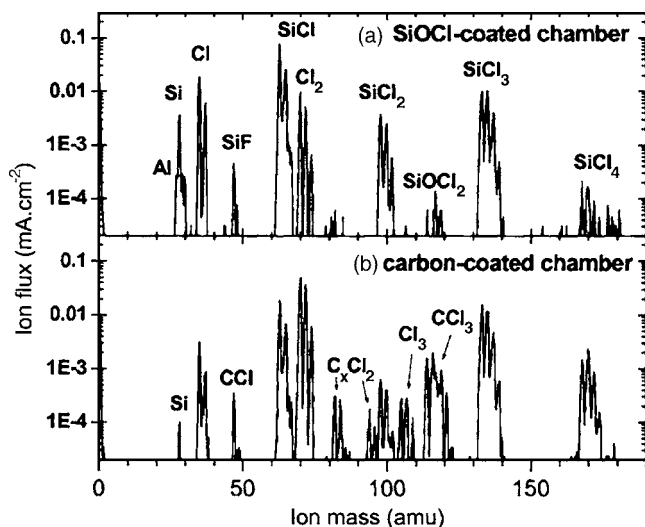


FIG. 2. Identical to Fig. 1 but in a 5 mTorr Cl_2 plasma.

- In the carbon-coated reactor there is an additional surface loss mechanism for Cl atoms: the etching of the carbon coating, which consumes Cl atoms and therefore induces a strong loading of the Cl density (in contrast, the SiOCl_x coating is not etched without energetic ion bombardment⁹). Evidence that the carbon coating is etched by chlorine atoms are shown in Figs. 1 and 2 with the presence of numerous C_xCl_y peaks in the ion mass spectra recorded in the carbon-coated reactor. Since the carbon coating also contains bromine and fluorine, it is not surprising to observe BrCl , Br_2 , or CFCl_2 mass peaks in this case. Similarly, C_xBr_y peaks appear in the ion mass spectra registered during silicon etching in pure HBr chemistry in the carbon-coated reactor.

For these reasons, we conclude that the halogen atom (Cl and Br) loss rate on reactor walls, which includes both homo- and heteronuclear recombinations and chemical etching reaction, is much higher in a carbon-coated reactor than in a SiOCl_x -coated reactor, thus dramatically decreasing the Cl and Br atom density in the gas phase.

Figures 1 and 2 show that besides the higher Cl_2 density and the appearance of C_xCl_y products in the plasma, there is another impact of the carbon-coated walls on the plasma chemistry: the silicon etch product distribution is shifted toward higher mass (chlorine saturated) etching by-products such as SiCl_4 or Si_2Cl_6 . To understand this point, one should first know the silicon life cycle in Cl_2 -based plasmas.^{25–29} In these plasmas, volatile etch products (SiCl_2 and SiCl_4) are produced from the wafer, and then ionized and dissociated into the plasma, leading to the formation of reactive radicals and ions that will stick on the reactor walls with a high probability. Without O atoms in the plasma, the silicon-based products deposited on the reactor walls do not stay on the reactor walls but are recycled into the plasma as volatile SiCl_4 molecules. As a result, the SiCl_4 density can be very high (even if the plasma is strongly dissociated) because SiCl_4 is produced both by the wafer and by the reactor walls.

In contrast, with O atoms in the plasma the silicon deposited on the reactor walls can be oxidized at the reactor wall surfaces instead of recycled into the plasma, thus reducing the production rate of SiCl_4 from the reactor walls and leading to the deposition of a SiOCl_x layer on the reactor walls. As a result, it is well established that the density of volatile silicon etch products drops when the O density in the plasma increases.²⁶ Therefore, the higher density of SiCl_4 (and Si_2Cl_6) measured in the carbon-coated reactor in Figs. 1 and 2 (although the etch rate is smaller as discussed below) suggests that the O atom density is lower in the carbon-coated reactor than in the SiOCl_x -coated reactor, which is intuitive since O atoms are expected to be consumed by etching the carbon walls. In the case of Figs. 1 and 2 measured in pure Cl_2 plasmas, this demonstrates that carbon coatings prevent the generation of O atoms in the plasma. As a matter of fact, silicon etching products containing O atoms are detected by mass spectrometry during silicon etching in the SiOCl_x -coated reactor [Fig. 1(a)] but not in the carbon-coated reactor [Fig. 1(b)].

More generally, in a gas mixture containing O_2 gas we expect that the O atom density will be lower in a carbon-coated reactor than in a SiOCl_x -coated reactor because O atoms will etch the carbon coating at a high rate, which will load their density. We will come back to this important point later.

Finally, regarding the chemical nature of the ions impinging on the wafer, Fig. 2 shows that it is modified by the carbon coating, but that the effect remains relatively small at low pressure (this is in good agreement with the observations of Xu *et al.*³⁰ who reported that the plasma sensitivity to the reactor wall coating increases with the pressure in the reactor). Furthermore, the ion flux measurements show that for all the plasma and process conditions studied, the value of the total ion flux is only slightly lowered (by 15% maximum) in the carbon-coated reactors. Hence, we can conclude that the reactive halogen atom densities are lowered in the carbon-coated reactor while the ion flux remains roughly unchanged. Therefore *the carbon-coating strategy provides plasma conditions with higher ion-to-neutral flux ratio than other conditioning strategies*, and as discussed below, this can be in some cases an advantage for obtaining highly anisotropic etching profiles. Feature profile simulation shows that the ion-to-neutral ratio is of primary importance for profile control of silicon structure,^{31,32} and more generally of any materials whose etching mechanism is strongly ion enhanced. In particular, increasing the ion-to-neutral flux ratio allows a better anisotropy to be achieved, at the price of a reduced etch rate.³³

The other impact of carbon walls on the plasma chemistry is a lower O atom density (for given plasma operating conditions with or without oxygen in the discharge) and the presence of C-containing radicals in the plasma. These latter points may have a strong impact on the etching process selectivity toward gate oxides.

In the following sections we have investigated the impact of using a carbon-coated reactor on the silicon etching rate,

TABLE II. Etch rate (ER) (in nm/min) of doped polysilicon and selectivity (S) towards SiO₂ gate oxide of state-of-the-art silicon gate etching recipe for different initial reactor wall conditions. "inf" for infinite selectivity means etching rate of gate oxide cannot be evaluated within measurement uncertainty.

Process step	SiOCl _x -coated reactor	Carbon-coated reactor
Main etch	ER=140	ER=75
Soft-landing	ER=240 S=inf	ER=120 S=120
Overetch	ER=90 S=inf	ER=90 S=440

on the process selectivity toward gate oxides and high-*k* dielectrics (and toward silicon substrate during high-*k* etching), on the etching anisotropy in the cases of silicon and metal gate etching processes, and finally on metallic contamination of the wafer.

B. Impact of carbon-coated walls on silicon etch rate

Sub-100-nm gate patterning requires a multistep etching process to ensure a good critical dimension control across large-size wafers and selectivity toward gate oxide.³⁴ The state-of-the-art recipe that we have used as a base line in the DPS reactor has demonstrated its capability to pattern 10 nm polysilicon gates over a 1.2 nm thick SiO₂ gate oxide.³⁵ As discussed previously, this process has been optimized in a SiOCl_x-seasoned reactor. Etch rates of polysilicon during the three steps of the process (main etching soft-landing, and overetching, plasmas 3, 4, and 5, respectively, in Table I) are measured by *in situ* reflectometry at 505 nm on full-sheet poly-Si (150 nm)/SiO₂(10 nm) wafers. Table II compares results obtained in the typical strategy (SiOCl_x-passivated reactor) and in the carbon-coating strategy. It shows that etch rates are strongly reduced in a carbon-coated reactor. According to the previous discussion, this is attributed to the lower halogen atom densities (Cl and Br) in the carbon-coated reactor [since the flux of C-containing ions is small at low pressure (Fig. 2), it is not expected to impact the etch rate]. Regarding the throughput of a process, this is not an advantage for silicon gate etching, but we will see in Sec. III D that the lower density of halogen atoms is helpful in patterning anisotropic poly-Si/metal gate stacks.

C. Impact of carbon-coated walls on selectivity toward the gate dielectric

Two different gate stacks have been used to study the selectivity toward thin SiO₂ gate oxides or high-*k* HfO₂ gate dielectrics. In the case of a polysilicon gate on an ultrathin SiO₂ gate oxide, a main etching (ME) step (plasma 3 in Table I) is first used to pattern most of the gate until the soft-landing (SL) step (plasma 4 in Table I) is launched when the thickness of the remaining polysilicon layer is about 10 nm. Then, as soon as the gate oxide is reached, an overetch (OE) step (plasma 5 in Table I) is performed to remove silicon residues in dense lines. The gate oxide is thus

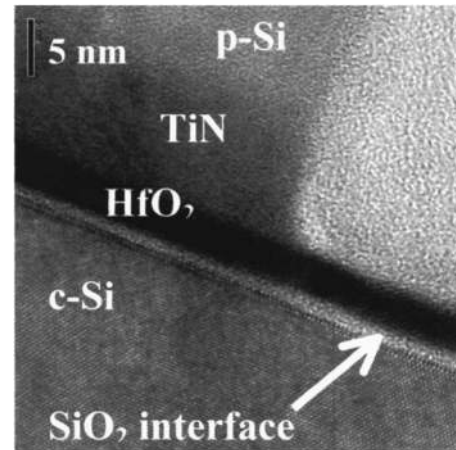


FIG. 3. High-resolution TEM cross section of the foot of poly-Si/TiN/HfO₂ gate stack after metal etching performed in the carbon-coated reactor.

exposed to the plasma only during the SL and OE steps. The etch rates of blanket 10 nm thick thermal SiO₂ wafers during these process steps have been measured by *ex situ* spectroscopic ellipsometry (KLA Tencor/Prometrix UV-1280SE). The results obtained in both typical SiOCl and carbon-coating strategies are shown in Table II. In the SiOCl_x-coated reactor, selectivities of the SL and OE steps are so high that they cannot be measured accurately (infinite selectivity), which is expected since the etching process has been developed in this reactor wall condition. In the carbon-coated reactor, the selectivity toward the SiO₂ thermal gate oxide decreases as expected. As discussed before, this is attributed to a lower density of oxygen atoms in the plasma³⁶ and also to the presence of carbon in the gas phase (which is known to enhance the oxide etch rate).³⁷ However, the SiO₂ etch rate remains two orders of magnitude smaller than the silicon etch rate (selectivity of the OE step is 440) in the carbon-coated reactor, which is still appropriate for gate patterning on ultrathin gate oxides. As a matter of fact, previously published profiles of silicon gates on 1.2 nm thick gate oxide etched within carbon-coating strategy¹⁰ have demonstrated that the SiO₂ integrity is maintained.

In the case of high-*k* gate dielectric, it is predicted that the gate electrode material could be metal and not poly-Si. Indeed, even if from an electrical point of view, metal integration would be required after high-*k* material integration, there is so much practical difficulties at the poly-Si/high-*k* interface that metal gate and high-*k* dielectric are likely to be introduced at the same time.¹ Since Hf-based oxides are the only foreseen candidates for short-term integration, we have focused our studies on the selectivity between TiN and 3.5 nm thick HfO₂ gate dielectrics. Patterned wafers, whose stack is described above, have been etched in the carbon-coated reactor, and the process has been stopped after the TiN layer etching step. Figure 3 shows a high-resolution TEM cross section photograph of the foot of the gate etched in the carbon-coated reactor. It can be noticed that the 3.5 nm thick high-*k* dielectric has not been eroded by the HBr/Cl₂ chemistry needed to pattern the TiN metal gate (plasma 8 in

Table I). Since the TiN overetch time is about 50%, it is obvious that the TiN etching selectivity toward HfO_2 is excellent in the carbon-coated reactor. This is not surprising since HfO_2 dielectric cannot be etched without energetic ion bombardment in Cl_2 chemistry at room temperature, even if carbon is present in the plasma gas phase.³⁸

However, when etching the metal layer of the gate stack, the challenge is not only to get a high selectivity toward HfO_2 but also to minimize the silicon recess induced by the oxidation of the bulk silicon below the HfO_2 layer during the metal etching step. This plasma oxidation through the HfO_2 film results in the growth of a SiO_2 layer below the high- k layer, generating the well known “silicon recess”^{36,39,40} [silicon loss in the source and drain active regions of complementary metal-oxide semiconductor transistor⁴¹ during (or after) gate oxide etching]. Silicon recess is considered as a critical issue for the next device generations (especially when <10 nm thick silicon-on-insulator wafers are used). It should be underlined that even if the metal etching recipe is O_2 -free, oxygen atoms and ions are always present in the plasma gas phase because of oxide hard mask consumption, reactor wall erosion in the case of SiOCl_x -coated reactors, or air leakage through chamber joints.⁴² It therefore remains difficult to minimize the silicon bulk oxidation even in O_2 -free chemistries. However, as discussed before, the O atom density is loaded by the carbon walls, and we thus expect a good performance of the metal gate etching process in the carbon-coating strategy. This is evidenced in Fig. 3, which shows that plasma-induced c-Si substrate oxidation is negligible with the carbon-coated walls. More precisely Fig. 3 shows that the interfacial oxide has almost the same thickness below the gate and on the surface exposed to the plasma, demonstrating that the reoxidation of the silicon substrate in open area is small in this case. We do not have a high-resolution TEM picture of the same process in the SiOCl_x -coated reactor for comparison. However, it will be difficult for a process to provide better results than that shown in Fig. 3.

D. Impact of the carbon-coating strategy on the sidewall passivation layers and profile control

1. Silicon gate etching over thin SiO_2

Silicon etching profiles are typically controlled by the thickness and chemical nature of passivation layers formed on silicon sidewalls during the process.^{34,36} Etching chemistries are adjusted very carefully to ensure that passivation layers are both thin (thus preventing excessive tapering of the sidewalls) and of similar thicknesses in dense and isolated structures (to minimize the critical dimension microloading). We have shown before¹⁰ (based on scanning electron microscope pictures) that the etching anisotropy seems to be as good in a carbon-coated reactor than in a SiOCl_x -coated reactor. To confirm this trend, we have performed XPS chemical topography analyses of the gate sidewalls to determine the chemical composition of the passivation layers with both types of reactor wall coatings. We use crystalline silicon substrates, on top of which is deposited a

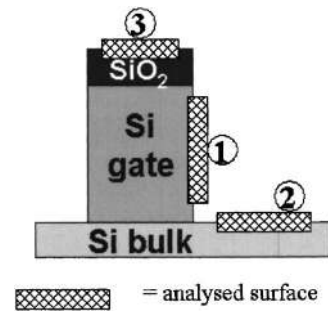


FIG. 4. Schematic of an oxide-masked silicon line showing the three regions analyzed by XPS with the chemical topography technique.

100 nm thick SiO_2 hard mask. The special pattern for chemical topography analysis (containing regular arrays of lines, blanket substrate, and unpatterned mask material) is obtained by optical lithography at a 248 nm exposure wavelength. To get reliable information on the influence of carbon-coating strategy on the etching process, we first performed hard mask patterning and resist stripping on both wafers and then removed native oxide on top of silicon with a short energetic CF_4 -based breakthrough step. The wafer is then removed from the reactor and kept under vacuum while the reactor walls are dry-cleaned and conditioned (with either the SiOCl_x layer or the carbon coating). The wafer then goes back into the etch reactor and the main etch step (plasma 3 in Table I) is carried out until sufficient thickness of silicon is etched to perform chemical topography analyses of the gate sidewalls. Figure 4 shows the locations of the three regions of the silicon gate that are analyzed by this technique: (1) the silicon passivation layer formed on the gate sidewall, (2) the Si wafer surface (open area), and (3) the SiO_2 hard mask surface. Table III gives the chemical composition of these three zones obtained after silicon gate etching in either a SiOCl_x -coated reactor or a carbon-coated reactor. First, we can notice that in carbon-coated reactor walls, the chlorine content in the reactive layers on Si and SiO_2 etched surfaces is less than the bromine content while the opposite trend is observed with SiOCl_x reactor wall coatings. This is in good agreement with the previous results stating that the Cl atoms are strongly loaded on the carbon reactor walls. The sidewall passivation layer chemical composition is calculated by removing the Si-Si bulk contribution originating from the silicon sidewall. In the carbon-coated reactor, its composition is $\text{SiO}_x\text{Cl}_y\text{Br}_z$ as in the typical SiOCl_x conditioning strategy, with a smaller Cl/Br ratio, a reduced O concentration, and a very small carbon content. So the most important result in Table III is that in the carbon-coating strategy, the passivation of the silicon gate sidewalls still relies on the oxidation of etch silicon by-products adsorbed on the feature sidewalls without significant carbon-based contributions. The passivation mechanism thus remains unchanged in a carbon-coated reactor.

As a result, in the carbon-coated reactor (as in the typical strategy) it is possible to tune the thickness of the silicon sidewall passivation layer (and thus the slope of the etching profile) by controlling the O_2 gas flow in the etching recipe.

TABLE III. Chemical composition of regions 1–3 of Fig. 4 measured by XPS (element concentration in at. %) after a HBr/Cl₂/O₂ main etch step performed in both SiOCl_x- and carbon-coated reactor.

Region	Reactor walls	Si–Si	Si	O	Cl	Br	C
1: Sidewall	SiOCl _x	...	27	34	30	9	0
	Carbon	...	24	18	32	23	3
2: Si	SiOCl _x	73.5	5	1.5	10	10	0
	Carbon	72	5	1	5	16	1
3: SiO ₂	SiOCl _x	...	37	48	10	5	0
	Carbon	...	37	55.5	2.5	3.5	1.5

However, at constant O₂ flow, TEM pictures below show that thicker SiOCl_x layers are observed in the SiOCl_x-covered reactor walls, which is attributed to a higher O atom density (passivation mechanism is O limited³⁴). Therefore, a higher O₂ flow will be required to get the same passivation layer thickness in the carbon-coated reactor than in the SiOCl_x-coated reactor.

2. Metal gate etching over HfO₂

In this section, advanced p-Si/TiN/HfO₂ gate stacks described in Sec. II are patterned in the carbon-coated and SiOCl_x-coated reactors. The hard mask is first opened in a fluorocarbon-based plasma, the resist stripping is then performed in an O₂ plasma, the wafer is removed, and the reactor is finally conditioned as desired (SiOCl_x or carbon coating) before the etching process. The standard process developed in SiOCl_x-passivated reactors consists in etching each layer selectively with respect to the underlayer. Thus, the silicon top part of the gate is etched using the SiO₂ hard mask with a state-of-the-art process, i.e., plasmas 3–5 in Table I (O₂ is suppressed from soft-landing and overetch steps to prevent the oxidation of the TiN surface). A short physical sputtering step (plasma 6 in Table I) is then performed to remove the TiO_x native oxide layer from the metal surface, and the 10 nm thick TiN film is then etched in HBr/Cl₂ chemistry (plasma 7 in Table I).

In the carbon-coated reactor the poly-Si top part of the gate has been etched with exactly the same process. However, it is necessary to tune the metal etching recipe (optimized in the SiOCl_x reactor) in order to get a good TiN etching anisotropy in the carbon-coated reactor. Indeed, it has been shown that TiN etching in HBr-rich chemistries generates a foot at the bottom of the metal layer, while etching in Cl₂-rich chemistry produces strongly undercut profiles.⁴³ It was thus possible to obtain anisotropic TiN profiles in the carbon-coated reactor by simply increasing the Cl₂/HBr ratio in the gas mixture. The final etching process is given as plasma 8 in Table I. Figure 5 shows TEM cross sections of TiN metal gates etched in both conditioning strategies. In both cases, TiN is etched anisotropically and selectively toward the HfO₂ gate dielectric [see Fig. 3, which is a zoom of the foot of the gate shown in Fig. 5(a)]. However, Fig. 5 shows that on the wafer etched in a SiOCl_x-coated

reactor, a strong notch is present at the bottom of the silicon part of the gate (i.e., at the Si/TiN interface position). This notch is a typical issue encountered when etching poly-Si/metal gates: O₂ must be removed from SL and OE silicon etching steps to avoid formation of etching-resistant TiO₂ layers, and as a result the foot of the silicon gate is not passivated. This part of the gate can then be etched laterally by halogen atoms during metal etching, thus generating the notch⁴⁴ at the poly/TiN interface. This phenomenon is not observed for the gate etched in a carbon-coated reactor, thanks to the higher ion-to-neutral flux ratio provided by this strategy. In the carbon-coated reactor the density of reactive

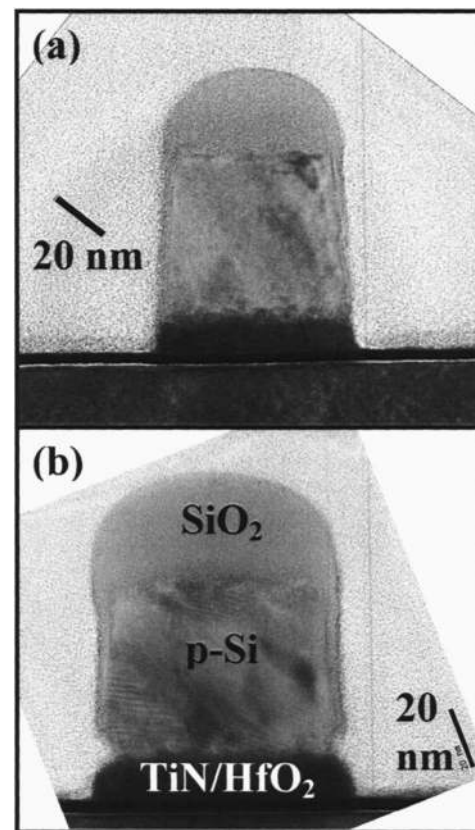


FIG. 5. High-resolution TEM cross sections of poly-Si/TiN/HfO₂ gate stack after metal etching, performed (a) in a carbon-coated reactor and (b) in a SiOCl_x-coated reactor.

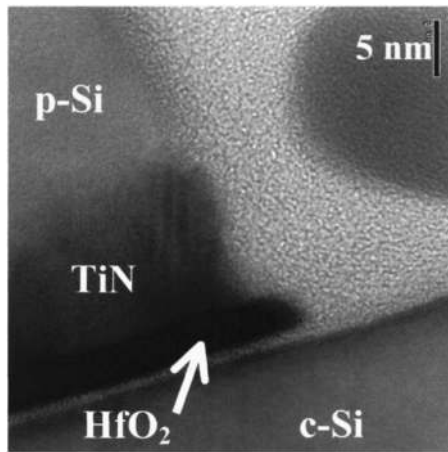


FIG. 6. Identical to Fig. 3 but after high- k dielectric etching.

radicals is very small and the etching is strongly ion assisted (i.e., mainly driven by Cl-containing ions). Therefore, there is almost no isotropic etching component in the carbon-coated reactor and notching is prevented. This result suggests that highly anisotropic features can be achieved almost without sidewall passivation in a carbon-coated reactor, which is a significant benefit when nanometric-scale gates must be patterned.³⁵

Figure 5 also shows that the silicon sidewall passivation layers (mainly formed during the silicon ME step) are thinner in the carbon-coated reactor than in the SiOCl_x -passivated reactor. This is obviously a consequence of the O atom consumption by carbon walls.

Hence, the carbon-coating strategy demonstrates a good potential for the successful patterning of metal gate stacks since the silicon sidewall passivation mechanism remains unchanged compared to standard processes (although thinner passivation layers are generated) and since notching at the silicon/metal interface can be eliminated. It should be highlighted that in the SiOCl_x -coated reactor the metal gate etching process can also be tuned to prevent the notch by modifying the plasma conditions to etch the TiN layer more rapidly (thus minimizing the lateral etching that generates the notch).⁴³

3. High- k dielectric etching

It has been reported in several papers that HfO_2 can be etched either at high temperature (350 °C) in Cl_2/CO plasmas³⁸ or at room temperature in BCl_3 -based plasmas.⁴⁵ In this work we use pure BCl_3 plasma (plasma 9 in Table I) to etch the HfO_2 film in the carbon-coated reactor after poly-Si and metal gate patterning (the etching up to the high- k dielectric layer is described previously). Figure 6 displays the high-resolution TEM picture of the bottom of the gate, showing that the HfO_2 profile exhibits a small foot. However, corroboration with the XPS analysis shows that the HfO_2 layer has been etched properly since no Hf residues is seen on the surface. The important result is that the process selectivity toward the silicon substrate is excellent and thus the silicon recess is almost negligible. The $\text{HfO}_2/\text{SiO}_2$ selec-

tivity is extremely high in the carbon-coated reactor because a B_xCl_y polymer grows selectively on the SiO_2 underlayer under these conditions (this is evidenced by the XPS analysis discussed in a forthcoming paper, and this polymer has also been observed by Kitagawa *et al.*⁴⁶). Furthermore, since the oxidation of silicon through HfO_2 during the TiN etching step is negligible in this case (see Sec. III C), the silicon recess after the full patterning of the gate stack in the carbon-coated reactor is only about two atomic plans (Fig. 6), which is remarkable.

We have observed that the B_xCl_y polymer formation rate on the SiO_2 surface is strongly enhanced in the carbon-coated reactor with respect to other reactor conditions. However, it remains difficult to conclude on the exact mechanisms. On the one hand, the higher deposition rate observed in the carbon-coated reactor can be attributed to a change in the plasma chemistry, which would enhance B_xCl_y polymerization in the carbon-coating strategy (for example, H atoms released from the carbon coating should promote B_xCl_y polymer deposition according to a recent work from Wang and Donnelly⁴⁷). On the other hand, the deposition rate of the B_xCl_y polymer is strongly ion energy dependent: a change in reactor wall conditions can impact the energy distribution function of the ions impinging on the wafer. It is beyond the scope of this article to discuss these selectivity mechanisms in more detail. However, our results allow us to conclude that HfO_2 etching can be achieved almost without silicon recess in the carbon-coating strategy (in agreement with the discussion of Sec. III C).

4. Remark for future etching processes with amorphous carbon hard mask

One final point needs to be discussed in this section. Since few years, amorphous carbon (α -C) hard masks⁴⁶ have been introduced to compensate the low etching resistance of a 193 nm photoresist when exposed to aggressive plasmas. The carbon layer acts both as an antireflective coating for the lithography step and as a hard mask for the gate etching process (silicon or metal gate). Furthermore, the introduction of these masks is accompanied by the development of alternative silicon etching processes using fluorine- and fluorocarbon-based chemistries (which improves the profile differences between n^+ - and p^+ -doped polysilicon gates). The trend in manufacturing is therefore to introduce α -C hard masks and to etch poly-Si gates in fluorocarbon-containing plasmas. Then, using carbon-coated reactor walls for gate stack etching seems well adapted and appears as an "all carbon" solution. Indeed, integration scheme with an α -C mask does not require a resist stripping step since resist and dielectric capping are removed during the etch process. It is therefore possible to perform the etching of the full stack while keeping the benefit of the carbon-coating strategy throughout the process.

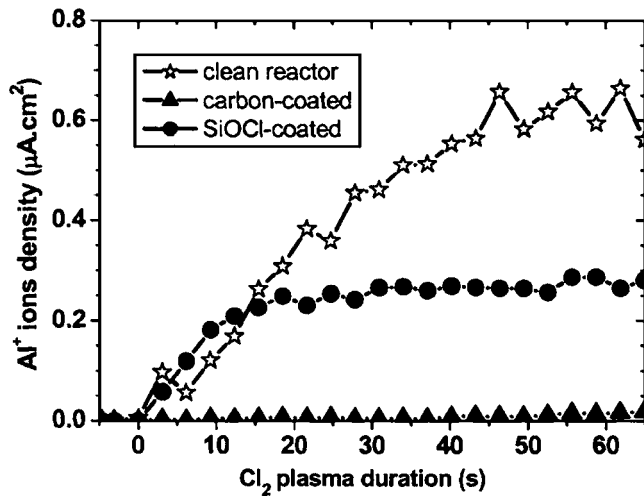


FIG. 7. Time evolution of Al^+ ion density during blanket silicon wafer etching in pure Cl_2 plasma (100 SCCM at 5 mTorr, 300 W source, and 90 W bias powers) for different initial reactor wall conditions in the Lam reactor.

E. Impact of carbon-coated walls on-wafer metallic contamination

If the carbon-coating strategy is mainly introduced to protect the inner Al_2O_3 reactor walls from the F-based cleaning plasma, it can also protect the wafer from Al contamination during the etching process. Metallic contaminants of any type can indeed generate severe damage to the device. With the shrinkage of feature dimensions and the introduction of new potentially contaminating materials in the gate stack (such as Hf), ITRS requirements for metallic contamination are becoming very stringent ($<10^{10}$ at. cm^{-2}).¹

For example, shallow trench isolation (STI) are etched directly into the silicon wafer before deposition of ultrathin gate oxides and electrode stacks. STI etching is a complex Cl_2 -based process containing numerous steps. To illustrate the potential of the carbon-coating strategy to minimize or eliminate the metallic on-wafer contamination, we measure the relative Al^+ ion density during the etching of blanket silicon wafer in Cl_2 plasmas in the Lam reactor for different reactor wall conditions. Mass spectrometry has been used to measure the IED of Al^+ ions at of 27 a.m.u. (with an energy resolution of 0.1 eV) repeatedly every 2–3 s after the plasma has been switched on. At each time, the integral of the IED is proportional to the Al^+ ion density. Figure 7 shows the time variations of the Al^+ ion density in the plasma during silicon etching in the clean reactor, in the carbon-coated reactor, and in the SiOCl_x -coated reactor. When the etching is performed in a clean reactor, the anodized aluminum reactor walls are directly exposed to the chlorine plasma which tend to induce an erosion by forming volatile AlCl_x products, eventually resulting in the formation of Al^+ ions (by electron impact dissociation and ionization reactions). Figure 7 shows that the Al^+ ion density increases as a function of time. This may be attributed to a modification of the reactor walls since the Al_2O_3 reactor walls are initially coated by an AlF_x layer in the so-called clean reactor.

In contrast, with the carbon-coating strategy, the entire reactor is protected by a carbon layer and no Al^+ is detected. After about 1 min of plasma, some aluminum ions begin to enter the spectrometer but at a very low flux. This demonstrates that the carbon coating is able to protect all parts of the reactor walls, thus preventing metallic contamination of the wafer.

Surprisingly, Fig. 7 shows that with SiOCl_x -passivated reactor walls, Al^+ ions are detected immediately upon plasma ignition and that it takes about 20 s for Al^+ density to stabilize. This is attributed to the chemical sputtering of the Al_2O_3 edge ring protecting the chuck of the Lam reactor.⁴⁸ Indeed, this ring is in close contact with the edge of the wafer and is thus subjected to the energetic ion bombardment (continuity of electric field forces the sheath facing the wafer to go over the edge). The erosion of the ring occurs during the etching of the silicon substrate in the Cl_2 plasma, which generates part of the Al^+ signal detected, but also during the passivation of the reactor performed by etching a silicon wafer in Cl_2/O_2 chemistry. Thus, aluminum is present in the gas phase during the SiOCl_x conditioning step and is likely to be incorporated in the SiOCl_x layer coated on the reactor walls. These Al atoms are then released in the gas phase and ionized during silicon etching in Cl_2 plasma. This is not observed in the carbon-coating strategy since even the edge ring is covered by the carbon film (no bias power is applied during carbon deposition). Similarly, Al atoms and AlCl radicals are detected in pure Cl_2 plasmas during silicon etching by broadband UV absorption spectroscopy in the clean and SiOCl_x -passivated reactor, whereas they are not in the carbon-coated reactor. Typically, we have measured an Al atom density of about 10^9 cm^{-3} and an AlCl density of 10^{10} cm^{-3} during high-pressure Cl_2 etching of silicon in the SiOCl_x -coated reactor.

On-wafer metallic contamination measurement is performed by ICP mass spectrometry analysis⁴⁹ after etching in the DPS reactor. The atomic Al density at the surface of a silicon wafer has been measured after etching by either SF_6 or HBr plasmas in clean reactor wall conditions. In both cases the etching condition are 100 SCCM (SCCM denotes cubic centimeter per minute at STP) of gas at 60 mTorr with 250 W source power and 120 W bias power for 10 s. Before etching, the reference Al contamination of the wafers is about 5×10^{10} cm^{-2} . After etching with the SF_6 plasma it rises to 2.6×10^{13} cm^{-2} , while after etching with the HBr plasma it is about 2×10^{12} cm^{-2} . We also measured the Al contamination after silicon etching by the HBr plasma in a SiOCl_x -coated reactor: it is about 3.4×10^{12} cm^{-2} , that is to say, comparable to the etching in the clean reactor. Hence, the Al contamination of the wafer rises by two to three orders of magnitude after a short HBr or SF_6 etching process operated in a clean or SiOCl_x -coated reactor. In contrast, when the same SF_6 process is run in a carbon-coated reactor for 10 s, the Al contamination of the wafer is only 5.3×10^{10} cm^{-2} , that is to say, identical to the reference before plasma exposure. Therefore, the carbon-coating strategy appears to reduce metallic contamination by at least two orders

of magnitude when compared to other reactor wall conditions (and, as a matter of fact, to completely prevent contamination).

F. Deposits formed on the carbon wall and reactor wall cleaning strategy

As discussed above, the carbon-coating strategy has demonstrated very good patterning capabilities for advanced gate stack etching applications. In particular, it has been shown that carbon-coated walls exhibit significant advantages compared to other types of wall materials (SiOCl_x coatings or Al_2O_3) because they load the gas phase density of O and Cl atoms and provide a higher ion-to-neutral flux ratio to the wafer. Furthermore, the carbon coating protects the Al_2O_3 reactor walls from exposure to F atoms, thus eliminating metallic contamination of the wafer and preventing AlF_x particle formation and flaking off (which should result in a high MTBC). For the manufacturing perspectives of the carbon-coating strategy, it remains important to analyze the time cost of this strategy (including coating deposition and cleaning after the process). This is clearly correlated to the thickness (and plasma etch resistance) of the coating that is required to protect the reactor walls. More precisely, to get all the benefits from the carbon-coating strategy it is necessary to analyze the three following points:

1. The initial carbon coating is deposited on *all* the surfaces exposed to the plasma (including on the reactor roof below the rf coil where the ion energy is high due to the capacitive coupling between the coil and the plasma).
2. The initial carbon coating is thick (and plasma resistant) enough to remain on all parts of the reactor walls during the whole etching process, which may comprise many steps in different plasma chemistries (this is not obvious since we have evidenced before that the carbon coating is etched by HBr, Cl_2 , and O_2 containing plasmas).
3. At least some part of the carbon coating remains exposed to the plasma to consume O and Cl atoms. If it is not the case, that is to say, for example, if the carbon wall gets entirely covered by a SiOCl_x layer, then the etching property will be again comparable to a SiOCl_x coating. This is not really an issue, but this point must be investigated to determine the best way of cleaning the reactor walls after an etching process in a carbon-coated reactor: in the case of a layered coating (SiOCl_x on top of carbon) a two step cleaning process such as SF_6 followed by O_2 will be required, although a composite coating may be cleaned in a single step plasma etch process.¹⁴

In this section, we will investigate these different points one by one for the typical case of silicon etching in $\text{HBr}/\text{Cl}_2/\text{O}_2$ chemistry, and starting with our typical carbon-coating layer (approximately 25 nm thick on the floating parts of the reactor walls).

The amount of silicon deposited on the carbon-coated reactor walls and the amount of carbon remaining on the reactor walls after the silicon etching process have been analyzed by a technique developed by Kogelschatz *et al.*⁹ (in the same reactor). The reactor wall coating to be analyzed is etched by

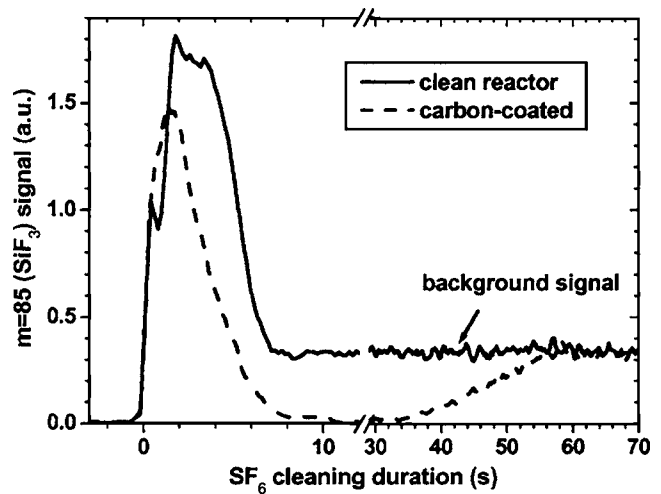


Fig. 8. Time evolution of the RGA signal intensity at mass 85 amu (SiF_3^+ originating from SiF_4) during SF_6 reactor cleaning after silicon etching in $\text{HBr}/\text{Cl}_2/\text{O}_2$ plasma for 60 s with two different initial reactor wall conditions. Note the break and scale change on abscissa axes.

an appropriate plasma, and mass spectrometry is used to monitor the time variations of the density of an etch product coming from the reactor wall deposit. For example, the SiOCl_x layer coated on the reactor walls after silicon etching by a $\text{HBr}/\text{Cl}_2/\text{O}_2$ plasma can be etched by a SF_6 plasma (after removing the wafer from the reactor). During this waferless reactor cleaning step, SiF_4 is the dominant etch product of the SiOCl_x layer, and the amount of silicon coated on the reactor walls can thus be quantified by monitoring the total amount of SiF_4 desorbing from the reactor wall during the layer removal. Mass spectrometry has been used in the RGA mode (using 70 eV electrons to ionize molecules in the mass spectrometer head) to monitor the time variations of the density of SiF_4 by following the SiF_3^+ signal intensity. It has been checked that using the SiF_3^+ or SiF_4^+ signal leads to the same result, but SiF_4 is detected with a better signal to noise ratio as SiF_3^+ than SiF_4^+ ions when 70 eV electrons are used.⁵⁰

For example, Fig. 8 shows the time variations of the SiF_4 density during the waferless SF_6 cleanings performed after etching a silicon wafer for 60 s in $\text{HBr}/\text{Cl}_2/\text{O}_2$ chemistry either in a clean reactor or in a carbon-coated reactor. It shows that in both cases the SiF_4 density increases upon SF_6 plasma ignition and then rapidly decreases when the SiOCl_x layer is cleared from the reactor walls. However, when the silicon etching process has been performed in a clean reactor, Fig. 8 shows that the SiF_4 density does not drop to zero (even at long times) but remains at a constant background level. This “residual” SiF_4 concentration in the reactor originates from the slow etching of the quartz roof of the reactor below the rf antennae,⁹ which is still producing SiF_4 once the SiOCl_x layer has been totally cleared. In contrast, with the carbon-coating, the SiF_4 density drops to zero once the SiOCl_x layer is cleared (at time $t=8$ s), which demonstrates that carbon coating still protects the roof of the reactor when SiOCl_x has been fully removed (and thus also the rest of the reactor body which, contrary to the roof, is not bombarded

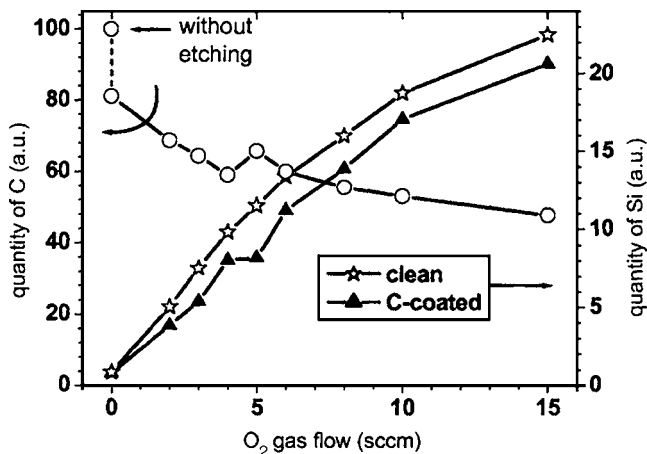


FIG. 9. Variation of the amount of silicon deposited on the reactor walls (\blacktriangle) and of the amount of carbon remaining on the reactor walls (\circ) after silicon etching processes in $\text{HBr}/\text{Cl}_2/\text{O}_2$ with various inlet O_2 flow rates in the carbon-coated reactor. Amount of silicon deposited on the reactor walls when the same process is started in a clean reactor (\star).

by energetic ions). However, after 30 s, the SiF_4 signal rises again and eventually increases up to the background level as the carbon layer is progressively etched away from the roof by the SF_6 plasma.

Therefore, we can already conclude that the carbon coating protects very well all the different parts of the reactor walls (including the roof below the rf coil) both before and after the silicon etching process. These experiments clarify points (1) and (2) mentioned above.

However, in this example the silicon etching process was performed at low O_2 flow (3 SCCM) in a regime where the SiOCl_x deposition rate on the reactor walls is low and where the removal rate of the carbon coating by the oxygen contained in the discharge is small. Although these conditions are typically those of state-of-the-art processes, we have also investigated the impact of a higher O_2 dilution in the $\text{HBr}/\text{Cl}_2/\text{O}_2$ plasma on the amount of SiOCl_x coated on the reactor walls and the amount of carbon remaining on the reactor walls after the process. To investigate the impact of this higher O_2 flow, the reactor walls are cleaned in a two step process: a first SF_6 cleaning step is used as previously to remove the silicon from the reactor walls, and the amount of silicon deposited on the reactor walls is quantified by integrating the SiF_4 signal over time (same technique applied previously in Fig. 8). This first cleaning step is stopped immediately when the SiF_4 density drops to zero and is followed by a pure O_2 plasma, whose role is to remove the carbon from the reactor walls. During this second reactor cleaning step the total amount of carbon left on the reactor walls is quantified by integrating over time the density of CO etch products (determined by mass spectrometry) during the O_2 plasma. This two step cleaning procedure is indeed the best one to clean the reactor after running an etching process in a carbon-coated reactor. The results are exposed in Fig. 9, which shows that the amount of silicon coated on the reactor walls after the $\text{HBr}/\text{Cl}_2/\text{O}_2$ plasma increases with the increase in the O_2 flow rate in the etching recipe, which is

expected since the thickness of the SiOCl_x layer coated on the reactor walls increases with the O_2 flow.²⁵ However, Fig. 9 shows that at the same time, the amount of carbon remaining on the reactor walls after the process decreases when the O_2 flow increases. Since we expect no etching of the carbon coating through a thick SiOCl_x layer, this result suggests that the SiOCl_x deposition rate is not uniform, and that at low O_2 flow, a significant area of carbon remains exposed to the etching plasma, thus affecting its properties. Kogelschatz *et al.*⁹ have shown that SiOCl_x deposition is inhibited at the roof position below the rf coil because this region is bombarded by high energy ions. Therefore, the carbon-coated reactor roof will not get coated by a SiOCl_x layer unless a very high O_2 flow is used, while at the same time SiOCl_x deposition will take place (on top of the carbon coating) on the other parts of the reactor walls. Hence, when the O_2 flow increases, both the thickness of the SiOCl_x layer and its area will increase (explaining why the amount of silicon coated on the reactor wall increases in Fig. 9), but at the same time the etch rate of the carbon film on the reactor roof (that is, still exposed to O atoms) also increases, explaining why the amount of carbon left on the reactor wall decreases with the O_2 flow. Eventually, above a certain O_2 flow, SiOCl_x deposition rate becomes so high that it covers the entire reactor area (including the reactor roof) after the 60 s etching process. This transition takes place at 5–6 SCCM O_2 flow (it corresponds to the bump in the curves of Fig. 9), and it can be experimentally detected. An O_2 plasma cracked after silicon etching at high O_2 flow does not produce CO species (thus, no carbon is visible anywhere in the reactor) and if the SF_6 plasma is then performed, SiF_4 density drops to zero after SiOCl_x clearing, demonstrating that carbon layer is still present *under* the SiOCl_x deposit on the reactor roof. These results demonstrate the importance of the reactor roof region in controlling the plasma chemistry.

Finally, Fig. 9 also shows the amount of silicon deposited on the reactor walls after silicon etching in a *clean* reactor. This quantity is always higher than that in the carbon-coated reactor, which is attributed to a lower density of O atoms in the carbon-coated reactor. As a matter of fact, since the SiOCl_x deposition is nonuniform, it takes some time to entirely cover the carbon coating with SiOCl_x even at high O_2 flow (furthermore, when the SiOCl_x layer is still thin it is permeable to O atoms⁹ and carbon etching may proceed through it at the early stage of the plasma). During that time, the carbon exposed to the plasma is consumed at a high rate (explaining the lower level of carbon remaining on the reactor walls at high O_2 flow) and the O atom density is loaded, resulting in a lower amount of silicon coated on the reactor walls.

In summary, we observe that an initial 25 nm thick carbon coating protects well the Al_2O_3 reactor walls from exposure to the plasma, whatever the O_2 dilution in the silicon etching process is: at low O_2 flow the carbon is slowly etched, while at high O_2 flow a SiOCl_x layer eventually coats and protects the carbon film. In a manufacturing environment, the time during which the plasma etch reactor is coated by the carbon

film has to be minimized. This can be easily achieved by using appropriate plasma conditions and chemistries (such as CH₄, or a mixture of fluorocarbon and H₂). Concerning the advantage of carbon coatings on the etch process reproducibility, MTBC, and reactor wall lifetimes, the introduction of this reactor conditioning step in the process flow should not be an issue. Furthermore, since we observe that plasma processes tend to deposit SiOCl_x layers on top of the carbon coating, we have demonstrated that after an etching process the plasma reactor can be easily cleaned in a two step process: a short SF₆ step to remove the silicon-based etch products followed by a pure O₂ plasma to remove the carbon still protecting the reactor walls.

IV. SUMMARY AND CONCLUSIONS

Carbon-coating strategy consists in adding a reactor conditioning step, which deposits a carbon-rich layer on the inner part of the plasma reactor, to the typical strategy based on dry-cleaning the reactor between each wafer processed. It has been originally introduced to improve process reproducibility while at the same time protecting reactor walls from aggressive F-based cleaning plasmas, thus preventing formation of nonvolatile fluoride residues and increasing mean time between reactor wet cleans. We demonstrate that the entire reactor (including the roof below the rf antennae) is still coated with carbon after typical halogen-based processes so that the wafer metallic contamination is drastically reduced. In the case of highly polymerizing chemistry (such as STI etching or fluorocarbon-based processes) the impact of carbon-coated reactor walls on process performances is expected to be small. On the other hand, in the most typical "less polymerizing" front-end processes, performing advanced gate stack etching in a carbon-coated reactor influences gas phase chemistry as follows. Firstly, the reactive neutral density is reduced but the ion flux impinging the wafer surface remains roughly unchanged compared to a typical conditioning strategy, leading to an increase of the ion-to-neutral ratio. Our experiments show that this change in the ion/neutral synergy induces a decrease in etch rates but makes easier profile control of new materials introduced in the gate stack (whose etching is strongly ion assisted). Secondly, oxygen atom density is strongly loaded by the carbon-coated surfaces. During the etching of the polysilicon gate, this allows us to minimize the thickness of passivation layers (thus improving profile control) without generating undercutting or notching phenomena. In addition, the process selectivity toward ultrathin gate oxides seems to be only slightly impacted. Furthermore, a combination of the low silicon re-oxidation during gate patterning with the good selectivity of high-*k* dielectric etching chemistry toward the substrate leads to a very low silicon recess. Implementation of the carbon-coating strategy in manufacturing seems potentially interesting. Using the carbon-coating strategy, we have been able to pattern state-of-the-art metal gate stacks in a sole plasma reactor with a very good long-term reproducibility.

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