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# Infrastructures for Education and Research: from National Initiatives to global operations

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## **Abstract :**

Infrastructures to provide access to custom integrated hardware manufacturing facilities are important because they allow Students and Researchers to access professional facilities at a reasonable cost, and they allow Companies to access small volume production, otherwise difficult to obtain directly from manufacturers. In the late 70s/early 80s, pioneering integrated circuits Multi-Chip Projects / Multi-Project Wafers initiatives have been launched in Europe, Asia, and North America. Some of these initiatives work together and today a worldwide cooperation has been established by the most experienced. The paper review these initiatives and the motivations for a global cooperation scheme.

**Keywords:** integrated circuits, infrastructures, multi-projects wafers.

## **1. The need for infrastructures**

Infrastructures to provide access to custom integrated hardware manufacturing facilities are important for several reasons:

- they allow Students and Researchers to access professional facilities at reasonable cost,
- they allow Companies to access small volume production, otherwise difficult to obtain directly from manufacturers.

The needs of Universities, Research Laboratories and Companies can be summarized as follows:

\* Universities need to have access to technology for teaching their students. Those students will be in the industry. Therefore they have to be trained at least on the actual state of the art technology processes.

\* Research Laboratories usually need to have high performance technologies to validate new concepts.

The quality of the research results depends mostly on the quality of the technologies. Accessing to up to date technologies is a necessity.

\* Industrial users also need to access to the state of the art of the offered technologies. This is vital for industrial users. The development of a product is usually long (more than 1 or 2 years). It is necessary that an industrial user has access to an up to date process, giving guaranty on product life.

Offering manufacturing Services has to be governed by the following basic principles:

- industrial quality process lines should be used (University process lines cannot offer a stable yield),
- design kits to link CAD and MPC/MPW facilities should be offered to ease the design.

## **2. Pioneering efforts in Europe**

A few countries have been pioneers in setting up such a kind of infrastructures. In Europe, France has been a pioneering country in this type of infrastructure since chip fabrication for

Universities had already been started in 1981 by CMP.

In Germany, The Institute of Microelectronic Systems at the Technische Hochschule Darmstadt offered multi-chip services for educational and research purposes for a long time. Fabrication was done at ITT – International Semiconductor Company in Freiburg. Also, integrated circuit manufacturing was supported by the Federal Ministry for Research and Technology (BMFT), in the E.I.S (Entwurf Integrierter Schaltkreise) project framework from 1983 to 1987.

In Scandinavia, NORCHIP was a service which started in 1981, to offer low cost prototyping of CMOS IC's in Sandinavian countries (Denmark, Finland, Norway, Sweden). NORCHIP has been later the name of a service offered to universities in Scandinavia by Nordic VLSI located in Trondheim, Norway.

In the United Kingdom, as soon as 1978 "Central Fabrication Facilities" had been established: silicon processing at the Universities of Edinburgh and Southampton, Ion Beam Processing at the University of Surrey, III-V components at the University of Sheffield, lithography at the Rutherford Appleton Laboratory. SERC produced its first circuit in August 1981, the masks being made at RAL and the process on University lines.

In Belgium, the fabrication line of the Université Catholique de Louvain (UCL) produced a limited number of MPCs for the 4 Belgian French-speaking universities within the association ARAMIS, as well as for foreign partners, for educational and research purposes. Also IMEC had a service operational between 1986 and 1992, for CMOS manufacturing.

Other European countries had more limited actions or initiatives or these came into action later, like Portugal at INESC, Ireland at NMRC, Switzerland at EPFL and CSEM, Spain at CNM, The Netherlands at DIMES.

Other countries had also set up initiatives, like Australia, Brazil, Canada, India, Japan, Korea, Malaysia, Taiwan, and the USA. Details on what happened in all these countries can be found in [COURTOIS 94].

## **3. First cooperative initiatives in Europe**

As a follow up of initial meetings of a group named "European Integrated Circuit Design", a meeting was held in Grenoble in 1986, and a protocol was signed. The protocol called for cooperation and mutual interdependency between individual programs. The signatories of the Protocol were B. COURTOIS as Director of CMP, H. HECKL as EIS project leader, K. WOELCKEN as EIS project leader, O. OLESEN as Chairman of Norchip, R. VAN OVERSTRAETEN as President of IMEC, P. DEWILDE as Chairman of the NELSIIS Group, R. CRAPPE

as President of ARAMIS, and E. MUNOZ MERINO as Coordinator PE-Micro E-CAICYT.

In 1988, the CEC launched a call for tenders to select a consortium to serve European universities for a number of services including multiproject chip fabrication. As a result, the EUROCHIP organization was set up including CMP from Grenoble France, the Technical University of Denmark (DTU), the German National Research Center for Computer Science (GMD), the Inter-University Center for Microelectronics (IMEC) in Belgium, and the Rutherford Appleton Laboratory (RAL) in the UK. Later, EUROCHIP issued a call for tenders towards vendors in 1989, and the service started in 1990. EUROCHIP, provided academic institutions with a number of services, including chip fabrication, and procurement of commercial CAD software, hardware, and testing equipment. More than 400 academic institutions from EU and EFTA countries participated in the action which was later opened to Central and Eastern Europe countries. More than 7,000 students have been trained in VLSI design during the first year of operation, and this figure increased to 10,000 for the second year. The high level of interest was also illustrated by the number of participants at the EUROCHIP Workshops held in Grenoble in 1991 and 1992 and next in Toledo (1993) and Dresden (1994). In order to help SMEs moving to microelectronics, the CEC launched in 1992 an initiative named: CHIPSHOP. CHIPSHOP was the service organization of the JESSI-SMI Project, whose goal was to address 15% of an entire target group of 25,000 enterprises in Europe. CHIPSHOP served SMEs for chip fabrication with a network of support and competence centers (SCCs). Thus, design assistance and support could be provided locally while prototype fabrication was performed on a European scale. During the 30 months of operation, more than 1,000 circuits were processed through CHIPSHOP. A summary of CHIPSHOP achievements can be found in [CHIPSHOP].

These European-level initiatives have been very successful at this time since they have pushed all the European countries to a uniform recognition of services. Unfortunately, the EC decided to stop them. A service called EUROPRACTICE is still in operation, but it suffers from bad decisions made at the structure level.

#### 4. Major infrastructure services today

There are 7 major infrastructure services today: CIC in Taiwan, CMC in Canada, CMP in France, ICC in China, IDEC in Korea, MOSIS in the USA and VDEC in Japan. They are briefly described below. Three of them, CMC, CMP and MOSIS have decided in 2002 to cooperate. It might happen that further cooperations will be developed later on. The following depicts these 7 services as per their inputs to the 2007 CMP Annual report.

##### **CIC**

National Chip Implementation Center (CIC) Project was initiated by the National Science Council in 1992. This project aims to pave the way for a national research and service center for IC/System design.

In 2007, the process technologies provided by CIC are listed below

- UMC 90nm MS CMOS,
- TSMC 0.13 $\mu$ m MS/RF CMOS,
- TSMC 0.13 $\mu$ m Logic/MS CMOS,

- TSMC 0.18 $\mu$ m 1P6M CMOS,
- TSMC 0.35 $\mu$ m 2P4M CMOS,
- TSMC 0.35 $\mu$ m SiGe BiCMOS,
- WIN 0.15 $\mu$ m PHEMT GaAs,
- TSMC 0.35 $\mu$ m CMOS MEMS Post Process,
- TSMC 0.18 $\mu$ m CMOS MEMS Post Process.

Totally, there were 1721 prototyped ICs being successfully fabricated in 2007. Up to now, CIC has provided MPC services for over eighty universities in Taiwan with 10,029 prototyped ICs including 9,044 ICs from the academics (universities and polytechnics) and 985 ICs from the research institutes as well as industrial sectors. Furthermore, CIC also develop Sip module and CMOS MEMS technologies for academia.

##### **CMC**

CMC Microsystems ([www.cmc.ca](http://www.cmc.ca)) provides national infrastructure for microsystems research and technology development.

As of 2007, CMC's services include:

- 65-nanometre CMOS (STMicroelectronics through CMP)
- 90-nanometre CMOS (STMicroelectronics through CMP)
- 0.13 $\mu$  CMOS (IBM through MOSIS)
- 0.18 $\mu$  CMOS (TSMC through MOSIS)
- 0.35 $\mu$  CMOS (TSMC through MOSIS)
- 0.8 $\mu$  CMOS in three process flavors: high-voltage--up to 300V, mid-voltage range-- $\pm$ 20V, and standard-voltage--2.7V to 5.5V (DALSA Semiconductor).
- 2.5 GHz Bipolar linear array (Gennum Corporation)
- PolyMUMPs surface micromachining process (through partnership with CMP and MEMSCAP)
- MetalMUMPs (through partnership with CMP and MEMSCAP)
- Micragem SOI-based micromachining process (Micalyne Generalized MEMS process)
- Protolyne for semi-custom microfluidics devices (Micalyne)
- Photonics/optoelectronics: InP, GaAs, EPI-only InP/GaAs, Silica/Si and Silicon-on-Insulator based technologies (through Canadian Photonics Fabrication Centre)
- On an exploratory basis: Microfluidic process with metallization (through Micronit)

A total of 378 designs were fabricated in 2007 using the technologies listed above.

##### **CMP**

Since 1981, several periods may be distinguished at CMP:

##### Development at CMP

Several periods may be distinguished.

- 1981–1982 : launching CMP with NMOS
- 1983–1984 : development of NMOS, launching CMOS
- 1984–1986 : development of CMOS
- 1987–1989 : abandon NMOS, increase the frequency of CMOS runs
- 1990–1994 : launching Bipolar, BiCMOS, GaAs MESFET, GaAs HEMT, advanced CMOS (.5  $\mu$  TLM)
- 1995–1997 : launching CMOS and GaAs compatible MEMS, DOEs, deep-submicron CMOS (.25 $\mu$  6LM)
- 1998 : launching silicon surface micromachining, abandon MESFET GaAs
- 1999 : launching SiGe, deep submicron CMOS (.18 $\mu$  6LM), SOI/SOS CMOS (.5 $\mu$ )
- 2000 : launching SiGe BiCMOS (.35 $\mu$  5LM)
- 2001 : launching very deep submicron CMOS (.12 $\mu$ )

	6LM)
2002	: launching Inp HBT process
2003	: launching 0.35 $\mu$ CMOS-Opto
2004	: launching very deep submicron CMOS (90nm, 7LM), HBT SiGe:C BiCMOS 0.25 $\mu$
2006	: launching CMOS 65nm (7LM)
2008	: launching CMOS 45nm

#### Processes available

Presently the processes available for ICs and MEMS manufacturing are depicted in Table 1.

Austriamicrosystems	0.35 $\mu$ CMOS C35B4C3
	0.35 $\mu$ CMOS C35B4M3
	0.35 $\mu$ CMOS-Opto C35B4O1
	0.35 $\mu$ CMOS Flash C35B4E3
	0.35 $\mu$ SiGe BiCMOS S35D4M5
	0.35 $\mu$ HV-CMOS H35B4D3
STMicroelectronics	45nm CMOS CMOS045
	65nm SOI
	65nm CMOS CMOS065
	90nm CMOS CMOS090
	0.12 $\mu$ CMOS HCMOS9GP
	0.12 $\mu$ SOI
	0.25 $\mu$ SiGe:C BiCMOS7RF
OMMIC	0.2 $\mu$ HEMT GaAs ED02AH
	0.2 $\mu$ HEMT GaAs ED02AH
	Bulk Micromachining
MEMSCAP	PolyMUMPs
	SOI MUMPs
	Metal MUMPs

TABLE 1: IC AND MEMS PROCESSES AVAILABLE

#### ICs design kits and CAD software

Design kits and libraries are distributed by CMP for most of the processes and most commonly used CAD tools. CMP sometimes develop design kits, in cooperation with the manufacturers and the CAD vendors. CMP also offers special CAD software conditions from a few CAD vendors. As a focal point, CMP also distributes information on configuration files, converters, etc. About 40 design kits are available for each process and the main CAD tools.

#### Other services

Packaging and testing services are also offered. Various types of packages are supported, including DIL, SOIC, CQFP, JLCC, PGA, etc. Test of prototypes is usually done by the final user. On request, especially for low volume production, CMP may take over testing together with manufacturing.

#### Key figures

Since 1981, CMP has served more than 1000 Institutions from 66 countries in various processes. Support to Industry started in 1993 for small volume production. CMP has been ISO 9002-1994 certified from 2000 to 2003. CMP is working on the certification ISO 9002-2000.

#### Recent developments

Recent developments have been the move to very deep submicron processes: 120 nm CMOS, 90 nm CMOS, 65 nm CMOS and 65 nm SOI, 45nm CMOS, .35  $\mu$  HBT SiGe

BiCMOS, .25  $\mu$  SiGe:C HTB BiCMOS from STMicroelectronics and the exploration of new MEMS fabrication offerings.

#### The move to very deep submicron processes.

CMP introduced 120 nm CMOS as early as 2001. A total of 175 circuits were fabricated from 2001 to June 2007. CMP introduced 90 nm CMOS in 2004 and nearly 100 circuits have been fabricated up to now. Finally 65nm CMOS was launched in 2006 and a ten of circuits have been fabricated already. This means a total of nearly 300 circuits coming from about 50 Research Laboratories and Industrial Companies. These processes have been very well received. Let's detail what happened with the CMOS 90 nm. The 90nm CMOS has been announced in 2004, first DRMs and design kits have been shipped to designers in 2004. The list of Institutions who have used the 90nm CMOS to date is depicted in Table 2. One can notice a number of top level Universities in Europe and USA mostly. All Canadian Universities are using the 90nm CMOS process. The move to 65nm has started. The 65nm CMOS has been announced in 2006. The Table 3 depicts the list of Institutions who have received the DRMs and design kits up to now. Again there are many top level Universities in Europe and in USA who are moving to 65nm CMOS.

CANADA	:	10
DENMARK	:	1
FINLAND	:	1
FRANCE	:	2
GERMANY	:	1
ITALY	:	3
NORWAY	:	3
SPAIN	:	1
SWEDEN	:	1
SWITZERLAND	:	2
USA	:	9
<b>TOTAL: 34 Institutions from 11 countries</b>		

TABLE 2: INSTITUTIONS HAVING SUBMITTED CIRCUITS 90NM CMOS

AUSTRALIA	:	1
BELGIUM	:	2
BRAZIL	:	2
CANADA	:	13
DENMARK	:	2
FINLAND	:	2
FRANCE	:	18
GERMANY	:	5
ITALY	:	13
JAPAN	:	2
NETHERLANDS	:	1
NORWAY	:	2
SINGAPORE	:	1
SOUTH AFRICA	:	1
SPAIN	:	7
SWEDEN	:	2
SWITZERLAND	:	3
TUNISIA	:	1
UNITED ARAB EMIRATES	:	1
U.K	:	5
USA	:	17
<b>TOTAL: 101 Institutions from 21 countries</b>		

TABLE 3: INSTITUTIONS HAVING RECEIVED THE 65NM DRMS & DESIGN KITS

### Advanced MEMS processes.

For many years, CMP has been offering the MUMPS processes from MEMSCAP: PolyMUMPS, MetalMUMPS, SOIMUMPS. Recently CMP has been moving to SUMMITV from SANDIA and to a MEMS process based on the CMU post process capabilities.

The SUMMIT (Sandia Ultra-planar Multi-level MEMS Technology) fabrication process is a five-layer polycrystalline silicon surface micromachining process (one ground plane/electrical interconnect layer and four mechanical layers). The MEMS structures made possible by this five-layer planarized surface micromachining process are extremely diversified.

CMU post process is a post CMOS processing from Carnegie Mellon University. This post process, applied to an advanced process proposed by CMP (0.35 SiGe BiCMOS from STMicroelectronics), allows to combine on the same chip MEMS structures (resonators, cantilevers, accelerometers, etc.) and microelectronics structures of an advanced BiCMOS process.

CMP also introduced a low cost bulk post process micromachining based on a CMOS .6 $\mu$  from CSMC.

### **ICC**

Founded in 2000 by Science and Technology Commission of Shanghai Municipality, Shanghai Research Center for Integrated Circuit Design (so-called ICC) is dedicated in promoting Shanghai and all China IC Design industry to realize durable rapid development. The services ICC provides include Multi-Project Wafer service, SoC design platform, testing service, training and evaluation, information service, etc.

From 1996 to 2000, Shanghai MPW Service (SMS), operated by Fudan University, was mainly open to academic users, with totally 116 designs fabricated. From 2001, ICC began to operate SMS, expanded the service to industrial sectors and became the China National MPW Center. Totally 877 designs from more than 250 design houses, universities and research institutes were prototyped on MPW runs and low volume production since 2001.

The following technologies were available in SMS in 2007:

- CSMC 0.6 $\mu$ m CMOS
- Chartered 0.35 $\mu$ m CMOS
- Chartered 0.25 $\mu$ m CMOS
- Chartered 0.35 $\mu$ m SiGe
- TSMC 0.13 $\mu$ m CMOS
- TSMC 0.18 $\mu$ m CMOS
- TSMC 0.25 $\mu$ m CMOS
- TSMC 0.35 $\mu$ m CMOS
- SMIC 0.13 $\mu$ m CMOS
- SMIC 0.18 $\mu$ m CMOS
- SMIC 0.35 $\mu$ m EEPROM
- HJTC 0.18 $\mu$ m CMOS
- HJTC 0.25 $\mu$ m CMOS
- HJTC 0.25 $\mu$ m EEPROM

There are totally 22 runs in the year of 2007. 158 chips from 75 customers were successfully fabricated. In 2007, ICC provided an SoC design support platform with the cores from ARM, ZSP, Synopsys and etc, such as ARM7TDMI, ARM926EJ, NEO, ZSP200, ZSP400.

### **IDEC**

IDEC (Integrated Circuit Design Education Center) was launched in 1995 with the support of the Ministry of Commerce, Industry and Energy and major semiconductor

industries for the purpose of educating designers in the non-memory IC field.

Currently, IDEC provides MPW services for 62 WGs (Working Groups) in Korea. As of January 2008, a total of 1,814 IC chips have been successfully fabricated through the IDEC MPW (Multi-Project Wafer) program. The technologies provided in 2007 are listed below:

- CMOS 0.35  $\mu$ , 1-poly 4-metal, Samsung Electronics
- CMOS 0.18  $\mu$ , 1-poly 4-metal, Samsung Electronics
- CMOS 0.35  $\mu$ , 2-poly 4-metal, Magnachip/Hynix
- CMOS 0.18  $\mu$ , 1-poly 6-metal, Magnachip/Hynix
- CMOS 0.18  $\mu$ , 1-poly 6-metal, Dongbu Electronics
- InGaP HBT, Knowledge-on

### **MOSIS**

MOSIS is a low-cost prototyping and small volume production service for VLSI circuit development with a worldwide customer base. Since 1981, the service has fabricated more than 50,000 integrated circuit designs for use by commercial firms, government agencies and universities and has served as the model for similar operations throughout the world. It is a not-for-profit organization started in 1980 by DARPA (Defense Advanced Research Projects Agency of the U.S. Department of Defense) at the Information Sciences Institute to provide their research community with access to advanced IC fabrication lines in a cost effective manner. Fast-turnaround prototype and low-volume fabrication of integrated circuits is available through a number of major commercial IC fabrication vendors such as Agilent/HP (now Avago) Technologies (0.5 $\mu$  CMOS), AMI Semiconductor (0.35 $\mu$ , 0.5 $\mu$ , 0.7 $\mu$ , 1.5 $\mu$  CMOS), IBM (65nm, 90nm, 0.13 $\mu$ , 0.18 $\mu$  and 0.25 $\mu$  CMOS; 0.13 $\mu$ , 0.18 $\mu$ , 0.25 $\mu$ , 0.35 $\mu$  and 0.5 $\mu$  SiGe BiCMOS) and TSMC (0.13 $\mu$ , 0.18 $\mu$ , 0.25 $\mu$ , 0.35 $\mu$  CMOS). CMOS-compatible MEMS technologies are also available. Other technologies such as austriamicrosystems (0.35 $\mu$  CMOS, 0.35 $\mu$  HV CMOS, 0.35 $\mu$  SiGe BiCMOS) are available through a partnership with CMP in France.

### **VDEC**

VLSI Design and Education Center (VDEC), which is located in the University of Tokyo, has been utilized by academic users in Japan since its foundation in May, 1996. As an MPC service center, VDEC aims at improvements of education on VLSI design and supports on VLSI chip fabrication for national universities, public universities, private universities and colleges in Japan. VDEC receives a lot of supports from Japan government, as well as semiconductor industries through STARC (Semiconductor Technology Academic Research Center).

Presently the following technologies are available for chip fabrication service.

- 2-poly 2-metal CMOS 1.2  $\mu$ m process from SCG Japan Ltd. (OnSemiconductor Ltd.)
- 1-poly 5-metal CMOS 0.18  $\mu$ m process from Rohm Co. Ltd.
- 2-metal 0.8 $\mu$ m bipolar process from NEC Compound Semiconductor Devices Ltd.
- 1-poly 6-metal CMOS 90 nm from ASPLA
- VDEC-MOSIS CMOS 0.25 $\mu$ m / 0.18 $\mu$ m from TSMC
- VDEC-MOSIS Si-Ge BiCMOS 0.5 $\mu$ m from IBM

In last VDEC fiscal year (2006.4 – 2007.3), there were totally 24 chip fabrication runs in the last year, each with a 2 to 3 months period. 103 professors and research groups from 55 universities and colleges participated chip design and fabrication through VDEC. Totally 433 chips on 5397 mm<sup>2</sup>

silicon area were designed and fabricated.

## 5. Expanding to MEMS

Another move has been very important: the expansion to MEMS. CMP offered manufacturing for MEMS as early as 1995, being the first service to offer MEMS. Since then the portfolio has been largely expanding and today CMC-CMP-MOSIS offer MEMS manufacturing, including the PolyMUMPS, MetalMUMPS and SOIMUMPS from MEMSCAP. These 3 services enjoy a 10 years MUMPS experience, obtained through 60+ runs, 1800+ designs. It is important that MEMS can be obtained from the same services delivering ICs, so that integration (either at the packaging level or at the die level) is made easier.

## 6. Present cooperative efforts

Presently, the major cooperative effort is undertaken by CMC, CMP and MOSIS. These 3 infrastructure services announced it at DAC in June 2002. Later on, CMP has developed cooperation with ICC in China and IDEC in Korea;

## 7. Conclusions

Several conclusions are addressed in the following, according to 3 broad lines:

- more Moore
- more than Moore
- more than more than Moore

and 2 considerations:

- going global
- being excellent

### A – More Moore

It has been recognized that Students, Researchers and SME designers must be provided with the possibility to have their circuits fabricated. From its inception in 1981, CMP has been successfully pursuing this goal and experiencing a very significant growth to reach and to keep its present level. The success is partly due to the basic principles which have been governing the choices of the Service: use of industrial and advanced process lines. Advanced processes are more and more necessary because of the need for very skilled designers and because CAD industrial software is more widely available to Universities (instead of University CAD software). Since new versions of CAD software are targeted to industrial use, there is no choice but to use advanced processes. Industry makes also more and more use of the Service. During the 80s, the CMP processes were not very advanced, but they approached more and more industry state of the art during the 90s, because of CAD software reasons and because of the increasing industry use of CMP. Since then, CMP is always offering state of the art processes.

Key issues in 2007 were:

- More and more circuits: +25% from 2005 to 2006, +22% from 2006 to 2007.
- Industrial circuits is maintained to about 20% of the total number of circuits and low volume production is provided up to tens of wafers.
- A large portfolio of technologies (17 different processes from low cost processes to very advanced ones) for ICs and MEMS.

### B – More than Moore

The quest for always larger densities may also be satisfied with 3D processes, possibly not including very advanced process dies. 3D processes lead to easier to manage interconnections and to reasonable cost. CMP will introduce soon 3D processes using TSVs (through silicon vias).

It is also recognized that complementary developments must be addressed, in order to address more diversified needs. With this respect, CMP has been a pioneer in being the first service in the world to offer MEMS processes as early as 1995. Going further, more than mechanics-electronics is to be addressed like photonics, optics, fluidics, etc. CMP will be actively promoting these developments in the future.

### C – More than more than Moore

Going further beyond, other communities than EE and CS should be addressed, for which electronics will offer more and more opportunities in the future. CMP has started to address the BioMed community [COURTOIS 08]. Many kinds of BioMed applications are addressed in this paper, ranging from neurosciences to surgery aid, to endoscopy, to skin treatment. Many other kinds of applications might be devised in the future. Going further from dermatology for example, hardware devices might be designed in view of the coming market dealing with dermonutrition or nutricosmetics, depending on the way companies are coming from. Danone is offering yoghurts “nourishing the skin from inside”, and L’Oreal is offering with Nestle nutritional food fighting the skin aging: nutraceuticals with cosmetic benefits (the so-called beauty pills). In both cases, the efficiency can be scientifically measured by specific devices. What is important for the BioMed community is that Education and Research should take advantage of these infrastructures, in the same way as Education and Research in microelectronics have taken advantage of these infrastructures in the 80s. At that time, these infrastructures offered the possibility to EE and CS students, teachers, researchers, to focus on the design of complex circuits hence to focus on the applications, because these infrastructures gave them the opportunity not to be burden by the manufacturing processes, nor by the cost of their projects. Today, various CMOS and MEMS processes can allow students, teachers, researchers to focus on BioMed applications. Not all possible applications can be reached by standard processes offered by service organizations like CMP, but many can be addressed. Other communities could take advantage of such services in the same way.

### D – Going global

All the above requires cooperation between services like CMP, since it is difficult for one single service to offer a wide set of processes of its own. CMP had set up a cooperation with CIC (Taiwan) long ago. Recently, CMC (Canada), CMP and MOSIS (USA) announced a reinforcement of their cooperation in 2002. More recently CMP announced a cooperation with ICC (China) and IDEC (Korea). It is expected that CMP will reinforce such cooperations in the future.

On the side of the users of CMP and of other similar services, the design way is also going more and more global in the sense that more and more IP blocks may come from various sources. This is due to the ever increasing complexity of designs, including parts coming from various teams, countries, companies, etc. An initiative is being developed to go this way: the Global education for Microelectronic Systems (GEMS).

## E – Being excellent

Globalization also requires to be excellent in order to stay ahead of others. This is important at the time of global markets, when every country or continent is a high cost country or continent to another one. Some countries or continents that were said to be “low-cost” countries or continents a few years ago already experience that other countries or continents are coming to the picture with lower costs, forcing them to outsource their own outsourcing. The way to combat that is to stay ahead of the others. The way to stay ahead is to educate and research using top level electronic processes available from top level services like CMP.

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