New lateral DMOS and IGBT structures realized on a partial SOI substrate based on LEGO process

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Abstract — **In this paper, we present new lateral DMOS and IGBT structures based on a partial SOI substrate. The partial SOI substrate, formed through LEGO recrystallization process improves considerably the breakdown capability and the thermal behavior of these devices compared to full SOI devices. Experimental results of high voltage power devices implemented on such a process are presented for the first time.**

Index Terms — **Partial SOI, LIGBT, LEGO, LDMOS**

I. Introduction

Silicon on Insulator (SOI) represents a key route for future development in ultra high level CMOS or Bi-CMOS integration. SOI is also used in MEMS, sensors, smart power and any technologies that require a high level of electrical or, in some cases, thermal isolation. BCD (Bipolar CMOS DMOS) processes are examples of power technologies where SOI has made very dramatic improvements. SOI has also been used in high voltage ICs. Such ICs make use of either thin silicon [1] or thick silicon high voltage technologies [2]. Recently, a combination between a power device and a MEMS (the membrane technology) has also been implemented with spectacular results in terms of breakdown and switching speed [3]. In general all SOI technologies show a very significant improvement in the switching speed when a bipolar device is used. For example, the increased speed of LIGBT (Lateral Insulated Gate Bipolar Transistors) [4] is due to perfect isolation between the substrate and the drift region. Carriers are only stored in the SOI layer and virtually no currents (other than displacement currents) flow through the substrate.

However, there are several aspects which need to be carefully considered when implementing the SOI technology in high voltage ICs: self-heating, reduced RESURF effect and latch-up susceptibility of bipolar devices. We have already showed in a previous paper that the partial SOI concept represents an efficient solution to these problems [5]. In this paper, we present new lateral DMOS and IGBT structures based on a partial SOI substrate realized with the Lateral Epitaxial Growth over Oxide (LEGO) technique [6] that allows obtaining the required thick SOI layers in a cost effective way.

II. PSOI Architecture

The novel PSOI (Partial SOI) device structure combines the advantages of SOI and JI (Junction-Isolation) technologies (Fig 1 c, a and b respectively) [5]. As compared to typical JI and SOI lateral power devices, the new device structure has an interrupted buried oxide (BOX), which allows the drift region to be connected to the substrate. All the results presented below are obtained from Medici (Synopsis) simulation software.

Fig 2 shows the potential distributions at breakdown for the JI, SOI and PSOI structures for typical dimensions and doping levels. The breakdown voltages on JI, SOI and PSOI structures are 545V, 163V and 499V, respectively. These discrepancies for identical LIGBTs are due to the buried layers. When the power device in traditional SOI technology is in the blocking mode, the buried oxide prevents the spread of the depletion region into the substrate due to the formation of a layer of mobile charge under the BOX layer. Just below the anode, the buried oxide and the top silicon layer support almost all the voltage applied between the anode and the substrate terminals. Hence in standard SOI devices, a thinner BOX lowers the breakdown voltage. To obtain a typical SOI device with a breakdown voltage above 400V, it is necessary to have at least 3-4μm of BOX. In the PSOI structure, the silicon window into the BOX at the anode allows the potential lines to spread into the silicon substrate in a similar manner to that met in JI high voltage devices. The voltage applied between the anode and the substrate is now supported across the buried oxide, top silicon and the depletion layer into the substrate. This helps significantly improve the device breakdown voltage. The breakdown of PSOI structures can be further improved by reducing the substrate doping. However, it is

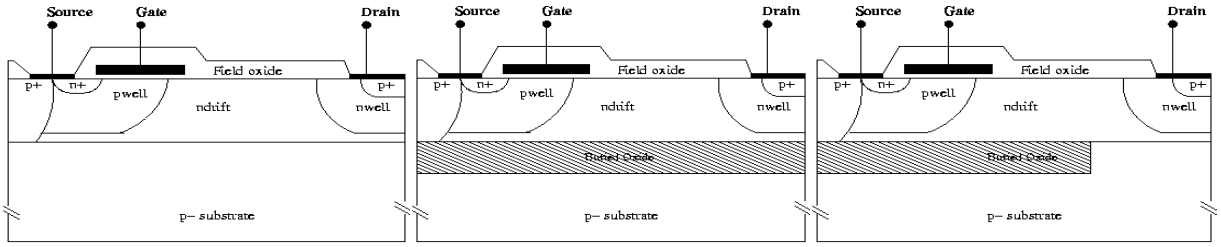


Fig. 1: Power LIGBT structures in (a) JI (b) SOI and (c) partial SOI technologies.

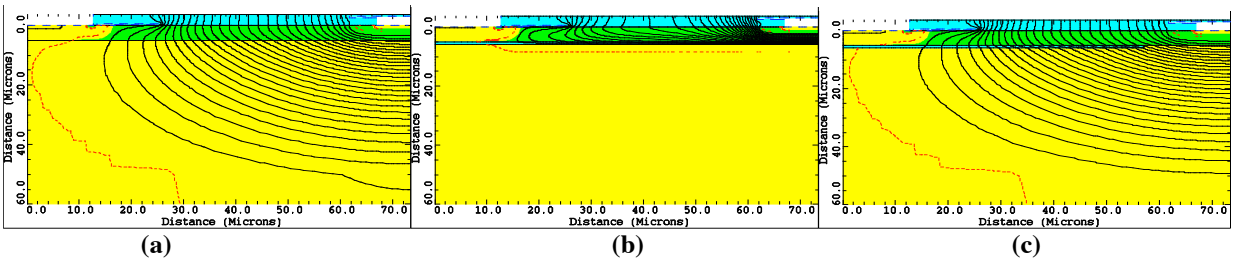


Fig. 2: Potential distribution at breakdown in the LIGBT structures in (a) JI (b) SOI and (c) partial SOI technologies. Buried oxide thickness is 1μm, top silicon layer is 5μm, substrate doping is 1e14 cm^{-3} and drift region doping is 13e14 cm^{-3}.

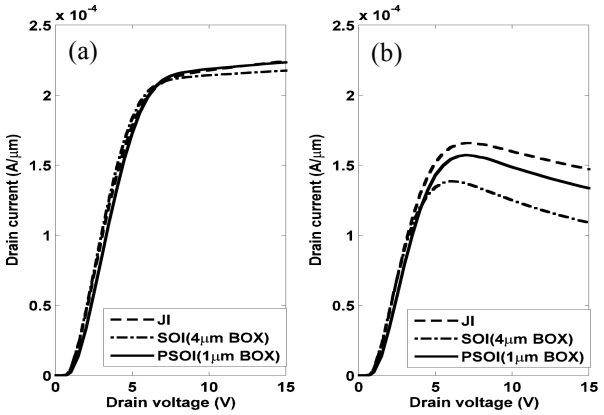


Fig. 3: Simulated on-state LIGBTs characteristics (a) without self-heating (b) with-self heating.

a technological challenge to have a lower substrate doping.

For a common substrate doping level of 6e14 cm^{-3} the breakdown on the PSOI structure would be around 325V.

Fig 3 depicts the on-state simulation results of JI, SOI and PSOI structures with and without self-heating effects. Without self heating effects the on-state characteristics of all the devices are nearly identical. However, when self-heating effects are included, the SOI device on the 4μm BOX has the largest self-heating effects due to the low thermal conductivity of the thick buried oxide compared to that of silicon. The high temperature inside the active area in SOI devices can therefore affect device operation and the reliability of the entire circuit. The LIGBT on JI technology has unsurprisingly the lowest self-heating effect. Finally, in the PSOI structure, some heat can flow through the open window at the anode, helping to lower the device temperature. However PSOI structure has also a substrate current generating power in the substrate, increasing the substrate temperature. Overall, the LIGBT on PSOI technology is only slightly worse in terms of on-state performance than the equivalent device in JI technology.

Fig 4 shows the turn-off waveforms for an inductive switching. The SOI and PSOI devices exhibit the classical terrace in the turn-off current waveforms due to the hole inversion layer at the top of the the BOX [7]. This terrace disappears when the depletion region hits the n-buffer. The turn-off current in the PSOI device is larger than in the SOI device due to the substrate injected carriers. The turn-off in the JI device is faster due to the fast expansion of the depletion width due to the absence of the hole inversion layer at the top of BOX.

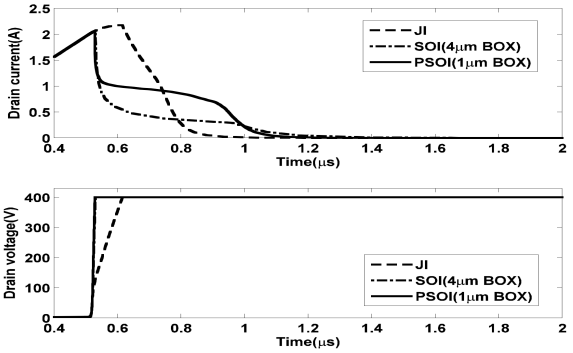
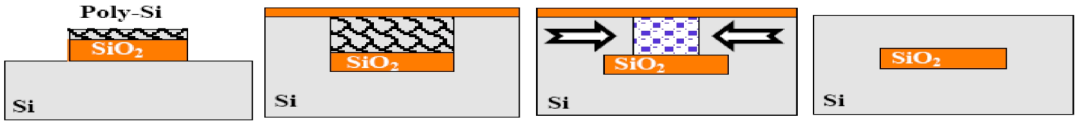


Fig. 4: Comparison of simulated turn-off currents and voltage waveforms for an inductive switching.



(a) (b) (c) (d)

Fig. 5: Basic steps of the recrystallization process to build the partial SOI substrates (see text).

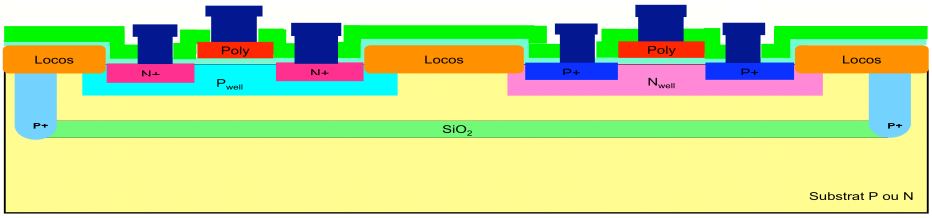


Fig. 6: Cross-section of the CMOS/DMOS/IGBT partial SOI process based on LEGO technique.

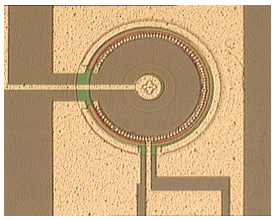


Fig. 7: Optical view of the new LIGBT on PSOI substrate.

III. PSOI Fabrication Technology: The LEGO Process

An important challenge is the realization of such partial SOI substrates at low cost and with efficient electrical insulation. Most of the existing techniques to obtain SOI structures are generally expensive and provide full and thin SOI wafers [6]. Only one technique, the Zone Melting Recrystallization (ZMR), allows the straightforward and cost effective production of thick SOI layers. This is achieved through a rapid melting, followed by a controlled recrystallization, of poly-silicon films deposited over SiO_2 patterns grown on a silicon wafer using a scanning heater.

To realize new PSOI-based LDMOS and LIGBT structures, we used the LEGO technique [6] that allows obtaining the required localized and thick SOI layers in a cost effective way. Firstly developed by Celler and al. [8], it is directly inspired by the ZMR technique and is being reconsidered today because of a new market demand for partial SOI. The main difference with conventional ZMR is that the heat source of the rapid thermal processor (RTP), is uniform throughout the entire wafer surface thus allowing a simultaneous recrystallization of all poly-crystalline patterns.

Hereafter is a brief description of the LEGO process, referring to Fig.5. The wafers are pre-processed with a 1μm-thick thermal oxidation and a polysilicon seed layer deposition. After patterning the SOI islands (Fig.5.a), a non selective epitaxy is deposited. It is polycrystalline over the SOI patterns and monocrystalline on the rest of the wafer. An oxide-capping layer is then added to prevent the melted silicon evaporation during the recrystallization step (Fig.5.b). Then, a specific RTP furnace [8] provides enough energy to melt the polycrystalline areas while maintaining the bulk monocrystalline area solid. As the temperature ramps down, given the different thermal conductivities of silicon and oxide layers, a thermal gradient is laterally induced and allows a recrystallization front spreading from the mono-crystal seed over the buried oxide layer (Fig.5.c).

However, after recrystallization, surface roughness is important because of the liquid silicon movement, and planarity has to be restored through a chemical mechanical polishing (CMP) (Fig.5.d). We have experimentally demonstrated [6] that such a process allows building recrystallized SOI islands 1 mm wide, for 30 µm initial epi-layer thickness and 15 sec RTP annealing duration. Using these partial SOI substrates, a CMOS/DMOS/IGBT process (Fig.6), was developed at LAAS-CNRS. On this cross-section, only CMOS devices are shown. The initial substrate could be either N or P-type and the epi-layer is N-type. Full isolation of the SOI islands is obtained through a deep P^+ diffusion.

IV. Experimental Results

A dedicated test mask was designed to validate the simulated structures. The starting P-type substrate has a 20Ω.cm resistivity (~6e14 cm^{-3}) while the N-type epitaxial layer resistivity is 5 Ω.cm. Both LDMOS and LIGBT devices were included. A circular layout, more appropriate for high voltages, was chosen. Fig. 7 shows an optical view of one LIGBT device. The SOI island is defined by the external circle featuring a 200 μm diameter. The central circle is the LIGBT anode and a 40μm-diameter window is opened underneath into the BOX.

Breakdown voltage measurement resulted in values ranged from 226V to 277V for the LIGBT (Fig.8) and from 280V to 315V for the LDMOS, in agreement with the simulated ones, thus confirming the beneficial effect

of the window opened into the BOX. Achieving breakdown voltages close to the predicted ones also demonstrates the crystalline quality of the recrystallized layers.

A static thermal measurement was carried out on the PSOI LIGBT using an infrared camera. Under a power of 2,28W, the maximum steady-state temperature resulting from self-heating was of 329K.

Switch off measurements were performed thanks to the electrical setup depicted below (Fig.9). A typical turn-off time of 400ns could be measured (Fig. 10) and fully agrees with simulation.

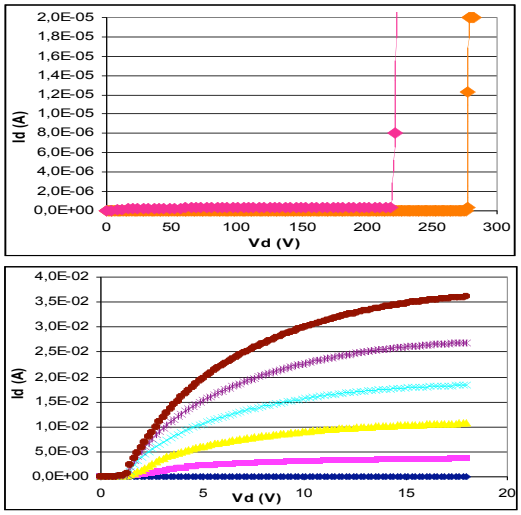


Fig. 8: Breakdown voltage at Vg=0V (top) and Id (Vd) characteristics with Vg ranging from 0 to 10V by steps of 2V (bottom) of the new LIGBT structure.

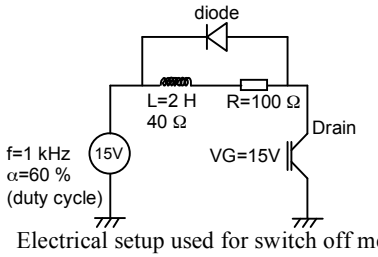


Fig. 9: Electrical setup used for switch off measurements.

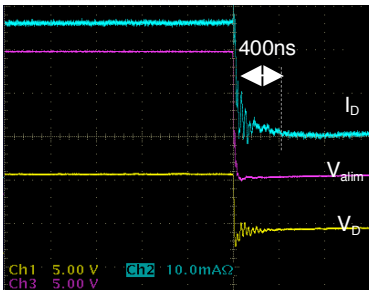


Fig. 10: Measurement of PSOI LIGBT switch off time.

V. Conclusion

New LIGBT and LDMOS structures based on a partial SOI technology are proposed. The partial SOI process has been implemented using the LEGO technique. The new structures offer an increased breakdown capability associated with reduced heating effects when compared to standard SOI. For the first time, high voltage devices exhibiting 300V breakdown voltage are implemented on such a technology. The new structure is particularly relevant to the manufacturing of high voltage integrated circuits (HVICs) where high speed, good isolation and reduced self-heating are essential.

Acknowledgement

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