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Abstract

In this paper, it is demonstrated that low frequency noise measurements are an efficient tool for the detection of latent defects induced by CDM stress in a complex circuit such as a DC-DC converter. This technique is able to detect the presence of a defect whereas classical electrical testing techniques such as Iddq or functionality test fail. In addition, a correlation between the noise signature and the nature of the defect is established. In particular, the presence of trapped charges in the oxides is clearly identified.

1. Introduction

ESD qualification of circuits usually insures that after a given maximum ESD stress level, the circuit keeps its functionality and leakage currents within specifications. Even if a low increase in leakage currents is acceptable, this is anyway the proof that the circuit suffered a degradation that could be a latent defect. Such a defect may evolve during circuit operation and later on result in a field failure.

CDM stress is susceptible to induce defects in gate oxides such as trapped charges that cannot easily be detected in a complex circuit using Iddq techniques given the low value of the induced leakage current (hundreds of nano-amps). In this work, low frequency noise (LFN) measurements [1] are used to detect such CDM induced defects into a commercial circuit, namely a DC-DC converter. For two particular parts under study, leakage current measurement and functionality testing indicate that the parts are good although the noise level did not get back to its pre-stress level, indicating the presence of latent defects.

LFN also allows identifying the nature of the defect, oxide or junction, depending on the noise signature. In section 2 we present the circuit under study and the CDM stress experiment. In section 3, a thorough electrical investigation based on DC and low frequency noise measurements allows identifying charge trapping into the oxides. In section 4, the analysis of the ESD protection strategy through TLP and VF-TLP measurement and mixed-mode simulation is carried out to get a deeper understanding of the failure mechanism.

2. Circuit under study and CDM stress plan

The product under study is a 1MHz PWM boost converter with integrated rectification optimized for constant current applications. It is fabricated in a 0.8μm BiCMOS technology. The input voltage range is from 2.7 to 5.5 V. Its ESD specifications guarantee a robustness of 2kV HBM and 200V MM but do not include CDM. CDM stress is well known to be a threat for thin oxides. This technology has a gate oxide

thickness of 20nm, which corresponds to a DC breakdown voltage of 18V. Under TLP (100ns pulse) and VF-TLP (5ns pulse) stresses, this breakdown voltage value increases up to 30V and 43V, respectively.

For this study, six parts, P1 to P6, of the converter circuit are chosen to undergo the stress plan. They are housed in DIL24 packages. Additional parts are used as reference ones. Before stress, functionality test of all chips is performed. It includes leakage current measurement (Iddq) in standby mode (CTL pin set to 0V to disable the whole chip) that ranges from 200 to 270nA at VIN=4.2V. Low frequency noise measurements were also carried out. Surprisingly, the noise level is very low and cannot be differentiated from the set-up noise.

Six chips, P1 to P6, are stressed using a Field Induced CDM tester from +/-500V to +/-2000V on the CTL pin, the Enable pin of the chip, which is directly connected to two NMOS gates (Fig. 1) (*M0 and M1*). The gate of M0 is five times longer than the one of M1. Each part receives a single voltage stress level (3 zaps) [2] as shown in Table 1. This input pin is protected by a localized ESD protection using a self-biased NPN transistor.

Table 1. CDM stress plan and Iddq (in µA) evolution measured at 4.2V on CTL pin. Iddq of reference device is 270nA. F stands for Failed and N.A. for Not Applicable.

	P1	P2	P3	P4	P5	P6
CDM (V)	+500	-500	+1k	-1k	+2k	-2k
Iddq after CDM (µA)	1.3	0.75	5.1	390	5.3	430
Functionality after CDM	**F**	**F**	**F**	**F**	**F**	**F**
Iddq after 3 months (µA)	0.76	0.62	3.9	1.0	3.7	438
Iddq after burn-in (µA)	0.2	0.2	0.56	57	1.2	91
Functionality after burn-in	**OK**	**OK**	N.A.	N.A.	N.A.	N.A.

3. Electrical analyses after CDM stress

3.1 *Functionality and leakage current tests*

After CDM stress, functionality tests of all chips are performed again. They showed that all stressed chips are failed (Table 1). For P1 and P2, only the leakage current in standby mode failed. Right after stress, we also carried out LFN measurements that will be described in the next sub-section.

Three months later, functionality tests are performed again and show that for the chips stressed at +500V (P1) and -500V (P2), all electrical functions are

retrieved. Concurrently, at 4.2V in standby mode, the leakage current of P1 and P2 has significantly decreased from 1.3 and 0.75µA to 760 and 620nA, respectively.

Fig.1. Electrical schematic of CTL pin input circuit.

EMMI (EMission MIcroscopy) analysis did not allow detecting any defect location in P1 and P2. However, as shown in Fig. 2, P6 part that is stressed at a higher CDM level, exhibits an emitting defect located into the gate oxide of the input NMOS, M1 (in Fig.1). During the CDM stress on CTL pin, M1 and M0 are both exposed to a high electrical field, but having a five times smaller gate surface, M1 is more susceptible than M0.

Fig.2. EMMI analysis of P6 showing an emission on M1 transistor of CTL pin input circuit.

To explain the evolution of the leakage current over time, we assume that for P1 and P2, charge trapping into the oxide, and in particular mobile charges [12], induced a shift in the threshold voltage of the MOS transistor. These mobile charges can be thermally activated and de-trapped from oxides [10], then resulting in a decrease of Iddq [9].

To verify this assumption, we performed a burn-in at 125°C for 24 hours for all chips. After the burn-in, as shown in Table 1, the Iddq current of all parts decreased. However, only P1 and P2 leakage currents returned to their original value (200nA). After burn-in, these two chips passed the functionality test. If such devices were tested for qualification, they would then pass the test.

To check that no latent defect was induced by the

CDM stress, we also performed LFN measurements. The analysis of the results is given in the following sub-section.

3.2 *Noise signatures of CDM induced defects*

LFN measurements are performed between 10 Hz and 100 kHz using a dedicated test set using a transimpedance amplifier [3]. They are realized before and after CDM stress on the power supply pin (VIN) under the standby mode (CTL=0V). Fig.3 represents the frequency variations of the power spectral density (PSD) of the noise current (S_i) associated to the leakage current Iddq for the different investigated circuits.

Before CDM stress, the PSD of the noise current of all the circuits is less than the noise level of the experimental setup (2.3 10^{-24} A^2/Hz) and is found almost constant over the frequency range. After CDM stress, the circuits with the smallest leakage currents (P1, P2 and P3) have been chosen to undergo LFN measurements. Iddq on VIN of P1 and P2 is in the range of 600nA at 3.6V and should be compared to 270nA before stress.
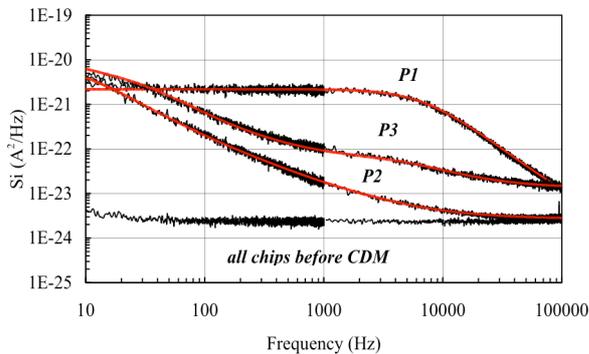
Fig.3. LFN measurements before and after CDM stress. (CTL=GND, VIN=3.6V, Iddq=270nA before CDM, Iddq = 600nA after CDM). The solid lines correspond to the model.

We can observe in Fig.3, a strong increase of the low frequency noise after CDM stress for the different circuits. All the different spectra have been modeled with the following equation represented by solid lines (Fig.3):

$$Si(f) = A + \frac{B}{f} + \sum_i \frac{C_i / f_{ci}}{1 + (\frac{f}{f_{ci}})^2} \qquad (1)$$

The parameter A corresponds to a white noise component, which is generally preponderant at high frequency. The second term in Eq.(1) is linked to the flicker noise, or 1/f noise, and is attributed to mobility or carrier number fluctuations. The last term in Eq.(1) is related to generation-recombination (G-R) noise sources characterized by Lorentzian spectra and corresponding to the presence of recombination centers located either in oxides or source-drain junctions reacting as Generation-Recombination sites or traps for carriers [13]. A, B and C_i are fitting parameters and f_{ci} corresponds to the corner noise frequency associated to the i_{th} G-R noise source. 1/f noise and G-R noise are very sensitive to the presence of defects and LFN measurements are used as a diagnostic tool for quality and reliability of electronic circuits [4].

As can be seen in Fig.3, CDM stress induces an increase of the low frequency noise for all the investigated devices. The noise coefficients obtained from the simplified model given by Eq.(1) are reported in Table 2.

Table 2. Noise coefficients used to model the noise PSD after CDM stress of the different circuits reported in Fig.3.

	P1	P2	P3
A	2 10^{-24}	2.7 10^{-24}	1.4 10^{-23}
B		1.5 10^{-20}	3.5 10^{-20}
C_1	1.6 10^{-17}	5 10^{-20}	9 10^{-20}
f_{c1}	7 kHz	10 Hz	30 Hz
C_2			2.5 10^{-19}
f_{c2}			7 kHz
C_3			1.5 10^{-19}
f_{c3}			30 kHz

The noise PSD of P1 part is largely dominated by a G-R noise source for frequencies up to 7 kHz. Concerning the part referenced as P2, flicker noise and a G-R noise source with f_{c1} close to 10 Hz are present. The behavior of P3 after the CDM stress is different since the noise PSD is now characterized by several G-R noise sources up to a few tenth of kHz.

On P1 part, LFN measurements were also carried out after a period of storage (one, two and three months) after the CDM stress to study the noise evolution. As shown in Table 1, the leakage current decreases gradually. However, the G-R noise source always exists in P1 part (Fig.4). Given this behavior over time, it can be assumed that this noise source is generated by the presence of traps located into the MOS gate oxides. The thermally de-trapped charges results in a decrease of G-R noises created by the carriers injected into the gate oxide by the field enhanced at the rough polysilicon/SiO$_2$ interface [11].
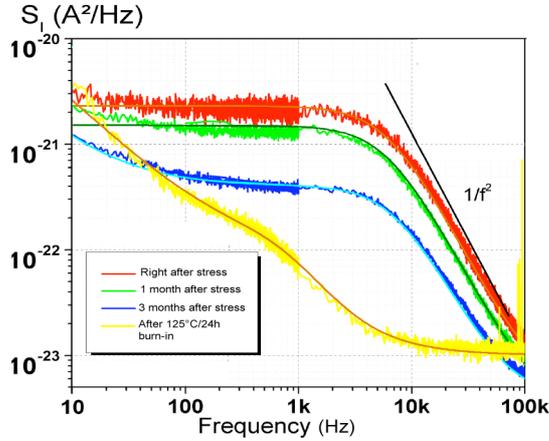
Fig. 4. LFN evolution of P1 after CDM stress and burn-in treatment. Solid lines are the fitting curves.

To evaluate the density of traps and its evolution, we used the G-R noise PSD formulation that is a function of current and trap density [5]:

$$S_i(f) = \frac{I^2}{n^2V^2}\overline{\Delta N^2}\frac{4\tau}{(1+\omega^2\tau^2)} \qquad (2)$$

where V is the semiconductor volume, n the free electron density, I the current, ΔN the carrier number fluctuation, τ the time constant (given by $1/(2\pi f_c)$) associated to the G-R process and ω the pulsation.

The fit of the measured LFN curves in Fig.4 requires that the parameter $\frac{\overline{\Delta N^2}}{n^2V^2}$ associated to the trap density decreases from a value of $7.2\cdot10^{-5}$ right after CDM stress down to $1.2\ 10^{-5}$ three months later.

To confirm that such behavior can be attributed to traps into the oxides, we carried out a burn-in at 125°C during 24 hours and performed again the noise measurement. After the burn-in treatment, the LFN signature of P1 (Fig. 4) greatly evolved: first, the G-R noise source with a 7 kHz corner frequency disappeared. This could be attributed to the de-trapping of trapped charges into gate oxides of the circuit [6]. Secondly, a new G-R source featuring an 800 Hz corner frequency is now visible. In addition, a 1/f noise source previously hidden by a strong G-R noise component before burn-in, now clearly appears on the spectrum for frequencies below 100Hz.

Nevertheless, despite the burn-in treatment, the noise level did not return to its initial value. At high frequencies, the original value was in the range of $2.0\ 10^{-24}$ A^2/Hz whereas after stress and burn-in, it increased by one decade (10^{-23} A^2/Hz) and by three decades at 10Hz. This result means that CDM-related latent defects are remaining after the cure of oxide-trapped charges.

The failure status observed after CDM stress can be explained by the presence of these trapped charges into the gate oxides of the CTL input MOS transistors. Even in disabled mode (CTL=0V), the resulting threshold voltage shift induces a marginal circuit biasing. Apparently, we are in presence of mobile charges [6]. With some energy, for example, burn-in at high temperature, they can be de-trapped and functionality and Iddq of the circuit reset to their initial values.

3.3 Evolution of the defect after 2000h ageing

Finally, to check the impact of the latent defect detected via LFN measurements, we carried out an ageing experiment on P1. The circuit was biased under 3.6V and is activated (CTL="1"), providing in this configuration a 500mA current to a resistive load. The temperature is 85°C and a reference circuit is also undergoing the same ageing experiment. The Iddq leakage current was monitored every day. After 2000h, the Iddq current at a 3.6V voltage of the reference circuit kept at its initial value whereas the P1 one increased very slightly from 270 nA to 400 nA.

LFN measurements were performed again on P1 after the ageing experiment and results are plotted in Fig.5. The noise PSD has evolved and increased mainly in the high frequency range of the spectrum. The noise coefficient obtained from the fitting are summarized in Table 3.
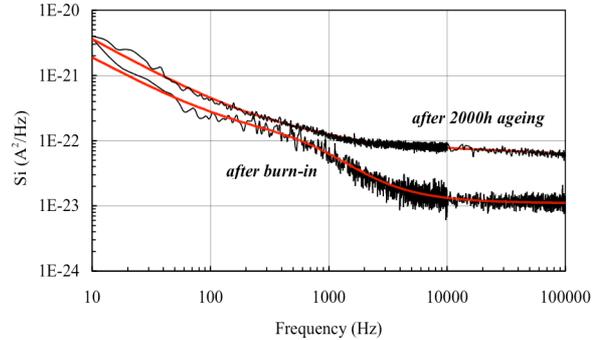

Fig. 5. LFN evolution of P1 after 2000h ageing experiment at 85°C and biasing for DC-DC conversion activated. Comparison with the LFN spectrum after burn-in. Solid lines correspond to the fitting curves.

Firstly, the 1/f noise component (B parameter) exhibits a slight increase and the G-R noise source around 1 kHz is still present. Secondly, additional G-R centers (C2, C3) appear after ageing. It is also interesting to notice that after ageing, the noise PSD of P1 is now similar to the one of P3 which underwent a

CDM stress with the same polarity but at a higher voltage level (1kV). Although the DC characteristic (Iddq) is still within the specifications, this result demonstrates that the CDM induced defect has evolved during the ageing experiment.

Table 3. Noise coefficients used to model the noise PSD of P1 reported in Fig.5. Noise coefficients of P3 obtained after CDM stress are also reported for comparison.

	P1 after burn-in	P1 after ageing	P3 after 1 kV CDM stress
A	$1.1 \ 10^{-23}$	$2.0 \ 10^{-23}$	$1.4 \ 10^{-23}$
B	$1.8 \ 10^{-20}$	$3.5 \ 10^{-20}$	$3.5 \ 10^{-20}$
C_1	$7.0 \ 10^{-20}$	$3.0 \ 10^{-20}$	$9.0 \ 10^{-20}$
f_{c1}	780 Hz	1 kHz	30 Hz
C_2		$1.6 \ 10^{-19}$	$2.5 \ 10^{-19}$
f_{c2}		20 kHz	7 kHz
C_3		$5.0 \ 10^{-18}$	$1.5 \ 10^{-19}$
f_{c3}		200 kHz	30 kHz

4. Discussion

To understand the reasons for the poor CDM performance of this circuit, we studied the robustness of the involved ESD protection on the CTL pin both under TLP and VF-TLP stress. To this aim, we used a minimum size MOS transistor *(W=0.8μm, L=1.6 μm)* as gate monitor (Fig. 6) [8].
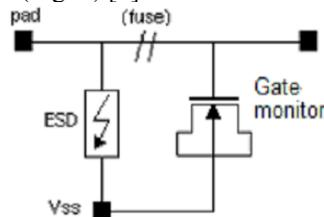
Fig. 6. Gate monitor configuration.

Under TLP stress, both in direct and reverse mode, the ESD protection that is a self-biased transistor, correctly protects the gate monitor. Under VF-TLP stress, in direct mode, the ESD protection also efficiently protects the gate monitor. However, in reverse mode, the gate monitor fails. We also performed TLP and VF-TLP testing on a standalone protection (Fig. 7). It resulted that the TLP failure current $I_{t2\text{-}TLP}$ is higher than 3A thus easily guaranteeing a 2kV HBM robustness whereas the VF-TLP failure current $I_{t2\text{-}VFTLP}$ is higher than 15A. This means that the ESD protection is very robust under a fast ESD transient such as a CDM one. However, it can be noticed that the on-resistance of the structure is such that at 8A, the VF-TLP oxide breakdown is reached. Such high currents can be reached during a CDM stress. Thus, during a CDM stress, the gate oxide could

be submitted to high electric fields that induce Fowler-Nordheim conduction through the oxide and then charge trapping.
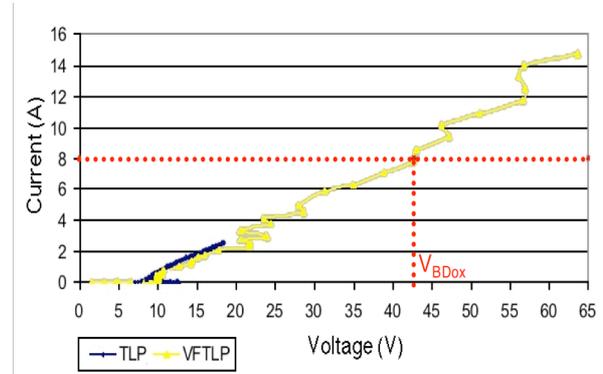

Fig.7 TLP and VF-TLP measurements in the reverse mode of the ESD protection that is implemented on the CTL pin. The red dashed line indicates the maximum current at oxide breakdown (V_{BDox}) under VF-TLP.

P1 part was stressed under a positive CDM stress whereas P2 was stressed under a negative one. For the failure of P2, the localized ESD protection on the CTL pin is clearly at the origin of the failure. For P1, it works in forward mode and then should efficiently protect the input circuit. In this case, the full protection strategy is probably not correctly sized for such high currents. As a result, resistive paths may induce high voltage drops and then the generation of electric fields high enough to induce charge trapping into the oxides.

To confirm these assumptions, we carried out mixed-mode simulations of the positive and negative CDM stress configurations on the CTL pin for 500V and 2kV stress levels. In these simulations, only the ESD protection device is 2D-simulated. Access resistances extracted via TLP measurement are added: 2.2Ω for the device in forward bias (positive CDM stress) and 5Ω for the device in reverse bias (negative CDM stress). As shown in Fig.8, the voltage across M0 and M1 is particularly high for both positive and negative stresses. As expected the positive stress is less stressful since it involves a forward biased diode. However, even for the lower stress level, the maximum voltage is in the range of the VF-TLP oxide breakdown value or higher (but just during few hundreds of ps). These qualitative results confirm that the protection device does not protect the input during a CDM stress and that gate oxides undergo very high electric fields susceptible to generate charge trapping. The observed trends are also in agreement with the measured post-stress Iddq: for positive and negative 500V CDM

stress, it is in the same range whereas for 2000V, the negative stress is much more stressful than the positive one (P6 was the only device where the gate oxide breakdown could be localized).
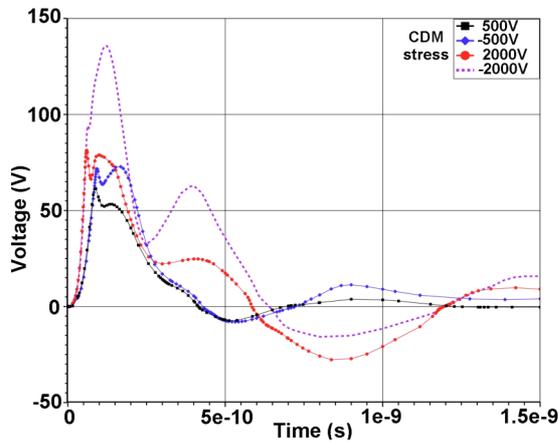

Fig.8. Voltage across the gates of M0 and M1 NMOS transistors obtained through mixed mode simulation for positive and negative 500V and 2kV CDM stresses.

5. Conclusion

We have shown that CDM stress can induce latent defects in a 1MHz DC-DC converter, realized in a 0.8μm BiCMOS technology. Such defects could not be detected via Iddq or functionality testing. They were successfully detected using LFN measurement technique. It was shown that a part of the noise was attributed to trapped charges into the oxides and could be correlated with a generation-recombination noise source. A burn-in treatment allowed getting rid of the G-R noise signature but the noise spectrum did not get back to its original one. A 1/f noise signature generated by mobility or carrier number fluctuations remained after burn-in that can be attributed to a latent defect. This defect is probably located into a junction, since a filament across a junction will increase crystal lattice scattering by carriers and impact the carrier mobility. It can be concluded that, in case of latent defects, LFN measurements can be an efficient tool to discriminate oxide-trapped mobile charges from silicon defects.

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