



Pushing away the silicon limits of ESD protection structures: exploration of crystallographic orientation

David Trémouilles, Yuan Gao, Marise Bafleur

► To cite this version:

David Trémouilles, Yuan Gao, Marise Bafleur. Pushing away the silicon limits of ESD protection structures: exploration of crystallographic orientation. BIPOLAR/BiCMOS Circuits and Technology Meeting (BCTM), Oct 2008, Monterey, United States. pp.200-203. hal-00383353

HAL Id: hal-00383353

<https://hal.science/hal-00383353>

Submitted on 12 May 2009

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Pushing away the silicon limits of ESD protection structures: exploration of crystallographic orientation

D. Trémouilles¹, Yuan Gao^{1,2}, M. Bafleur¹

LAAS-CNRS; Université de Toulouse ; 7, av. du Colonel Roche, F-31077 Toulouse, France

Freescale Semiconductor; 134 av. du Général Eisenhower 31023 Toulouse Cedex, France

Abstract — Improving the ESD robustness of integrated protection structures to cope with the constraints of severe environments such as the automotive one is a real challenge. Getting a deep understanding of the involved high injection physics during an ESD stress helps defining specific design guidelines. The grounded-base NPN bipolar transistor is a popular and efficient protection device. In this paper, we explore the impact of crystal orientation on the electrical characteristics and the robustness of this device. It is shown for the first time that orienting the structure 45° with respect to the wafer flat allows significantly improving its on-resistance. A 30% improvement is measured on the device under study.

Index Terms — Grounded-base bipolar transistor, electrostatic discharge (ESD), impact ionization, ESD protection, crystal orientation.

I. INTRODUCTION

Designing area efficient and robust ESD protections is more and more challenging. ESD specifications are getting increasingly more severe with the requirement of new ESD testing on ICs such as the gun stress in automotive applications. Concurrently, the ESD design window is narrowed thus requiring protection structures with a very low on-resistance. The grounded-base NPN bipolar transistor is a popular and efficient protection device. In previous work [1][2], the thorough analysis of the physical mechanisms involved under the high injection conditions of an ESD stress allowed proposing efficient ESD design guidelines. To further push away the silicon limits of such protection structure, we explored the impact of crystal orientation. In this paper, after reminding the main physical mechanisms that control the robustness of a grounded-base NPN bipolar transistor, we will present experimental results on this structure when implemented with a 45° angle with respect to the wafer flat. The improved performance will be explained according to the theory of impact ionization.

II. DESIGNING A HIGH ROBUSTNESS ESD PROTECTION

A widely used ESD protection is the grounded-base NPN bipolar transistor. We thoroughly analyzed the

physical mechanisms involved under the very high current density that the protection structure has to handle during an ESD stress [1].

Firstly, let us remind that, in the reverse mode (positive ESD zap on the collector), the grounded-base NPN transistor is triggered on by the current resulting from the avalanche breakdown of the collector-base junction. Fig.1.a illustrates its principle of operation: the current source is the collector-base avalanche current and the resistance is either the intrinsic base resistance or an external resistance. The corresponding I-V characteristic is shown in Fig.1. Once the NPN is activated (at triggering voltage V_{t1}), the current gain allows the base-collector voltage needed to bias the bipolar transistor to decrease down to the holding voltage V_H .

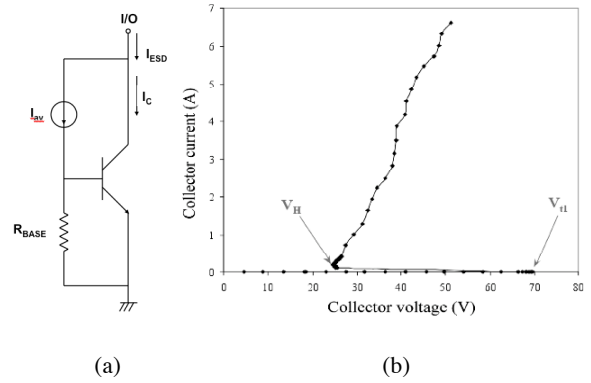


Fig. 1: Electrical schematic of the principle of a vertical grounded-base NPN transistor (a) and TLP characteristic in reverse mode (b).

In this mode, we observed two main remarkable physical behaviors. First, given the self-biasing triggering mode, the voltage along the width of the emitter is not homogeneous and there is a current focalization at the emitter edge closest to the collector-base junction as shown in Fig.2 for a vertical grounded-base NPN transistor.

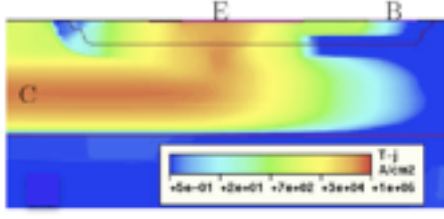


Fig. 2: Current density in a vertical grounded-base NPN submitted to a 2kV HBM stress. Cross-section across the emitter width.

A good current homogenization along the emitter length is also necessary to achieve a high ESD robustness. To study the current flow along the device length, we used a simplified structure of the NPN transistor as shown in Fig.3.e and performed 2D-simulations of an HBM stress in open-base condition.

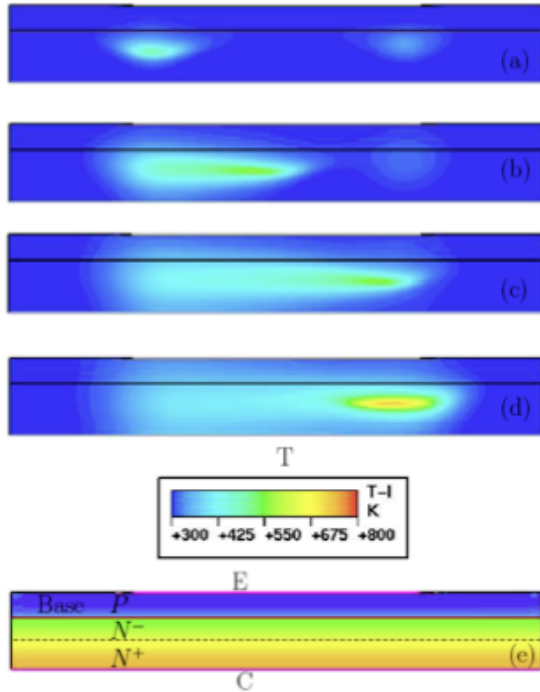


Fig. 3: 2D-electrothermal simulation of a 500V HBM stress along the emitter length of the NPN of Fig.2. Temperature at (a) 10ns, (b) 30ns, (c) 50ns and (d) 70ns. Doping profiles in the structure (e).

Even though the base-emitter voltage is uniform, current focalization, starting at the edges of the emitter occurs (Fig.3.a-d). However, during the ESD transient, its location moves along the length of the device as shown by the various cross-sections of Fig.3 at different times during the stress : 10, 20, 50 and 70 ns. This behavior that homogenizes the power dissipation, can be explained by the negative temperature feedback of the avalanche phenomenon. After this theoretical study, the hot spot movement was experimentally demonstrated using laser interferometry by Pogany et al [3].

The hot spot movement greatly delays the ESD failure of the structure and if favored should allow increasing the ESD robustness. This study, carried out on a vertical grounded-base NPN transistor issued from a smart power technology resulted in the definition of universal design guidelines [1] [2]. They are mainly based on decoupling the two multiplication mechanisms involved in the bipolar device: current gain (β) and avalanche multiplication. To validate the universality of these design guidelines, we applied them to different technologies and in particular to a CMOS technology where the only available NPN bipolar transistor is a lateral one.

III. IMPACT OF CRYSTAL ORIENTATION

The considered technology is a $0.6\mu\text{m}$ CMOS technology. The NPN bipolar transistor is a lateral one realized by using the minimum spacing between two N^+ diffusions separated by field oxide isolation. To favor the hot spot movement during the ESD stress, we designed an octagonal NPN structure so as the hot spot could move around it thus resulting in a better temperature homogenization. The protection structure was designed in such a way that it could be integrated within a pad: the base and emitter are in the center and the collector surrounds the structure.

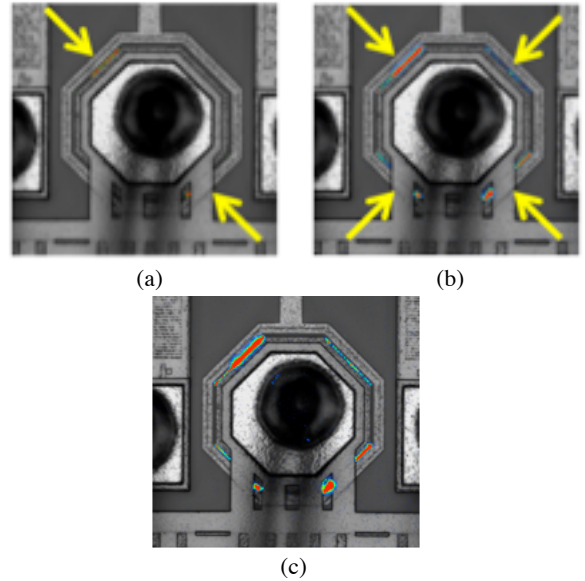


Fig. 4: Octagonal NPN-based protection structure observed by EMMI under DC stress: (a) $I=0.5\mu\text{A}$, (b) $I=5\mu\text{A}$ and (c) $I=10\mu\text{A}$. Emitter and base are in the center and collector surrounds them.

To check how the structure triggers on, we observed it by emission microscopy (EMMI) both under DC and TLP bias. The DC results are shown in Fig. 4. In contrast to what expected, the structure firstly triggers on along the sides of the octagon that are oriented at 45° with respect to the flat. The conduction starts along one couple of sides at 45°

(Fig. 4.a) and when current increases, the second couple of sides at 45° also triggers on (Fig. 4.b). However, further increasing the current do not allow the sides at 90° to contribute to the current (Fig. 4.c).

We suspected that the triggering on a preferential orientation might be attributed to the difference in density of the crystal network resulting in higher impact ionization and then larger avalanche current. Indeed, when the avalanching collector-base junction of the bipolar device is oriented parallel or perpendicular to the flat of a {100} wafer, the corresponding directions of the current are $\langle 110 \rangle$. If this junction is rotated by 45°, these directions are $\langle 100 \rangle$. Anderson and Crowell [4] were the first to consider the influence of crystallographic direction on the threshold energy of electron-hole pair production by impact ionization. Later on, other authors [5] [6] computed more accurately this threshold energy and it resulted that the lowest one is in the $\langle 100 \rangle$ crystal direction. The authors particularly highlighted that this anisotropy between crystal directions should mainly play an important role at low fields. This last feature should be particularly useful when the bipolar device goes into snapback mode since in this mode the base-collector junction will be in weak avalanche regime. This is the purpose of the study presented in the next section.

IV. EXPERIMENTAL VALIDATION

As we did not have a rectangular structure for comparison, the octagonal structure did not allow validating the impact of orientation on the triggering voltage and in the snapback mode. We then designed two specific test structures having exactly the same layout: one oriented along the flat and one rotated by 45°. The considered technology is a smart power technology and the test structure is a lateral NPN bipolar device. As shown on the schematic cross-section given in Fig.5, the NPN bipolar device is embedded into a P-well diffusion and has a symmetrical layout with the collector in the center of the structure.

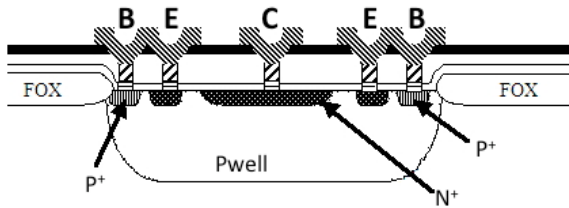


Fig. 5. Cross-section of the lateral grounded-base NPN bipolar structure used to assess the impact of crystal orientation.

To compare the two structures, we carried out DC measurement and Transmission Line Pulse (TLP) testing that allows extracting the quasi-static I-V

characteristic of the structure. We measured ten different packaged samples of each structure. Regarding the DC properties, we compared the breakdown voltage of the base-collector junction and no difference was observed between the two orientations. Similarly, under TLP testing, the two structures exhibited the same triggering voltage value, i.e. 10V. At low current, the TLP measurement resolution did not allow to distinguish a significant difference between the holding voltages. For both structures, it is around 8.5V and the holding current is in the range of 20 mA. However, we observed a significant impact at high current. The corresponding comparative measurement is shown in the plot of Fig.6.

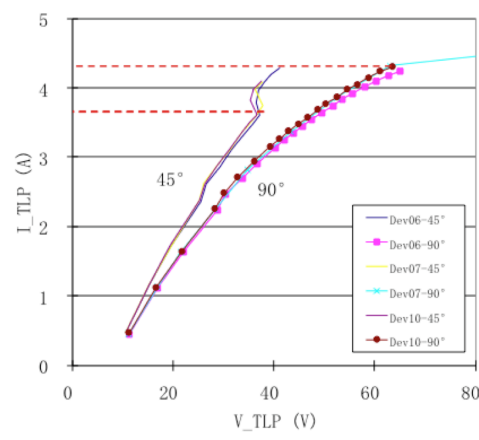


Fig. 6. Comparative high-current TLP measurement for 3 samples of the self-biased NPN bipolar structure for 2 orientations, 90° and 45°.

Firstly, it has to be noticed that the electrical characteristics are reproducible on the 3 samples of each structure. The very important result is that the on-resistance of the 45°-oriented structure is improved by about 30% compared to the 90° one. The on-resistance of the structure (8 Ω) is quite high since we just implemented a single finger and small area structure for the purpose of the study. The red dotted lines indicate the failure current, I_2 , of the components. Unexpectedly, the 45° structure with the lowest on-resistance has an earlier failure. Its current failure is 3.8A whereas the 90° one is 4.3A. This corresponds to an equivalent Human Body Model robustness of 6 and 6.6kV, respectively. The two structures have a different layout for the metal interconnexion between the pad and the emitter. This could explain an early current focalization in the 45° oriented structure and the resulting robustness difference. Anyway, both structures are very robust (≥ 6 kV) but the 45° oriented structure is the most appropriate to efficiently protect a circuit. Indeed, the voltage value corresponding to a TLP current of 3.6A is 37V for the 45° structure whereas it is 49V for the 90° one, i.e. a 12V difference.

The previous theoretical studies on the influence of crystallographic orientation on impact ionization were not validated with measurements [4] [5] [6]. Only the breakdown voltage of diodes was studied in function of crystal orientation and no clear evidence of any measurable impact could be demonstrated. Our study clearly shows that the crystal orientation has a significant impact on the ESD performance of a grounded-base NPN bipolar device. It also corroborates that the influence of crystal orientation is only effective under weak avalanche, i.e. at low electric fields.

VII. CONCLUSION

We experimentally validated for the first time that the performance of a grounded-base NPN bipolar protection device can be significantly improved by taking advantage of the impact of crystal orientation. 45° oriented structures that involve impact ionization in the <100> direction exhibit a significantly improved on-resistance compared the 90° ones related to the <110> direction. A 30% improvement was measured on the devices under study. This can be attributed to the lower threshold energy of electrons in the <100> direction. This offers a new option to

drastically improve the efficiency of NPN bipolar-based ESD protection structures.

REFERENCES

- [1] D. Trémouilles, G. Bertrand, M. Bafleur, N. Nolhier, L. Lescouzères, "Design guidelines to achieve a very high ESD robustness in a self-biased NPN", *EOS/ESD Symposium*, pp. 281-288, October 2002.
- [2] A. Gendron, C. Salamero, N. Nolhier, M. Bafleur, P. Renaud, P. Besse, "Deep Trench NPN transistor for Low-RON ESD Protection of High-Voltage I/Os in Advanced Smart Power Technology", *Bipolar / BiCMOS Circuits and Technology Meeting (BCTM'2006)*, pp. 226-229, October 2006.
- [3] D. Pogany, S. Bychikin, E. Gornik, M. Denison, N. Jensen, G. Groos and M. Stecher :, "Moving current filaments in ESD protection devices and their relation to electrical characteristics", *International Reliability Physics Symposium*, p. 243, 2003
- [4] C.L. Anderson and C.R. Crowell, "Threshold energies for electron-hole pair production by impact ionization in semiconductors", *Physical Review B*, vol. 5, n° 6, pp. 2267-2272, 15 March 1972.
- [5] I.K. Czajkowski, J. Allam, M. Silver, A.I. Adams and M.A. Gell, "Impact ionization thresholds in silicon and germanium under hydrostatic pressure and strain", *IEE Proceedings*, vol. 137, n°1, pp. 79-87, February 1990.
- [6] J. Bude, K. Hess and G.J. Iafrate, "Impact ionization: beyond the Golden Rule", *Semicond. Sci. Technol.*, vol. 7, pp. B506-B508, 1992.