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# Design Guidelines to Achieve a Very High ESD Robustness in a Self-Biased NPN

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**Abstract** - In this paper, using extensive TCAD simulations and measurement results, we analyze the basic mechanisms involved during an ESD stress in a self-biased NPN bipolar transistor used as an ESD protection. From the deep understanding of these mechanisms, we define design guidelines to achieve a very high ESD robustness (=10kV) in this type of device. These guidelines are validated on several CMOS technologies.

## I. Introduction

Electronic applications such as wireless or automotive require harsher and harsher ESD specifications. On some particular circuit pins, ESD robustness over 10kV is often specified, standard HBM specification being 2kV. To achieve such a high ESD robustness, insight into the basic ESD failure mechanisms of the ESD protection is necessary to support its design. 2D-electrothermal simulation is the perfect tool to reach this ambitious goal. In this paper, we focused our study on a self-biased NPN protection structure. The analysis of the behavior of a self-biased NPN of a smart power technology, with TCAD simulations, TLP and EMMI measurement, allows defining design guidelines for high ESD robustness. An important result of this investigation is that current focalization is a necessary condition for the self-biased NPN to efficiently absorb an ESD stress. These ESD design rules are successfully validated on two different CMOS technologies.

## II. Case of a vertical NPN with buried layer in a smart power technology

The structure we have thoroughly analyzed is a vertical NPN bipolar transistor from the library of a smart power technology [1]. The considered technology is a 1.8  $\mu\text{m}$  65V smart power technology. It combines a P-well CMOS technology with a variety of optimized vertical and lateral bipolar transistors as

well as both vertical and lateral DMOS power devices.

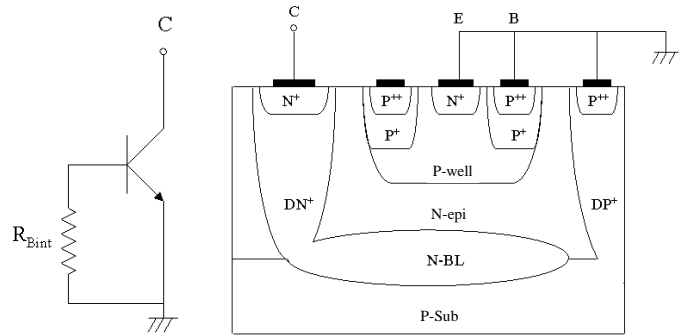


Figure 1: Electrical schematic and cross-section of the studied vertical self-biased NPN bipolar transistor.

Fig.1 shows the electrical schematic and cross-section of the NPN used as an ESD protection structure in this technology. The main characteristics of this device are a good current gain and a low on-resistance resulting from the presence of both a buried layer and a deep  $\text{N}^+$  diffusion. Two modifications are introduced in this device with respect to the standard one: use of a single base contact and of an emitter ballast resistance by increasing the spacing between emitter edge and contact.

When a negative ESD stress is applied to the collector of the NPN, it behaves as a forward biased diode. In this mode, the ESD robustness is high and there are no layout difficulties since the electric field is low. In the case of positive ESD stress, the NPN bipolar transistor is activated when the voltage on the collector electrode reaches the base-collector

breakdown voltage. The resulting avalanche current flowing through the internal base resistance then forward-biases the base-emitter junction and triggers the NPN bipolar transistor on. Once the NPN turns on, the avalanche and bipolar effects combine resulting in the decrease of collector voltage down to the snapback holding voltage. Depending on specific design rules and triggering configurations, this structure provides very good ESD robustness ranging from 3.5kV (26V per  $\mu\text{m}$  of total emitter length) to more than 10kV (75V/ $\mu\text{m}$ ) under positive HBM (Human Body Model) stress [2] and from 700V (5V/ $\mu\text{m}$ ) to 1300V (9.5V/ $\mu\text{m}$ ) under positive MM (Machine Model) stress [3].

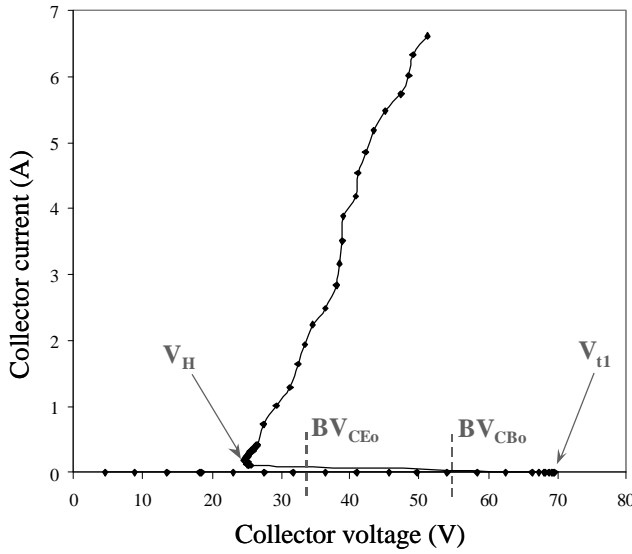


Figure 2: TLP and DC measurements for the NPN of Fig.1.  $BV_{CB0}$  and  $BV_{CE0}$  are measured at  $10\mu\text{A}$ .

We used Transmission Line Pulse testing to characterize this structure. As shown in Fig.2, the most striking feature is that the resulting snapback holding voltage ( $V_H$ ) is much lower than the measured  $BV_{CE0}$ , the common emitter breakdown voltage: it is 25V versus 32V for  $BV_{CE0}$ .

To understand this behavior, both 2D-simulation and emission microscopy (EMMI) experiments were carried out. The results of these investigations are summarized in a previous paper [1]. The main result is that, under low-level injection, the space charge of the reversed biased base-collector junction spreads out around the metallurgical junction, mainly into the collector side. The collector doping concentration,  $N_D$ , determines the collector-base junction breakdown voltage value  $BV_{CB0}$  as well as the common emitter breakdown  $BV_{CE0}$ .

With ESD current increase, the structure enters into high-injection conditions and Kirk effect occurs [4]. It can be noticed that this phenomenon is localized on the left side of the emitter (Fig.3). It results from the non-uniform base-emitter voltage induced by the base current flow. This effect is identical to current focalization described in power bipolar transistor [5]. Maximum electric field then moves from the metallurgical junction to the  $N^-/N^+$  buried layer boundary (Fig.3). As a result, the electric field is now sustained by a space charge mainly build-up by free carriers. The breakdown voltage of this equivalent “planar junction” is determined by an effective “doping” concentration  $N_{\text{eff}} > N_D$  in the range of the local electron density [6] [7]. As a consequence, the corresponding snapback holding voltage can be much lower than low current  $BV_{CE0}$  voltage value. This electrically initiated mechanism is the one involved in the current mode second breakdown of epitaxial bipolar power devices [8], failure resulting from the induced local heating (thermal second breakdown). However, the relatively short duration of the ESD stress ( $\sim 150\text{ns}$ ) does not result in a destructive heating and the previously described effect is very beneficial to the device since a lower snapback holding voltage leads to a globally lower power dissipation at the expense of a local heating. Failure analysis carried out using the Focus Ion Beam (FIB) technique confirmed that failure actually occurs at the  $N^-/N^+$  buried layer boundary [9].

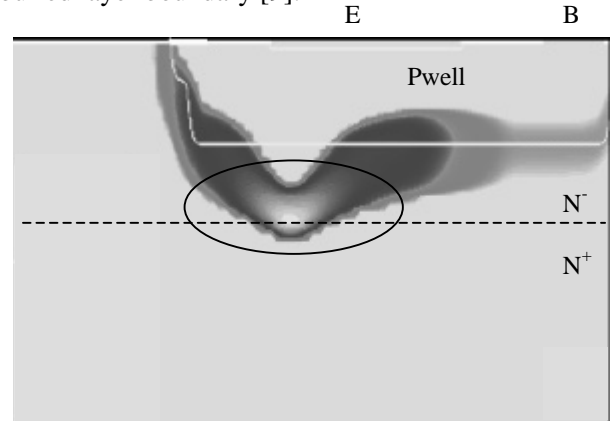


Figure 3: Simulated cross-section of the NPN showing impact generation rate at peak current under a 2kV HBM stress. Region of highest impact generation is circled.

### III. Design guidelines for a very high ESD robustness

This vertical NPN structure already provided a good ESD robustness. However, wireless and automotive applications are even more demanding and require ESD robustness above 10kV in HBM.

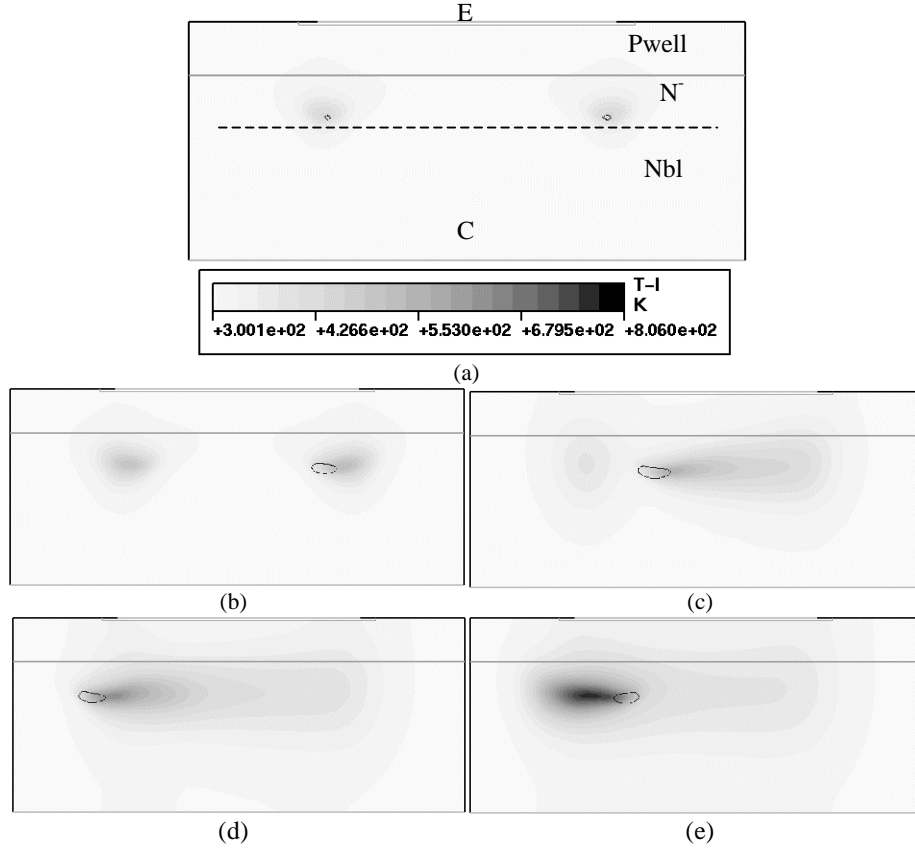


Figure 4: 2D-electrothermal simulation of a 500V HBM stress along emitter length. Temperature at (a) 10ns, (b) 20ns, (c) 45ns, (d) 70ns and (e) 90ns. In each figure, circled zone is current focalization location.

We then carried out a thorough study aimed at drastically improving the performance of the self-biased NPN. 2D-electrothermal simulations, based on analytical profiles resulting from calibrated process simulation, support this study. The cross-section of Fig.3 is along the emitter width. Since the current density during an ESD event is very high, Kirk effect is unavoidable except by increasing the total device size, which is not our goal. Current focalization is also unavoidable since the NPN bipolar transistor is self biased by the base-collector junction avalanche current, flowing below the emitter (from left to right on Fig.3), and them leading to non-uniform base-emitter voltage.

However, to achieve a high ESD robustness, it is also necessary to obtain a good current homogeneity along the emitter length. To study the current flow along the device length, we used a simplified structure of the NPN as shown in Fig.4.a. In this structure, there are 3 layers: the emitter with a heavy  $N^+$  doping, the collector with a graded doping and the P-type base in between. To avoid time consuming 3D-simulation, we chose to perform a 2D-simulation in open-base

condition. This approximation is valid in the high current regime.

When the structure undergoes an ESD stress and enters the high current regime, the emitter acts as an electron injector characterized by its injection efficiency, which determines the transistor current gain. As described above, the collector behaves as a hole injector since the base-collector junction sustains an electric field high enough to induce avalanche injection. This hole injection is controlled by the avalanche coefficient  $M$ . These two strongly coupled multiplication mechanisms, bipolar effect and avalanche injection, induce current focalization and finally thermal second breakdown. This coupling is directly proportional to the effective base width in the high current regime.

We performed 2D-electrothermal simulation of a 500V HBM stress (Fig. 4 and 5) on this simplified structure using the same technology parameters as the NPN device in Fig.3. The obtained result is that, even though in this case the base-emitter voltage is uniform, current focalization, starting at the edges of the emitter occurs in the same way as in Fig.3. However, during the ESD transient, its location

moves along the whole length of the device as shown by the cross-sections of Fig.4 at different times of the stress : 10, 20, 45, 70 and 90 ns. This behavior that homogenizes the power dissipation, can be explained by the negative temperature feedback of the avalanche phenomenon (Fig.6).

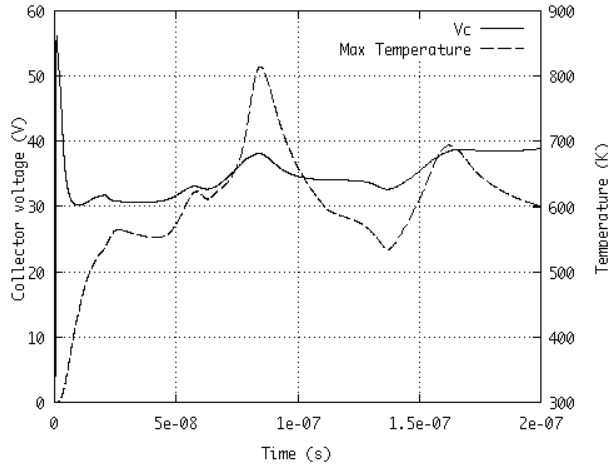


Figure 5: Collector voltage and maximum temperature evolution during 2D-electrothermal simulation of a 500V HBM stress along emitter length.

The high electric field and current density in the hot spot lead to a local temperature increase in its center. The resulting decrease of ionization coefficient induces a displacement of the maximum current density to the coolest edge of the hot spot, resulting in its apparent movement to a lower temperature region.

Most of the physical models used in TCAD simulator are only valid up to 600K, although extreme temperature is reached during ESD events. Consequently we performed simulation for relatively low ESD current, leading to a temperature rise compatible with TCAD simulator.

There is no easy way to experimentally verify this physical mechanism. Uniformity of the current distribution is generally observed in such devices either by laser interferometry [10] or emission microscopy [1]. This is not in contradiction with the simulation results since these two measurements setup do not directly account for the current density. Experimental results, using a laser interferometric thermal mapping technique, have been carried out by Pogany et al [10] on triggering instabilities and triggering behavior of protection devices in smart power technology. The authors defined a temperature spreading rate which is in order of  $1\mu\text{m}/\text{ns}$ . In our simulations this spreading rate is in the same order of magnitude. This corroborates the simulation validity.

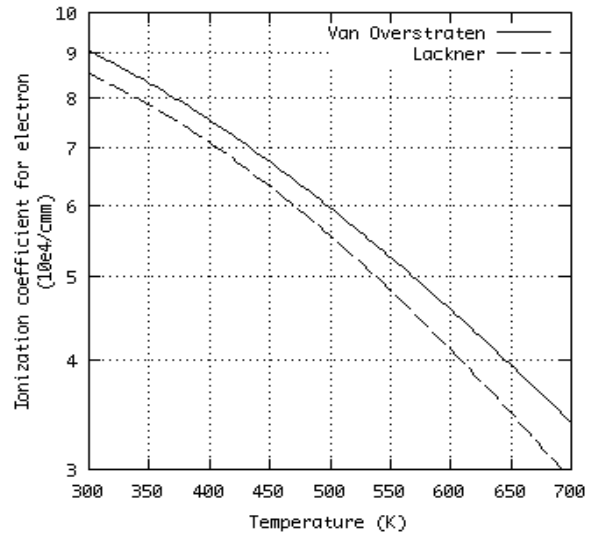


Figure 6: Temperature dependence of the ionization coefficient for electron at  $E=6e5$  V/cm

It can be concluded that, when an ESD stress is applied to a self-biased NPN, current focalization always occurs and the ESD robustness depends on the ability of the hot spot location to move to a cooler location along the whole device length. Therefore, at any time, the structure is at the onset of thermal second breakdown.

An efficient way to delay this fatal event is to reduce the strong coupling between the emitter current and the avalanche injection. Widening the high current effective base width ( $W_{\text{Beff}}$  Fig.7) of the device is the best way to achieve a significant decoupling effect as shown in Fig.7.b and Fig.8. For these simulations, only half of the device length is simulated and thermal analysis is turned off to reduce computation time. In both case, high and low coupling (HC and LC), collector current focalization occurs in the same way (Fig.7) at the N/Nbl boundary. There is no displacement of the “hot spot” (current density x electric-field product:  $J \cdot E$ ), however, the current distribution over the emitter length is significantly improved (Fig.8). As a result, the hot spot can move more freely under the negative temperature feedback of the avalanche phenomenon, described above. It has to be noticed that this design only induces a slight increase (few percents) in the snapback holding voltage value (Fig.9)

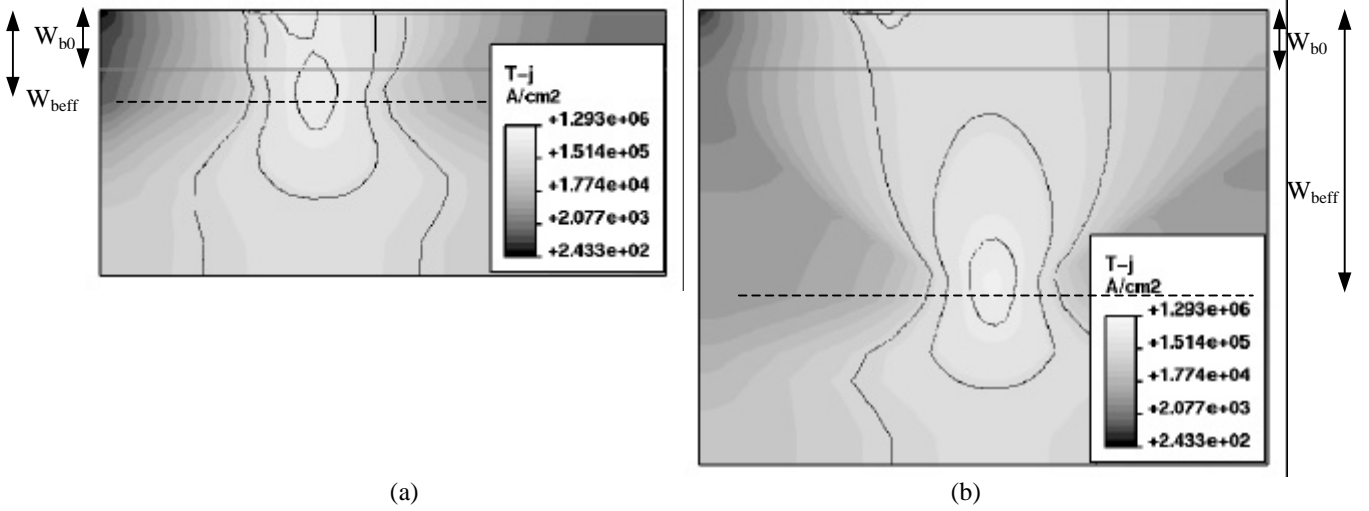


Figure 7: 2D-electrical simulation of effective base width influence on decoupling emitter injection and avalanche generation. Vertical and horizontal scale are the same for figures a and b, only varied parameter is the epi-layer thickness. Current density is plotted for (a) High coupling (HC) and (b) Low coupling (LC).

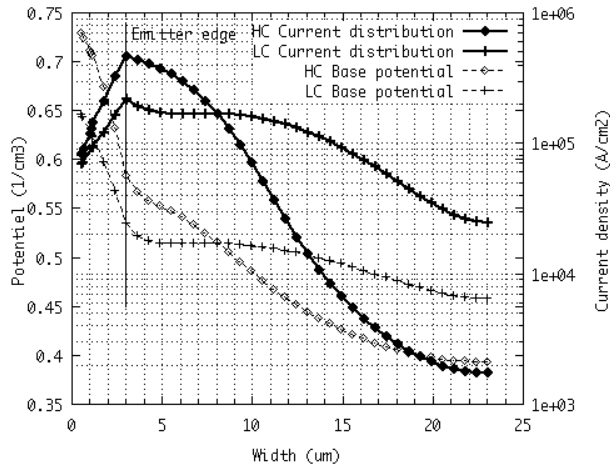


Figure 8: 1D cutline of current density and potential into the base below the emitter for low coupling (LC) and high coupling (HC) cases.

This design rule cannot be implemented in a vertical NPN without technology changes: it requires an increase of the epi-layer thickness. Using a lateral NPN helps circumvent this drawback. In addition, this design rule induces a significant increase of the NPN triggering voltage  $V_{t1}$ : in this particular case, it goes from 65V to 200V according to the simplified simulation (Fig.9). However, design solutions makes possible the use of this modified NPN either by implementing an appropriate triggering scheme or associating it to a secondary stage.

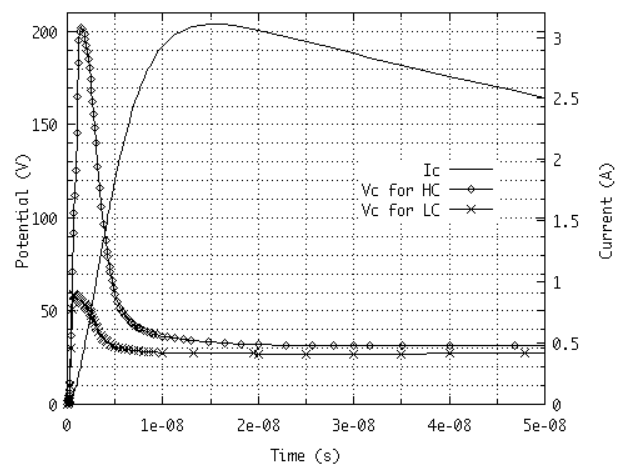


Figure 9: Collector voltage vs. time during a 2kV ESD event in the high coupling (HC) and low coupling (LC) cases (simulation results).

Widening the effective base width of the device allows improving the emitter current homogeneity. In the same way, using a heavier doping for the base layer homogenizes the base-emitter voltage. This positive effect was validated in the smart power technology. Furthermore the decoupling of bipolar action and avalanche generation allows delaying thermal runaway associated with second breakdown.

Another important parameter, for improving the robustness, is the collector profile between low doped ( $N^-$  in Fig.4a) and highly doped region ( $N_{bl}$  in Fig.4a). The abrupter the profile, the lower is the snapback holding voltage. In figure 10, simulation results, along the emitter length, of an imaginary structure with an abrupt buried layer profile is compared with the reference structure of Fig.4a. The

abrupt layer depth has been adjusted in such a way that the effective base width is close to the reference one.

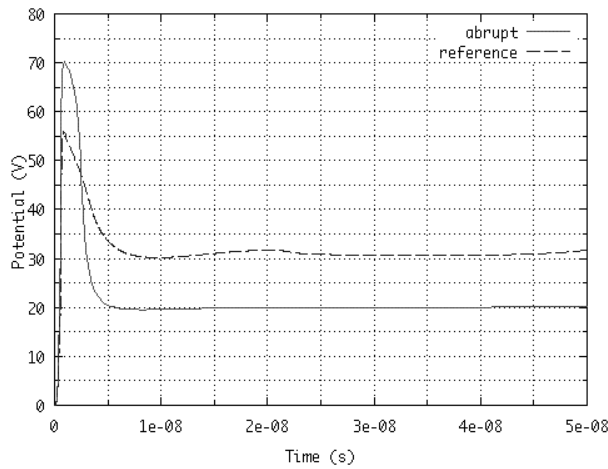


Figure 10: Collector voltage vs. time during a 2kV ESD event for a graded (reference) and abrupt collector doping profile (simulation results).

The snapback holding voltage decreases by ten volts while the dynamics of the hot spot is not modified. The holding voltage decrease is due to the modification of the space charge profile in the collector high electric field region. As shown in figure 11 and 12, we can define an effective collector base junction (Ebcj line), which corresponds to the maximum electric field.

In the abrupt case, the negative space charge (left side of the Ebcj line in Fig.11) is mainly built by electron carrier and the positive one (right side of the Ebcj line in Fig.11) by ionized donor impurities. This leads to an equivalent abrupt profile and a sharp electric field (Fig.11).

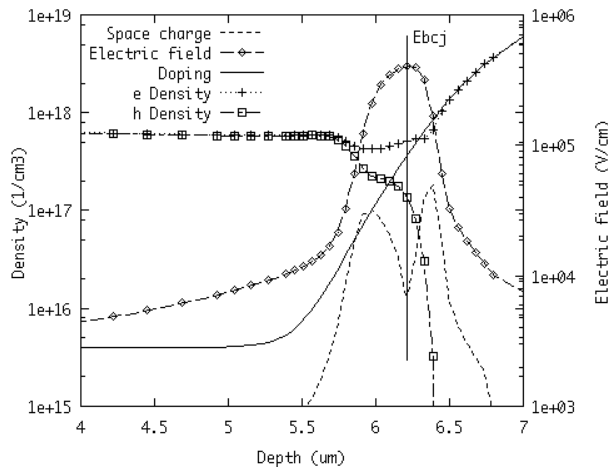


Figure 11: Simulated electric field and space charge profile in the collector, during high current regime, for an abrupt doping profile. Ebcj line represents the effective base collector junction.

For a graded doping profile the positive space charge is still generated by ionized donors while the negative results from the difference between electron density and ionized donors, leading to a graded and lower doped equivalent junction. The resulting electric field is smoother than in the abrupt profile case (Fig.12) and the breakdown voltage of this junction is higher than in the abrupt case.

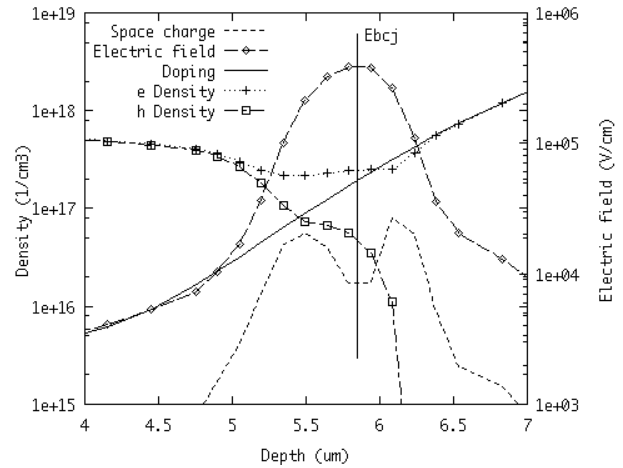


Figure 12: Simulated electric field and space charge profile in the collector, during high current regime, for a graded doping profile. Ebcj line represents the effective base collector junction.

Mergens [11] also described the phenomenon of strong snapback in LDMOS devices. Actually, the snapback holding voltage depends on the breakdown voltage of the effective base collector junction (located by Ebcj lines in Fig.11 and Fig.12). As shown, this breakdown voltage is a function of the collector doping profile between its  $N^-$  and  $N_{bl}$  region. As a result, DC breakdown voltage of the base collector junction depending on the base doping and collector  $N^-$  doping does not determine the snapback holding voltage. The DC breakdown voltage can be very high while the snapback holding voltage can be very low resulting in an "extraordinary 'strong' snapback" [11].

An abrupt doping profile between lower and highly doped collector region reduces the snapback holding voltage and lower the global energy dissipated in the device, that allows higher ESD robustness.

This last enhancement associated with the use of an enlarged effective base width, which is supposed to delay thermal second breakdown, leads to a significant improvement of the ESD robustness of a self-biased NPN. This is experimentally shown hereafter for two different technologies.

## IV. Experimental results

These design rules were successfully implemented in NPN-based ESD protection structures in two different technologies:

- A 1.7 $\mu\text{m}$  analog CMOS technology with up to 20 mask levels allowing to build low and high voltage CMOS, LDMOS power transistor, capacitors and bipolar transistors.
- A standard 0.6 $\mu\text{m}$  CMOS technology.

For the analog CMOS technology, the structure resulting from the previously defined design guidelines is given in Fig.13. It is a vertical NPN device with a double emitter and a central base contact.

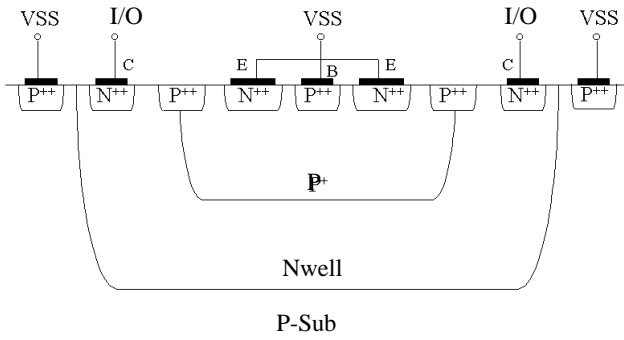


Figure 13: Self-biased NPN used as an ESD protection structure in an analog CMOS technology (not to scale).

The base layer is a PHV layer, which has a higher doping than the P-well of the CMOS devices. The collector is the N-well of the CMOS devices. This layout arrangement allows the avalanche generation to be located at the inner edge of the N+ collector contact (Fig.14) in high current regime.

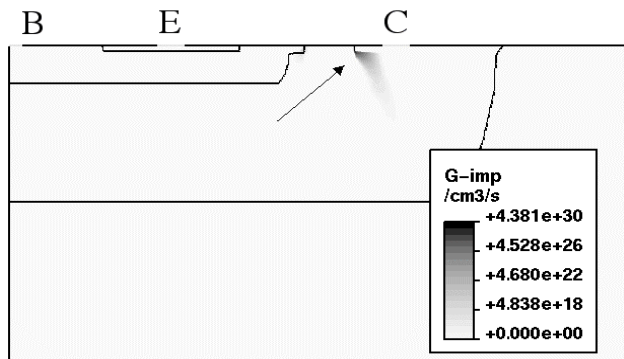


Figure 14: Maximum avalanche generation rate location at peak current of an ESD event in the improved NPN structure of the analog CMOS technology.

The layout of this device is such that vertical operation is favored. As shown in Fig.15 the current flows vertically below the emitter, down to the Nwell

layer and comes back up to the N+ collector contact diffusion.

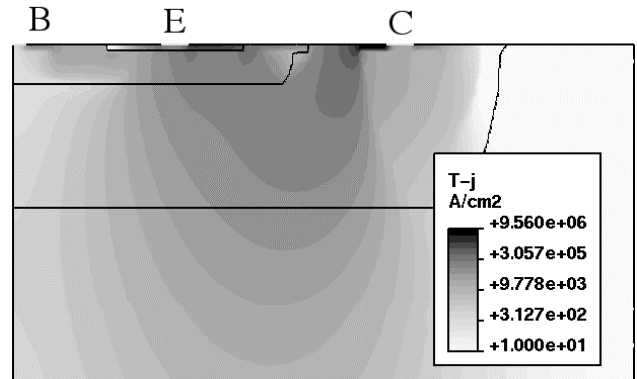


Figure 15: Current density at peak current of an ESD event in the improved NPN structure of the analog CMOS technology.

This structure results in an HBM ESD robustness of 12kV, that is 175V per  $\mu\text{m}$  of total emitter length to be compared to the 75V/ $\mu\text{m}$  obtained with the NPN structure of Fig.1. As shown by the TLP measurement of Fig.16, the decoupling between emitter efficiency and avalanche phenomenon, obtained by enlarging the effective base width in the high current regime, induces a significant increase of the trigger voltage: from the 22V of the base-collector breakdown voltage up to 51V. However, the subsequent strong snapback and the low on-resistance allow absorbing high energy ESD stresses.

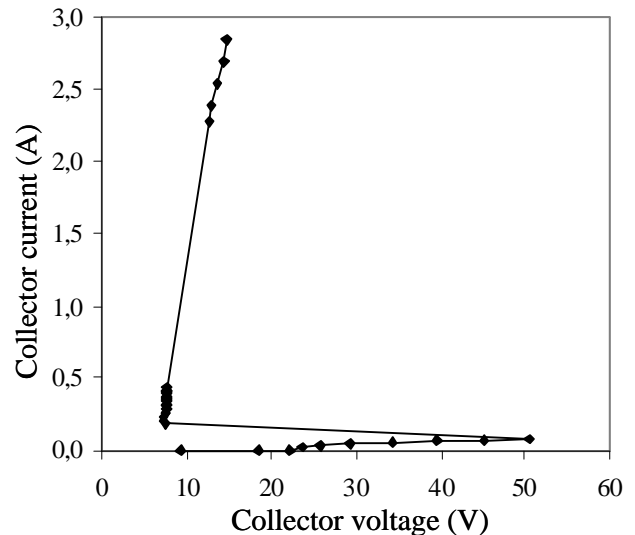


Figure 16: TLP measurement of the improved NPN structure of the analog CMOS technology.

This structure was successfully implemented as an input ESD protection in a commercial analog circuit. Its high triggering voltage required using it as the primary stage of a two-stage protection structure.



In the same manner, these design guidelines were used to design a self-biased lateral NPN in a standard 0.6 $\mu$ m CMOS technology. This allowed providing the technology with a 5kV ESD robustness structure compared to the 1.5kV guaranteed by the silicon foundry.

## V. Conclusion

Thorough analysis of the physical mechanisms involved in a self-biased NPN helped define high ESD robustness design guidelines. The most striking result is that, current focalization always occurs in such devices as part of the self-biasing mechanism and temperature homogeneity is obtained through a rapid movement of the hot spot. To improve the ESD robustness, this current focalization has to be controlled in such a way that second breakdown destruction is delayed. This is obtained through an efficient decoupling between the emitter current and the avalanche injection phenomenon. The resulting design guidelines are successfully applied to two different CMOS technologies. In the analog CMOS technology, ESD robustness as high as 175V per  $\mu$ m of emitter length is obtained.

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## REFERENCES

- [1] G. Bertrand et al, "Analysis and Compact Modeling of a Vertical Grounded-Base NPN Bipolar Transistor used as an ESD Protection in a Smart Power Technology", IEEE Journal of Solid State Circuits, Volume 36, Issue 9, pp. 1373 -1381, September. 2001.
- [2] JEDEC Standard, "Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)", JESD22-A114-B, June 2000.
- [3] EIA/JEDEC Standard, Test Method A115-A, "Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)", EIA/JESD22-A115-A, October 1997.
- [4] C. T. Kirk, Jr, "A theory of transistor cutoff frequency (fT) falloff at high current densities", IRE Trans. Electron Device, vol.ED-9, pp.167-174, Mar. 1962.
- [5] P. Leturcq, "Power bipolar transistor: a survey", Proc. Fourth Brazilian Workshop on Microelectronics, pp 275-300, March 1983.
- [6] R. Rossel et al, "Avalanche Characteristics of MOS Transistors", Proc. 21th International Conference on Microelectronic (MIEL), Nis (Yugoslavia), pp 371-381, 1997.
- [7] P.L. Hower et al, "Avalanche injection and second breakdown in transistors", IEEE transaction on Electron Devices, Vol. ED-17, n°4, April 1970.
- [8] H.B. Grutchfield and T.J. Moutoux, "Current mode second breakdown in epitaxial planar transistors", IEEE Transactions on Electron Devices, vol. ED-13, n°11, pp. 743-748, November 1966.
- [9] C. Delage et al, "The mirrored lateral SCR (MILSCR) as an ESD Protection Structure : design and optimization using 2D device simulation", IEEE Journal of Solid-State Circuits, vol. 34, No. 9, pp. 1283-1289, September 1999.
- [10] D. Pogany et al, "Study of trigger instabilities in smart power technology ESD protection devices using a laser interferometric thermal mapping technique", EOS/ESD Symposium, 2001.
- [11] M. Mergens et al, "Analysis and compact modeling of lateral DMOS power devices under ESD stress conditions", Proc. EOS/ESD Symp. 1999, Orlando (USA, pp. 1-10), 1999.