



M. Sevaux
A. Rossi
K. Sörensen

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Intel's predictions
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Electronic design

a new field of investigation for large scale optimization

Marc Sevaux André Rossi Kenneth Sörensen

University of South Brittany
UEB – Lab-STICC – Lorient, France

University of Antwerp
Faculty of applied economics – Antwerp, Belgium



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Electronic devices are everywhere

Let's count. . .

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Electronic devices are everywhere

Let's count. . .

- ▶ How many mobile phones in the room, now?
Maybe counting the people who don't have one is easier
- ▶ How many laptops?
- ▶ How many digital camera?
don't forget the combined devices ;-)
- ▶ How many cords and power units in your hotel room?
- ▶ . . .

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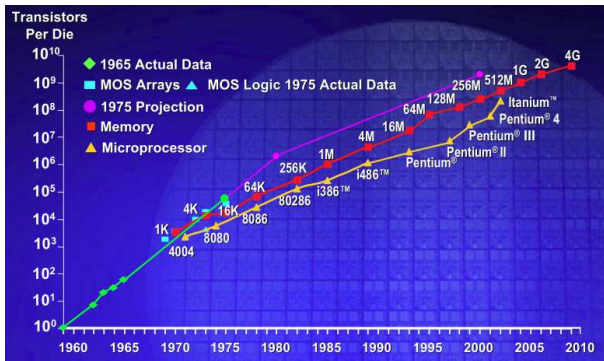
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Moore's law

In 1965, Gordon Moore, co-founder of Intel

predicted that the number of transistors per square inch on integrated circuits will double every year.





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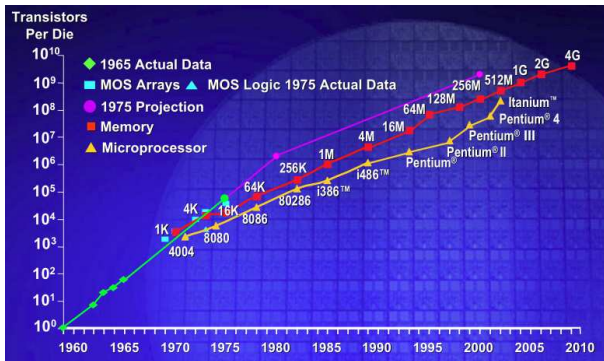
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Moore's law

In 1965, Gordon Moore, co-founder of Intel

predicted that the number of transistors per square inch on integrated circuits will double every year.



It will not be true anymore. . .



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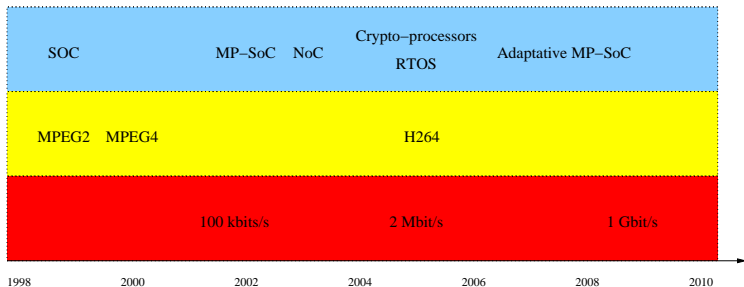
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Increasing needs and means

Demand and needs are constantly increasing

- ▶ increase in throughput
- ▶ increase in complexity
- ▶ and change in design strategies



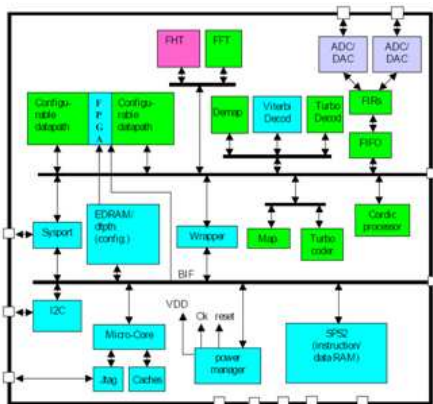


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FPGA (2003) : Multistandard circuit WLAN

Main features

- ▶ Bus hierarchy
- ▶ IP-based concept



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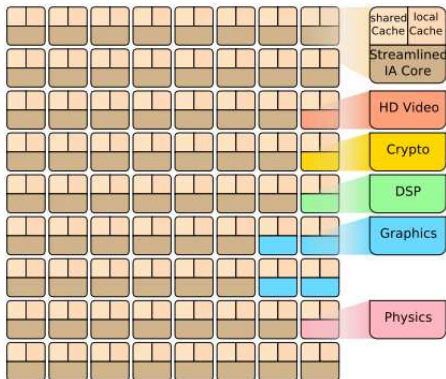
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Adaptive MPSoC (2007) : Intel TeraScale

Main features

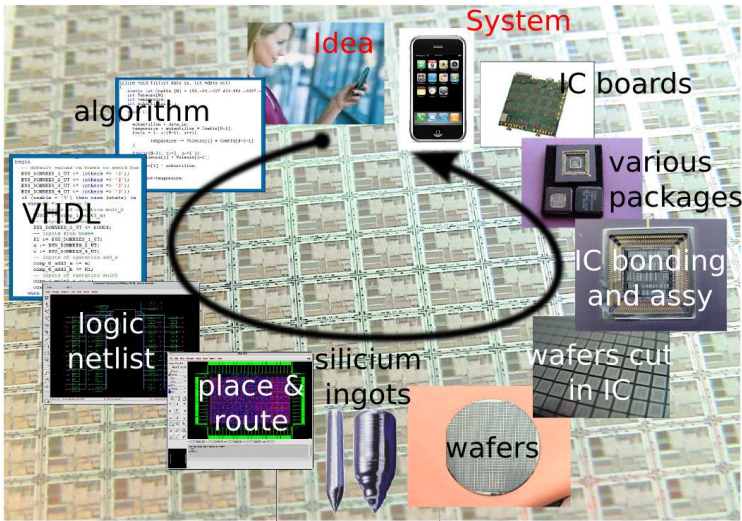
- ▶ change to all-processor
- ▶ dedicated processors
- ▶ communication network



How does it work?



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What can we do?

What is **operations research** doing there?

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What is **operations research** doing there?

- ▶ optimization is needed at every step of the design process
- ▶ methods are known ([meta]heuristics, ILP)
- ▶ very badly implemented and used
- ▶ we have to interfere



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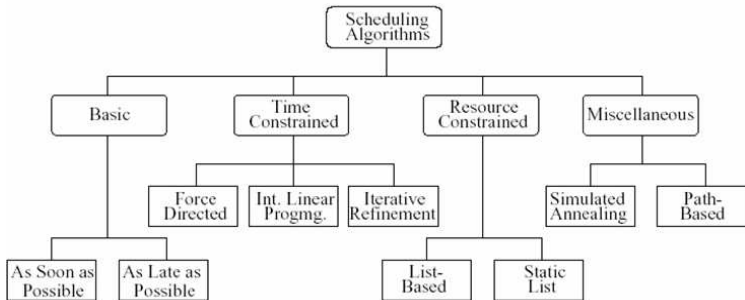
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It's time to help

Even if they use optimization methods, look at this...





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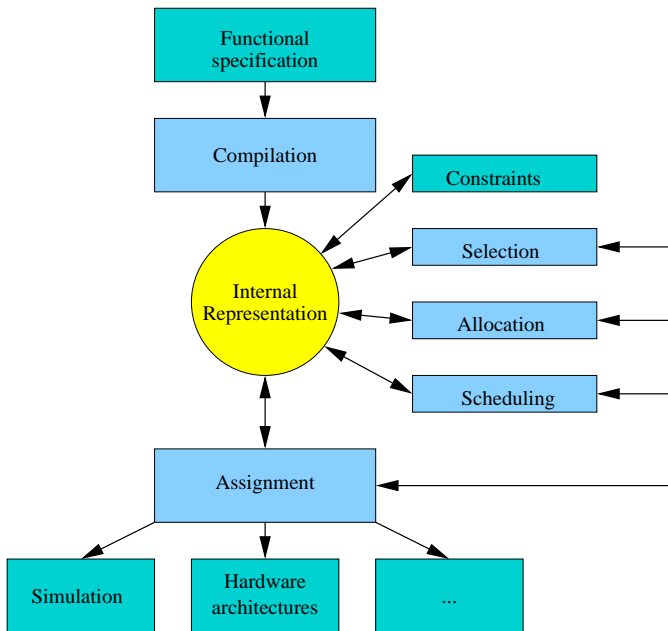
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Synthesis flow





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Memory allocation

Build $2a + b$ and $2d + c$ with two adders in parallel

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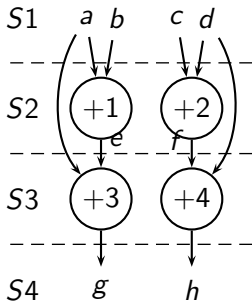
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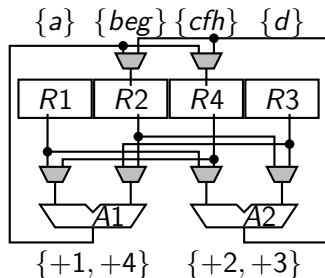
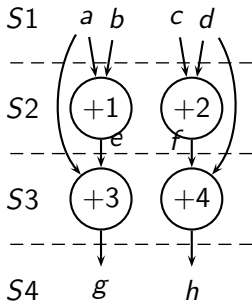
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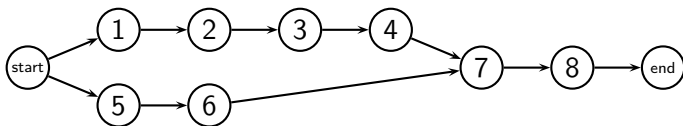
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And pipeline



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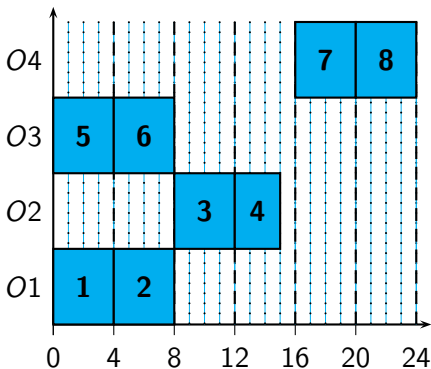
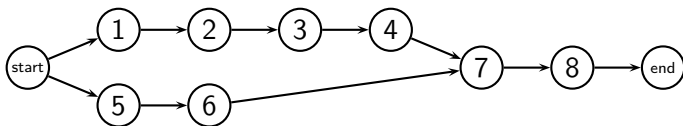
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Methods for HLS

We have developed

- ▶ MILP
but limited in size and constraints
- ▶ VNS
 - ▶ several neighborhoods
(assignment of variables/operators, scheduling order)
 - ▶ descent method as local search
- ▶ GRASP
 - ▶ based on MLEA (semi active schedules with minimum of registers)

A Tabu Search implementation, instead of descent method, and an effective version of the GRASP is still under improvement



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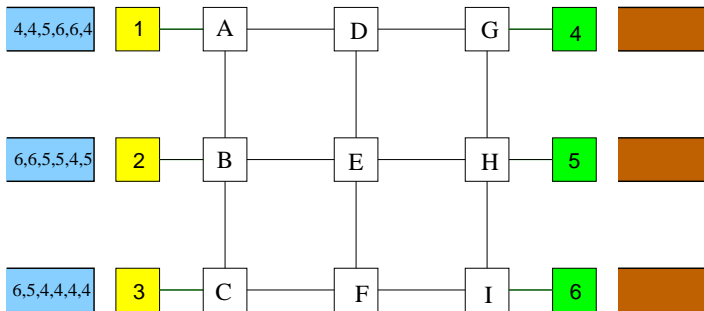
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Network on Chip

IPs or Processors communicate through the NoC

Data are contained in FIFOs and should be sent to specific destinations

An edge can be occupied with only one data at a time

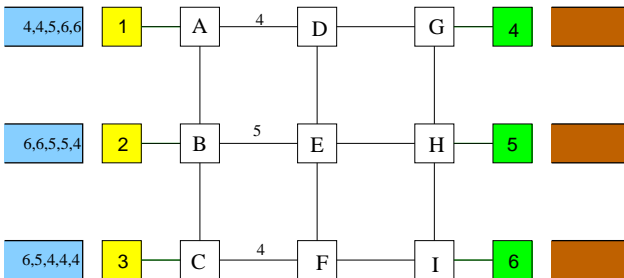




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A simple example

Packets from left should be sent to IP on the right
A shortest path algorithm is used for packets



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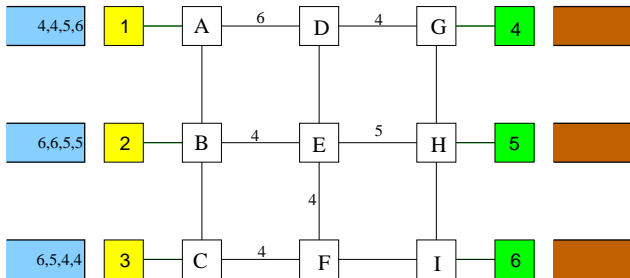
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A simple example (cont'd)

SSP are increasingly computed for each packet



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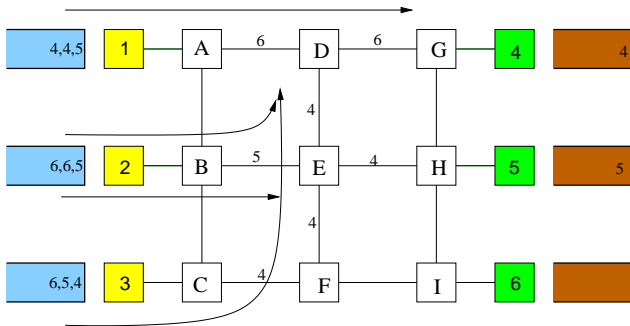
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A simple example (end)

And now comes the real trouble!!!



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A first heuristic

Consider that FIFOs' sizes inside routers are infinite

1. Take the first available packet
2. Compute its shortest path to destination
3. For each time instant (click), consider that an occupied edge is a unitary resource (or is not anymore in the graph for the other packets)
4. Go back to step one until all packets are handled



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Return from practitioners

- ▶ Excellent results
- ▶ Simple to implement and put in embedded systems
- ▶ Ignored constraints: FIFO size, order of packets, ...
- ▶ But can used for a more elaborate hybrid algorithm



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Memory allocation

- ▶ Allocating variables in memory banks
k-weighted graph coloring problem

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Memory allocation

- ▶ Allocating variables in memory banks
k-weighted graph coloring problem

Problem : which data should be assigned to which memory bank to minimize the conflicts when accessing data?

- ▶ conflict graph $G = (V, E)$
- ▶ nodes $V \rightarrow$ data
- ▶ edges $E \rightarrow$ conflicts
- ▶ weight $w_{i,j} \rightarrow \#$ memory access to conflicting data
- ▶ k colors $\rightarrow k$ memory banks

Knowing k , the number of colors, which color to assign to which node to minimize the sum of weights of conflicting edges?



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Problem size and Extensions

General problem size

- ▶ Graph
Nodes: 1 000 – 10 000
Density: 50% – 80%
- ▶ Colors
 $k \in [2, 100]$



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Problem size and Extensions

General problem size

- ▶ Graph
Nodes: 1 000 – 10 000
Density: 50% – 80%
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 $k \in [2, 100]$

Extensions

- ▶ Memory bank capacity
- ▶ Additional cost for distant memory banks
- ▶ DA-system for Decision-Makers in conception
- ▶ RAM pages (another problem?)



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Power consumption

Remark

Power consumption partially depends on wire length

It concerns

- ▶ HLS and final design
- ▶ NoC and path for packets
- ▶ Memory assignment
and distance from memory banks to processors
- ▶ ...

Take it into account from the very beginning



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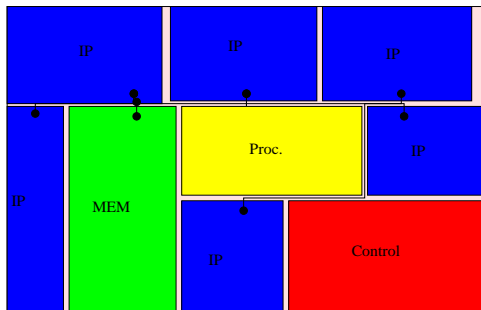
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Location-Routing problems

Before solving the routing problem in the NoC

- ▶ The NoC itself should be built
- ▶ Placement constraints are important
- ▶ Time span and total data are basis of the constraints





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Multiojective optimization

Customers want to

- ▶ increase battery life
- ▶ have smaller devices
- ▶ with more functionalities

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Multiobjective optimization

Customers want to

- ▶ increase battery life
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Electronic device designers want to

- ▶ reduce their costs
- ▶ meet customer needs
- ▶ reduce the time-to-market



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- ▶ with more functionalities

Electronic device designers want to

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- ▶ meet customer needs
- ▶ reduce the time-to-market

All are conflicting objectives

- ▶ silicon (surface)
- ▶ power consumption
smaller batteries and more functionalities!



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Strong hypothesis are made: everthing is **deterministic!!!**

- ▶ but there are malfunctions
- ▶ so increase of redundancy (in networks)
- ▶ methods are added for reliability, security, cryptography. . .



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Strong hypothesis are made: everthing is **deterministic!!!**

- ▶ but there are malfunctions
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- ▶ methods are added for reliability, security, cryptography. . .

Why all of that?

- ▶ heavy ions in embeded systems (satellites)
- ▶ miniaturisation → electron loss
- ▶ complex systems → “GALS”
Globally Asynchronous Locally Synchronous
- ▶ DRAM access, variable reading time
 - depending on preceding operations
 - depending on cache, on HDD



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Consequences

At the circuit level

- ▶ if $p'_i > p_i$ sampling at time p_i is wrong
- ▶ register reading not complete
- ▶ **error**: system unstable
- ▶ DM should make the synthesis again. . .



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At the NoC level

- ▶ communication delays should be added
- ▶ data are not always predictable
- ▶ stochastic or sampling models should be used



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At the NoC level

- ▶ communication delays should be added
- ▶ data are not always predictable
- ▶ stochastic or sampling models should be used

At the conception level

- ▶ the final chip/circuit might have bad areas
- ▶ like bad cluster in HDD, but no software layer



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What's next?

Intel's top ten technology predictions for next decade

1. New classes of portable devices with ten times more battery life
2. Low-cost silicon photonics for faster, more reliable data transmission
3. New heights of realism in visual computing
4. Realistic computer generated images
5. Malware will become a thing of the past
6. Personal internet devices will be truly personal
7. Interactive computing devices make 'composable computing' a reality
8. Next-generation TV will not be about pixels
9. Seamlessly connected 3-D worlds
10. A spectrum revolution is looming



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A. Rossi
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Increasing the collaborations

To be efficient we need to

- ▶ create as many contacts as possible
- ▶ collaborate more with the electronic community
- ▶ do not let them do it badly
- ▶ have more OR people involved
- ▶ publish in the electronic journals



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It is time to start a real network

1. exchange students
2. give seminars/tutorials for the electronic community
3. meet regularly
4. get financial support from the institutions
5. and...



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It is time to start a real network

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5. and... why not start a European project?



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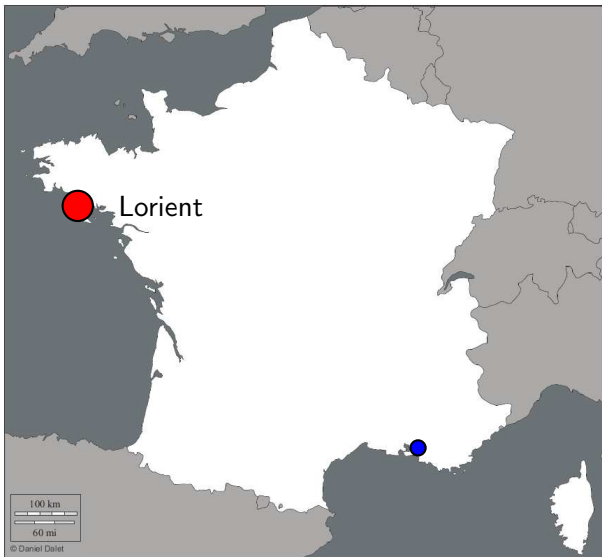
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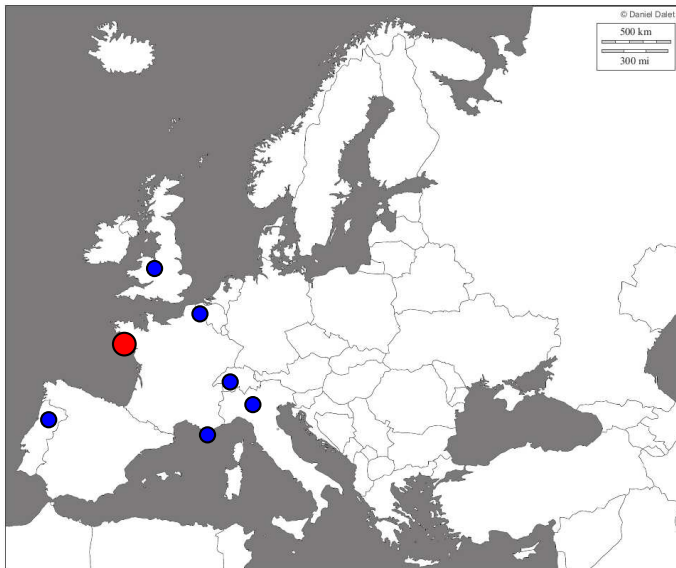
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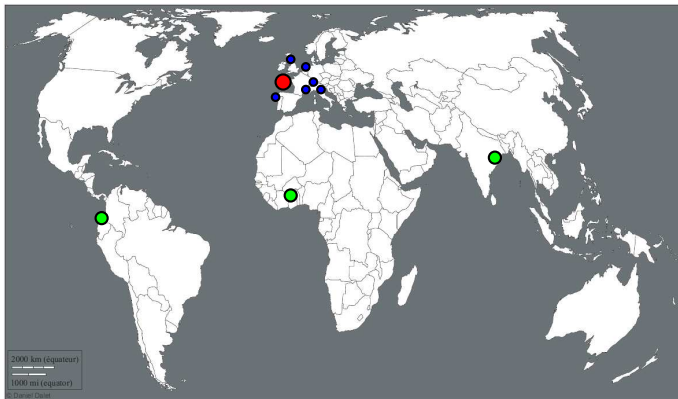
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Electronic design

a new field of investigation for large scale optimization

Marc Sevaux André Rossi Kenneth Sörensen

University of South Brittany
UEB – Lab-STICC – Lorient, France

University of Antwerp
Faculty of applied economics – Antwerp, Belgium



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