



**HAL**  
open science

# Integrated Design of MEMS: Designing Manufacturable Products

Matthieu Museau, Cédric Masclet

► **To cite this version:**

Matthieu Museau, Cédric Masclet. Integrated Design of MEMS: Designing Manufacturable Products. MIT'05, 8th International Conference on Management of Innovative technologies; Org. Laboratory for Alternative Technologies, Sep 2005, Fiesa, Slovenia. hal-00375196

**HAL Id: hal-00375196**

**<https://hal.science/hal-00375196>**

Submitted on 10 Jul 2023

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# Integrated Design of MEMS Designing Manufacturable Products

M. Museau, C Masclet

*3S laboratory, Grenoble, France*

## Abstract

This paper is a first attempt to qualify the design process in the field of MEMS product. Through this study, we try to analyse how the issue of manufacturability is addressed. This imply to understand specificities of the manufacturing process involved in the realization of these products (we focus on process derived from electronic industry). Then we look at the main design methodologies to understand how the manufacturing can be taken into account. Computer aided tools associated to these methodologies are presented at the same time. Finally, we conclude on the need of specifications for a design methodology that would provide designers with greater independence from manufacturing constraints

**Keywords:** MEMS, DFM, manufacturing constraints, design methodology.

## 1 Introduction

MEMS (MicroElectroMechanical Systems) are small components build of both electronical and mechanical parts. Their size (whole or part) range from few micrometers to millimeters. A detailed taxonomy of microproducts can be found in [1]. Few MEMS are already integrated in mass-market product (automotive, cellular phones, ink-jet printers, PDAs...) but major possible applications are still to come.

MEMS are fundamentally multidisciplinary devices and so the design teams. Hence, designers from differents disciplinary need to communicate efficiently, but also have to collaborate with manufacturing experts. This last point is all the more sensitive since micro-manufacturing process are often not familiar to the designer in charge of the mechanical part. This lack of knowledge combined with R&D context involve, most of the time, traditional design approach for new products, based on "top-down" methodologies. This approach don't support collaborative design and implies many "build and test" iteration which increase time to market and product costs. In this paper we'll try to describe design methodologies that are advocated to deal efficiently with the problem of manufacturability.

Next section is dedicated to a brief overview of the most representative manufacturing processes in order to have a better knowledge of what kind of constraints the designer have to deal with.

## 2 MEMS manufacturing processes

The main manufacturing processes used in the micromachining of MEMS are derived from the silicon industry. So, all electronic and mechanical parts are realized at the same time. Indeed, processes must be compatible with Very Large Scale Integration (VLSI) technologies : for instance, during the manufacturing sequence, temperature should not exceed certain value to avoid alteration of electronical parts. In general, multiphysics aspect with strong coupling at this scale level will greatly influenced the design process [2].

MEMS are build from silicon wafers by a sequential process consisting in stacking up layers of materials with appropriate geometries. Thus, the third dimension is not achieved in one step but result from the whole sequence. The manufacturing operations are based on whether chemical or physical principles applied to the wafers. They can be broadly divide in three main processes which are : additive processes, selective processes and etching processes. Patterns are created on the surface or in the bulk of the silicon wafer by selecting thin films previously deposited and then etching processes remove material which has been selected. The organization of these three processes constitutes a step of the global manufacturing process and one of the difficulties in MEMS manufacturing is to organize those steps in a manufacturing sequence. Indeed, processes

used in a step should not deteriorate material previously deposited, selected and etched.

## 2.1 Additive processes

The first building block in MEMS processing is addition of thin films of material with thickness between a few nanometer to about 100 micrometer. Additive technologies can be classified in two groups : addition that happen because of a chemical reaction or because of a physical reaction.

### 2.1.1 Chemical Reaction

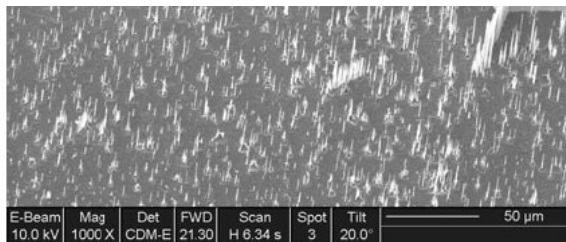
These processes exploit the creation of solid materials directly from chemical reactions in gas and/or liquid compositions or with the substrate material. The main processes are Chemical Vapor Deposition, Electrodeposition, Epitaxy and Thermal oxidation.

**Chemical Vapor Deposition (CVD)** The substrate is placed inside a reactor to which a number of gases are supplied. A chemical reaction takes place between the source gases and produces a solid material with condenses on all surfaces inside the reactor, including the substrate. The two most important CVD technologies in MEMS are:

**Low Pressure CVD** produces layers with excellent uniformity of thickness and material characteristics and deposit films on both side of at least 25 wafers at a time but the deposition temperature is higher than 600°C.

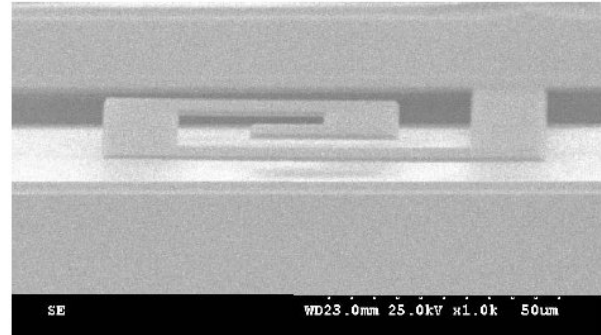
**Plasma Enhanced CVD** can operate at lower temperature (down to 300°C) but the quality of the films tend to be inferior to LPCVD processes. Moreover, most PECVD processes can only deposit the material on one side of the wafers on 1 to 4 wafers at a time.

A variety of materials can be deposited with CVD technologies, however, some of them are less popular with fabs because of hazardous byproducts formed during the chemical reaction (figure 1)



**Figure 1** Example of bi-product "grass" formed by CVD process.

**Example :** Thick and smooth amorphous Si film of 2 μm without hillocks has been obtained at low temperature of 300 °C by PECVD technology [3]. Fabrication of suspended MEMS microstructure are thus accessible (figure 2)



**Figure 2** Suspended Si microstructure.

**Electrodeposition.** The substrate is placed in a liquid solution (electrolyte) and need electrical potential to provide a chemical redox resulting in a formation of a layer of material on the substrate. This process is typically restricted to electrically conductive materials and it is well suited to make films of metal such as gold, copper and nickel. The films can be made in any thickness from ~1μm to >100μm.

**Epitaxy.** If the substrate is an ordered semiconductor crystal (i.e. silicon, gallium, arsenide), it is possible with this process to continue building on the substrate with the same crystallographic orientation with the substrate acting as a seed for the deposition. An advantage of this process is the high growth of material, which allows the formation of films with thickness of ~1μm to up to 100μm. However, the temperature of the substrate typically must be at least 50% of the melting point of the material to be added. This technology is widely used for producing silicon on insulator (SOI) substrate.

**Thermal oxidation.** This most basic additive process simply consist in oxidation of the substrate in an oxygen rich atmosphere. This process is naturally limited to materials that can be oxidized and can only form films that are oxides of that material. The temperature is raised to 800°C-1100°C to speed up oxidation.

### 2.1.2 Physical reaction

Common for all these processes are that the material deposited is physically moved on to the substrate. In other words, there is no chemical

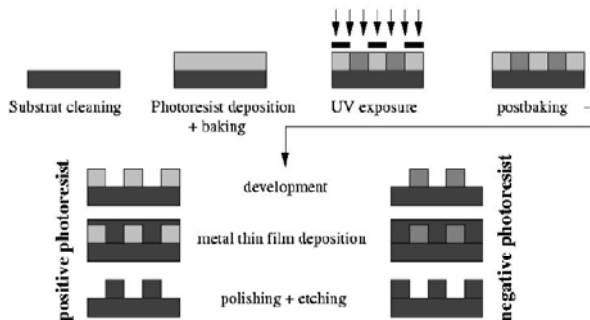
reaction which forms the material on the substrate. The main processes are Physical Vapor Deposition and Casting.

**Physical Vapor Deposition.** PVD covers a number of technologies in which material is released from a source and transferred on the substrate. Major physical principle called on is evaporation : the source material is heated to the point where it starts to boil and evaporate before depositing on substrate. Many materials are restrictive in terms of what evaporation method can be used, which typically relates to the phase transition properties of that material.

**Casting.** In this process the material previously dissolved in liquid form in a solvent, can be deposited to the substrate by spraying or spinning. Once the solvent is evaporated, a thin film of the material remains. This is particularly useful for polymer materials (i.e. photoresist), which may be easily dissolved in organic solvents, The thicknesses that can be cast on a substrate range all the way from a single monolayer of molecules (adhesion promotion) to tens of micrometers. The control on film thickness depends on exact conditions, but can be sustained within +/-10% in a wide range.

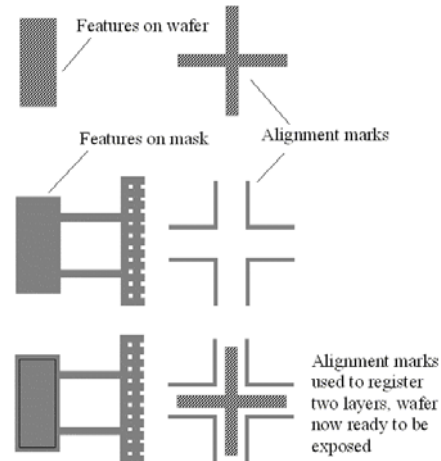
## 2.2 Selective Process

In the MEMS context, the basic selective process is lithography, i.e. the transfer of a pattern to a photosensitive material (mainly photoresist) by selective exposure to a radiation source such light using a set of masks. The photoresist can be either positive or negative, it then reproduces the pattern or its complementary image. Once the photoresist exposed is developed, the pattern appear on the wafer and steps of deposition or etching then occur. A description of positive and negative lithography, metal deposition and etching is shown figure 3.



**Figure 3** Photolithography and metal deposition process steps.

The main problem during this step is masks alignment : the patterns for different lithography steps that belong to a single structure must be aligned each others. The first patterns transferred to a wafer usually includes a set of alignment marks (figure 4), which are high precision features. They stand as reference for positioning subsequent patterns to the first pattern.



**Figure 4** Use of alignment marks to register subsequent layers.

Other problems like exposure parameters required to transfer accurate pattern on the photoresist or adhesion of the photoresist on the substrate may occur.

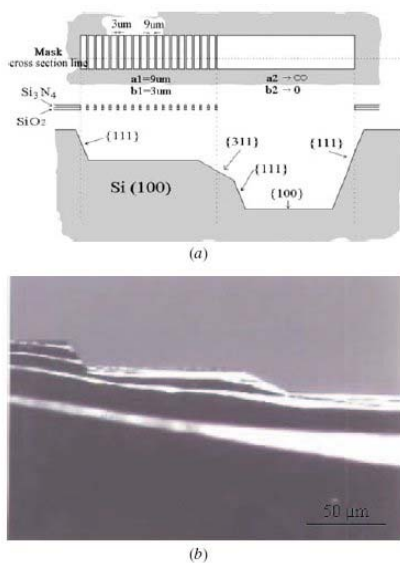
## 2.3 Etching processes

Etching is the basic manufacturing step to remove material which has been selected in lithography in order to form a functional MEMS structure on the substrate. In general there are four classes of etching processes : wet etching, where the material is dissolved when immersed in a chemical solution, dry etching where the material is sputtered or dissolved using reactive ions or vapor phase etchant, these two etching processes being able to be isotropic or anisotropic. Anisotropic etching, in contrast to isotropic etching means different etch rates in different directions in the material.

**Wet etching.** It is the simplest technology because all it requires is a container with a liquid solution that will dissolve the material to be removed. But a mask is desired to selectively etch the material and one must find a mask that will not dissolve, or much slower than the material to be patterned. Etching a hole in a <100> silicon wafer in a chemical (such as potassium hydroxide, KOH ) is an anisotropic etching process : the <111> crystal plane appear and the result is a pyramid shaped

hole.

**Example :** modelling an fabrication of step height control of a multilevel Si <100> structure in KOH solution, using one photomask. Conventional multilevel structures are fabricated by the lithography, deposition and etching technologies. Multimasks are required for the multilevel structure formation : m masks can form (m+1) to 2<sup>m</sup> level terraced structures. The plurality of masks and process cycles of film deposition, lithography and etching not only make the fabrication of multilevel structure a long process with a high cost but also means that the misalignment problem of the masks cannot be avoided, as we've seen before. [4] propose a novel model for the step height control of the Si <100> multilevel structure using one photomask and the KOH wet etching process. The relationship between the step height and the widths and intervals of the masked areas was derived and experimentally verified. Figure 5 shows the mask pattern and cross-sectional diagram of a three-level terraced structure (a) and the micrograph after KOH etching (b).



**Figure 5** A three-level terraced structure with different step heights.

**Dry etching.** Those technologies can split in several separate classes, of which the reactive ion etching (RIE). In RIE, the substrate is placed inside a reactor in which several gases are introduced. A plasma is struck in the gas mixture using an RF power source, breaking the gas molecules into ions. The ions are accelerated towards, and reacts at, the surface of the material being etched, forming another gaseous material by chemical reaction. If the ions have high enough energy, they can knock atoms out of the material to be etched without a chemical reaction. By changing the balance between chemical and physical reactions,

it is possible to influence the anisotropy of the etching, since the chemical part is isotropic and the physical part highly anisotropic the combination can form sidewalls that have shapes from rounded to vertical. A special popular subclass of RIE processes is Deep RIE (DRIE). This process can achieve depths of hundred of micron with almost vertical sidewalls and etching aspect ratio of 50:1. It can also be used to etch completely through a silicon substrate and etch rate are 3-4 times higher than wet etching. However, the cost per wafer, for a silicon wafer, will be 1-2 orders of magnitude higher than wet etching.

We've seen that it is possible to identify some processes constrains and capability. Thus, the shape and the quality of the product depend on the selected process, since that it influences: quality (thickness and uniformity) of deposited materials, deposition rate, formation of bi-products, etched shape of the product, electrical isolation of the wafer, product costs, etc. We can also notice that some parameters are few or less relevant in the choice of process. For example, the batch size is not as sensitive as in traditionnal macro manufacturing because of the natural manufacturing organization in batch and lots.

Of course, this list is not exhaustive. We simply wanted to show that it was possible, for various processes, to identify constraints influencing the manufactured product. However we must keep in mind that there's a wide variety of constraints depending on the physical principle involved in the operation. Thus, it's impossible to give neither generic nor definite classification to guide to the process selection. So there's a stronger need to make all these informations available during the design process. That requires to identify what kind of information is necessary to the designers and at which time during the design process. Moreover, it is necessary to hold account of the constant evolution of the processes and to integrate it in the design tools so that designers do not design according to obsolete processes.

### 3 MEMS design tools and methodologies

In order to be able to integrate process constraints in the design process, we were interested in the MEMS design methodologies and especially the way processes constraints and capabilities can be integrated. Two types of methods seem to emerge : first is Design For Manufacturability, a methodology that considers manufacturability during the design process in order to design manufacturable MEMS. This methods already exist

in the fields of electronics or traditional mechanics and [5] proposes to adapt it for the design of manufacturable MEMS. DFM is an alternative to traditional MEMS product development cycle in which in particular "build and test" approach increase design process and product costs. This method is also proclaimed by one of the reknown integrated specific MEMS design tools : CoventorWare™, composed of four main products, of which ARCHITECT, ANALYSER and INTEGRATOR. We will be interested in the applications of the methods in those products, like presented in [6].

Second method is based on the share of manufacturing knowledge using distributed web tools (that cannot be put in the category of

integrated design tools) to help designers selecting manufacturing processes and material combination.

### 3.1 Design For Manufacturability

DFM is well known as a design methodology that aim to reduce manufacturing time and cost [7]. In contrast, we'll try to value the assistance provided by such method in the crucial problem of process selection. Fundamental activities of MEMS development may be broadly divided in four overlapping phases organized as shown in figure 6.

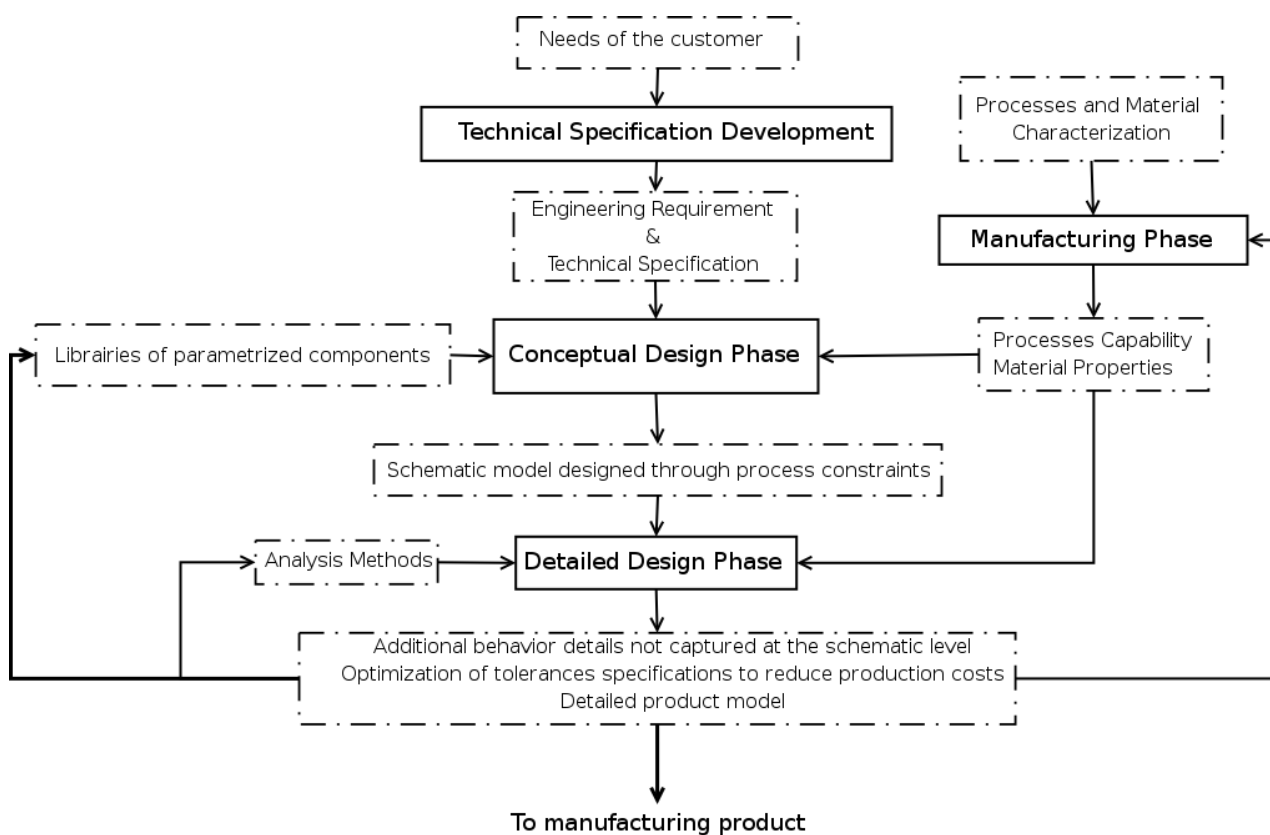


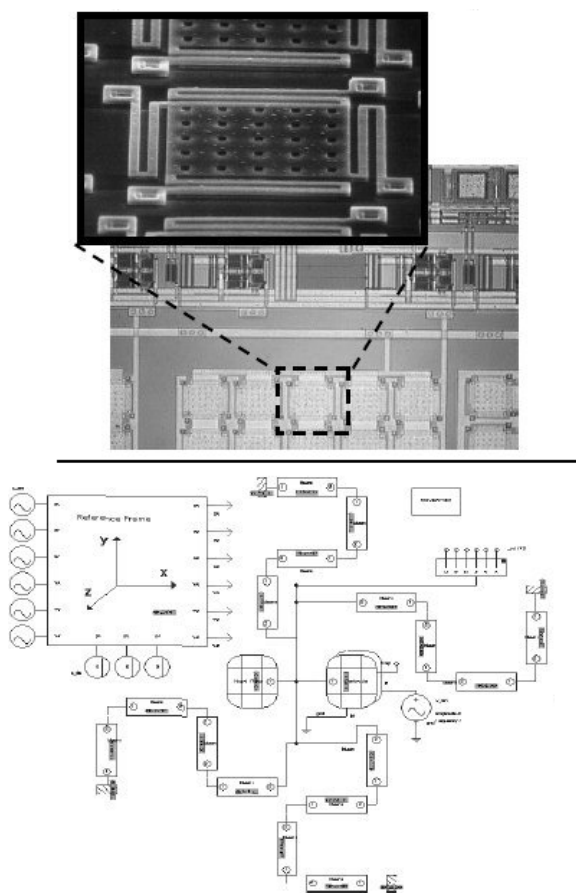
Figure 6 Schematic of DFM methodology implementation.

**Technical Specification Development.** It is the phase where the determination of the needs of the customer is converted into engineering requirements and technical specifications, starting points of the following phase. It is important that the customer requirements document maintain the original intent of the customer and is not overly influenced by perceptions of the engineering teams.

**Conceptual Design Phase.** It is a phase where designers develop and evaluate many design concepts simultaneously so as to offer enough

choices for a successful product. For that, they create then use libraries of standard parametrized components elements that they can piece together to create more complex designs. Each element of the library is essentially an analytical or semi analytical model that captures the behavior of the element accurately over all possible displacements of the element. All parameters of the element model are available to the designers as variable to be defined and set. For instance, the non-linear beam element model is the model of an Euler beam, where parameters such as length, thickness, width, as well as material properties such as

Young's modulus, Poisson's ratio, residual stress are all available variables. As MEMS can sustain mechanical deformations in 3D space, each component model necessarily has 6 degrees of freedom. A schematic model assembled from parametrized library components immediately enables very rapid and accurate characterization of the behavior of a specific conceptual design. One of the advantages of this phases is the ability for designers to design through process constraints. Indeed, parameters may be well defined within the tolerances of the specific manufacturing unit and this influences the product development process substantially as only those designs that can be manufactured within the process are considered. Figure 7 shows an example of the Conceptual Design Phase of a variable capacitor designed using ARCHITECT. We can see an image of the CMOS fabricated device (top) and the schematic model (bottom). Each "component" in the schematic model correspond to a part of the CMOS fabricated device : for instance, the four folded suspension arms are each modelled with four connected parametrized beams.



**Figure 7** CMOS variable capacitor (top) and its schematic model.

**Detailed Design Phase.** During this phase, detailed engineering analysis of the selected design

concepts is performed in order to provide additional details of the behavior of the design or to study effects not captured at the schematic level during Conceptual Design Phase. CoventorWare™ has analysis tool, ANALYSER, composed of different bundles which include for instance : finite element methods (FEM), for mechanics and general fluidics, boundary element methods (BEM), for electrostatics and inductance... All ANALYSER bundles include moreover MEMS-specific mesh generation. These details make it possible to the designers to optimize product shape and to asses tolerances specifications in order to reduce production costs. For instance, for the variable capacitor, analysis performed in the detailed design phase allowed designers to calculate the distribution of the pull-in voltage in function of the tolerances of the material properties (thickness, stress gradients ...) Then, INTEGRATOR reduces the detailed 3D analysis produced in ANALYSER into a reduced-order model that can supplement Coventor's extensive ARCHITECT library of parametrized MEMS components.

**Manufacturing Phase.** Concurrently with the initiation of the design group's activities, begins the Manufacturing Phase, with an aim of :

- identifying critical process characteristics, such as verticality or surface roughness
- identify and evaluate existing processes, in order to chose between a standard process, a slightly modified standard process or a newly developed process.

That necessarily requires characterization of processes capability and materials properties : for instance, experiments are initiated so as to determine what kind of shape can be made, with which processes and materials. Processes capability and materials properties informations are integrated in parametrized models used in the design phases.

It should be pointed out that some traditionals guidelines of DFM (in the mechanical engineering field) clearly arise in MEMS context:

- use of standard components,
- develop a modular design,
- design for ease of fabrication,
- avoid separate fasteners.

But some are completely out of scope:

- minimize assembly directions,
- design parts for multi-use.

This only tends to prove that DFM method can't be a simple mix of methodology available in both mechanical and electronic world.

After all, we can concentrate on informations and distinguish which one should be

useful for designers at the conceptual and detailed design phases.

**Conceptual Design Phase.** At this level, designer needs

- geometrical informations, in order to know if he's designing manufacturable product and if so, with which process.
- material informations, to know which material can be deposited, selected, etched...
- economical informations, to help him to choose between two processes having the same performances
- thermics informations, to know if the manufacturing temperature of one schematic element will not damage the others.

One needs, moreover, to take into account the maximum of information simultaneously because independently, these informations has only little interest. For instance, it is possible to obtain rounded wall using wet etching process, but not in silicon, because of anisotropic etching properties of this material (taking account simultaneously geometrical and material informations).

**Detailed design Phase.** At this phase, designer needs information on the limits of capabilities of the processes because in this phase, one optimizes geometrical product characteristics to obtain awaited behaviour while assessing tolerance specifications in order to reduce production costs. Designer needs, for instance, minimum thickness or temperature of a deposited material, best roughness obtained after etching...

### 3.2 Sharing knowledge using web tools.

The following approach is more oriented "process selection". Due to the typically unstable context of R&D, designers currently tend to conceive MEMS in terms of processes and materials in which they are familiar and may not consider process and material combination that may have proven more economic. To solve this problem, some tools have been developed to help designers selecting "best" manufacturing processes and material combinations, based on the share of knowledge using Internet and web databases. [8][9].

Processes and materials characteristics are stored in web databases. For instance, on the website [www.mems-exchange.org](http://www.mems-exchange.org) for the silicon nitride PECVD process, one can found informations like thickness (amount of material added to a wafer), ambient (to which substrate is exposed during processing), material (which can

be deposited), microstructure, uniformity, wafer geometry, wafer material, wafer thickness...(see figure 8)

Designers build a manufacturing sequence, using these informations, and submit it to a specialized team which validate the project or propose best sequence.

Silicon nitride PECVD	
Fab site	Commercial
Process characteristics:	
Thickness <small>Amount of material added to a wafer</small>	2.0 <input type="text"/> μm <input type="button" value="v"/>
Ambient <small>Ambient to which substrate is exposed during processing</small>	nitrogen, silane, ammonia
Material	silicon nitride
Microstructure	amorphous
Sides processed	either
Uniformity	-0.03 .. 0.03
Wafer diameter	150 mm <input type="button" value="v"/>
Equipment	Oxford Plasmalab PECVD System
Equipment characteristics:	
Batch sizes	150 mm: 1

**Figure 8.** Example of typical informations available to the designer.

The WebMems-Mass tool also contains manufacturing and materials data but propose an algorithm to select processes and material combination against econo-technical criteria. While running, WebMems-Mass generate a dialogue with the designer to inquire and acquire about batch size, typical tolerances size, overall shape, cost requirements... Then, the user is given real-time feedback regarding plausible fabrication sequence. At each step of the design process, the user is presented with an updated, ranked list of manufacturing and material possibilities.

Of course, those tools are not integrated MEMS design tools and only help designers selecting right manufacturing process and material combination. But these tools shared on Internet are well adapted to a concurrent collaborative design by making easier communication between designers from different disciplinary and manufacturing team. Using libraries of standard components for the design of new products certainly restricts little more the design state space, but increase guarantee of designing manufacturable product. An other advantage of shared web tools is their facility with being updated in order to be aware of manufacturing processes evolution. This seems to be the most efficient answer to the lack of availability with boundary limits of manufacturing process.

## 4 Conclusion

MEMS products are getting more and more popular everyday. Though the industrial context is still research and development oriented, efforts are



made to turn to mass-production era.

To achieved this conversion, the concept of manufacturability must be considered. At the present time, manufacturability roughly sounds to rely on a good process choice. So we have had a special interest in presenting a sample of manufacturing processes derived from VLSI technologies that our community (mechanical manufacturing) is not familiar with. This has allow us to propose some rough qualifier to the informations designers may integrate.

We now have to concentrate on the building of the manufacturing sequence. Indeed, process selection is only part of the manufacturing issue, and manufacturability is also concerned with process compatibility.

Another aspect of the problem is that manufacturing process can be based on various physical principles and the knowledge attached to them, even expressed under constraint form doesn't prove to be easily understood. Consequently, further works have to be done concerning the cognitive aspect of the knowledge sharing as very different communities of experts are involved in such projects.

Finally, VLSI technologies are pushed to their limits to let the designers be more innovative (by introducing non silicon materials for example) but we must already think about the integration of innovative technologies in the current design process. This means introduction of further more different physical principles (micro-cutting, abrasive...). This will increase the need for a unified classification of manufacturing constraints that would overcome the limits of disciplinary expertise.

## References

- [1] A. De Grave : *Conception intégrée de micro-systèmes électro-mécaniques*. PhD Thesis, University Joseph Fourier, 3S Laboratory, Grenoble, 2004.
- [2] A. De Grave, C. Masclet and D. Brissaud : Integrated design of MEMS, in proceedings of MIT'04, Constanta, pp 67-72 , October 4-5th 2004.
- [3] C-K Chung, M-Q Tsai, P-H Tsai, C Lee: *Fabrication and characterization of amorphous Si films by PECVD for MEMS*. Journal of Micromechanics and Microengineering, vol 15, pp.136-142 IOP Publishing, September 2004.

- [4] C-K Chung: *Modelling and fabrication of step height control of a multilevel Si(100) structure in KOH solution*. Journal of Micromechanics and Microengineering, vol 14, pp.341-346, IOP publishing, 2003
- [5] M. G. da Silva, R. Giasolli, S Cunningham, D. DeRoo: *MEMS Design For Manufacturability (DFM)*. Sensor Expo & Conference, Boston, Fall 2002
- [6] G. Schröpfer, M. McNie, M. G. da Silva, R. Davies, A. Rickard, F-X Musalem: *Designing manufacturable MEMS in CMOS compatible processes – methodology and case studies*. In SPIE's Photonic conference, MEMS, MOEMS and Micromachining proceedings, Strasbourg, 26-30th april 2004.
- [7] D. M. Anderson: *Design for manufacturing and concurrent engineering*, CIM press, 2004.
- [8] X. F. Zha, H. Du : *Manufacturing process and material selection in concurrent collaborative design of MEMS devices*. in Journal of Micromechanics and Microengineering, vol 13, n. 5, pp.509-52, IOP Publishing Ltd, May 2003.
- [9] Mems and technology exchange, available at <http://www.mems-exchange.org>. last accessed July 05.