SiC Power Semiconductor Devices for new Applications in Power Electronics

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***Abstract*— This paper addresses the benefits of SiC semiconductor, owning excellent physical properties able to fulfill new scope of applications in terms of high temperature, high voltage and for more specific applications. Devices and applications developed at Ampere laboratory are detailed.**

***Keywords*— SiC-device, High temperature electronics, Power semiconductor device, High voltage Device, Power integrated circuit.**

I. Introduction

The first unipolar power silicon carbide devices (Schottky diodes) were commercialized in 2001 [1], [2]. Nowadays power JFETs are available as engineering samples [3], [4] . These two devices enable to build a large number of power switching converters. It is worth listing the scope of applications for which silicon carbide devices can advantageously replace classical silicon power semiconductor devices. The first kind of applications for SiC power devices are applications for which the use of silicon is impossible or restricted. The second kind of applications for SiC devices correspond to systems in which mass reduction is a key issue, e.g. for embedded systems like in transport.

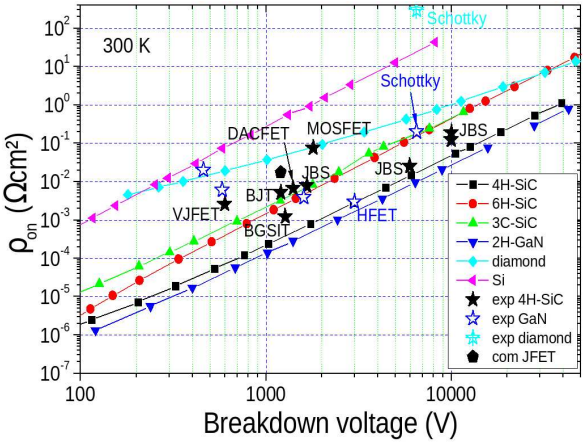

Fig. 1. On state resistance for unipolar devices for various semiconductor materials.

Figure 1 illustrates the on-state resistance for different semiconductor materials. It yields the optimal on-resistance limit versus breakdown voltage of an infinite plane junction for different semiconductor materials. These are theoretical limits. Stars correspond to power device demonstrators. It is clear that there are over the theoretical limit of Si and also from the SiC limits. From this figure, it is clear that there is still a great margin to get the optimal performances of SiC devices.So, clearly, SiC power device applications are high temperature and/or high voltage applications. However, most of recent studies have shown that the use of SiC devices does not consist in a simple replacement of silicon devices by silicon carbide devices. Indeed a new design of power electronic systems must take advantage of the properties of the new SiC power devices.

II. High voltage applications

Such applications are medium term applications because high voltage devices are not ready for industrial applications. However 10 kV demonstrators have been developed, $15kV$ demonstrators are under development even $30kV$ and further may soon be obtained. The interest in such devices is huge since they enable to :

- replace heavy $50Hz$ high voltage electrical transformers by high voltage static power electronics.
- replace AC-current distribution networks by DC-current distribution networks and eliminating numerous associated problems like instability (wind-power farm ...) even blackout. This enables an easier integration of renewable energy sources (Photovoltaic, Wing power...) and removes the need of $50Hz$ electric transformers.
- improve the high voltage system protection with very fast active protection systems.

The main issues of these new applications are :

- availability of high bipolar diodes and switches (BJT, Thyristors, ...),
- electrical insulation of the high voltage converters (packaging, passivation, ...),
- thermal cooling of the high voltage converters, highly insulated driver for high voltage converters even multi-level converters.

Ampere lab works are divided in several tasks:

A. Design of high voltage periphery protection

Design of efficient peripheral protection is fundamental for high voltage devices. This protection should have an optimum geometry in order to avoid local critical electric field areas. There are various possible protections such as JTE (Junction Termination Extension), Mesa, field plates

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or guard rings [5]. Design of classical JTE needs an accurate control of the doping dose to reach the complete depletion of the termination well for a given reverse voltage (V_{BR}). The peripheral protection efficiency is the ratio between breakdown voltage of the protected diode and of the ideal diode (plane parallel junction), this last being named theoretical breakdown voltage afterwards. JTE process for SiC device is most often an ionic implantation followed by a thermal annealing. Figure 2 shows the breakdown voltage of a bipolar diode against the termination doping dose for several JTE lengths.

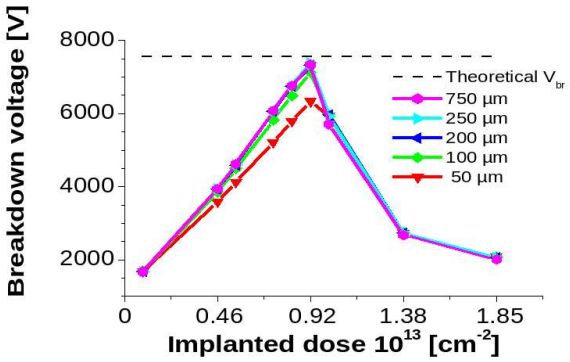

Fig. 2. Breakdown voltage against implanted dose for a constant lateral doping profile and for several JTE lengths.

With an epitaxial layer thickness of $50\mu m$ and a doping level of $10^{15}cm^{-3}$, the diode is able to sustain $7.5kV$. The JTE depth is $0.8\mu m$. As can be observed from Figure 1, breakdown voltage is very sensitive to the implanted dose. Besides this voltage is almost independent from the well length if the JTE is longer than $100\mu m$. The breakdown voltage is calculated by numerical bi-dimensional simulation using $MEDICI^{TM}$ software [6] and impact ionization coefficients published by Konstantinov [7]. V_{BR} is defined as the voltage involving a leakage current of $1\mu A.\mu m^{-1}$. JTE with variable lateral doping is a good way to get an efficient protection valid for a wide range of doping concentration. Thanks to the diffusion process, it is possible to realise this kind of JTE in silicon. However, due to the lack of dopant diffusion in SiC, variable doping JTE is very difficult to obtain. A good alternative is a JTE with multiple constant doping zones to approximate the optimum lateral profile. Figure 3 presents a SiC bipolar diode protected by a three-zone JTE that has been optimized to achieve a breakdown voltage that is as close as possible to the theoretical breakdown voltage.

Each zone is defined by its doping dose D_i and its length X_i. Figure 4 shows 5 possible configurations of doping variation of the three zones enabling a V_{BR} of 7500 V i.e. 99% of the theoretical breakdown voltage. The highest doped zone is the first one and its variation range is the widest. For the two other zones, dose choices are more critical, because of the wider $D2$ variation range, and of the narrower $D3$ one.

A 7500 V breakdown voltage can be obtained using

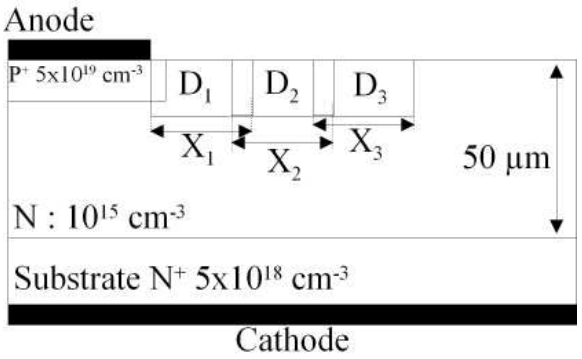

Fig. 3. Vertical cross-section of the triple JTE (D1, D2 and D3) protected diode.

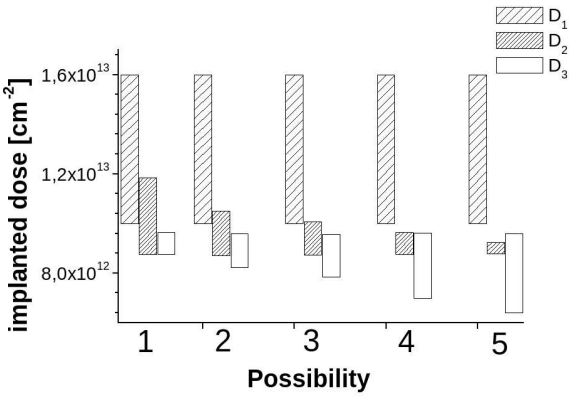

Fig. 4. Five possible dose configurations and their variation ranges to obtain a 99% protection efficiency.

simple or triple JTE. Nevertheless the latter option (which is a discretization of the ideal variable lateral doping profile) enables a larger flexibility on doping concentrations. The only drawback of this technique is a little more complicated technological process.

B. Fabrication of high voltage bipolar devices

The aim of this study is to show potentialities of silicon carbide for high voltage power systems. Test structures are SiC bipolar diodes able to sustain $1.3kV$ and $5kV$. Emitter and periphery protection (JTE) are obtained by ion implantation of Aluminium in epitaxial n-type layer grown on commercial substrate. The number of devices which exhibit efficiency $> 84\%$ has been improved during the last four years. Indeed 70% of the $1.3kV$ diodes with an emitter implanted at $300\,^{\circ}C$ and a long JTE (120 m) exhibit a breakdown voltage higher than $1100V$ (up to $1300V$) without any impact of the ambient conditions (air or SF6 gas or dielectric liquid). The ambient conditions impact breakdown voltage only for diodes with short JTE length ($50m$) [8]. These results show in the same time that post-implantation annealing realized in the lab furnace [8] allows a full activation of dopants in JTE. In forward state, current densities and efficiency have been improved

(200 A/cm2 @ 5 V at room temperature) also due to the improvement of metallization step and subsequent annealing at IMM Bologne [9]. Results of acceptable ohmic contacts on highly doped P+ zones are comparable with other results already published in literature [10]. As it can be observed in Figure 5, Ampere-lab is now able to present results of breakdown voltage in the range of 4 kV, with a maximum of 4.8 kV with low reverse current density in fluoride ambient (Galden and SF6) [11].

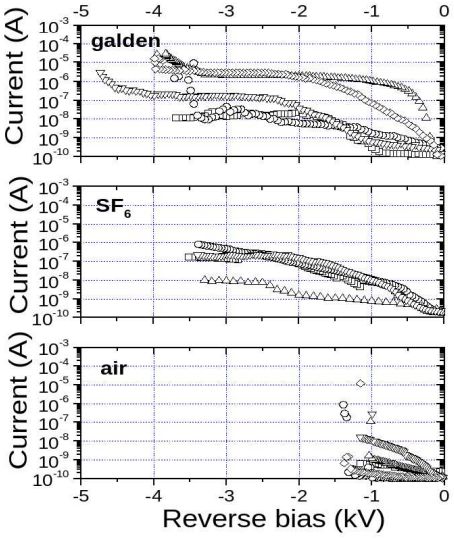

Fig. 5. Reverse I-V characteristics of $5kV$ bipolar diodes measured in three different ambient conditions: air, galden and SF6. Active area $A = 0.05mm^2$.

Without passivation, breakdown voltage is only $1.3kV$ for these devices with a JTE length of $250m$ (optimized with respect to the semiconductor properties). This clearly proves the need for passivation in order to fully take benefit of SiC properties for high voltage applications. Theoretical interest to use passivation materials with high dielectric permittivity (ϵ) in order to reduce electric field outside SiC have been shown using simulation software MEDICI on a 5 kV bipolar diode protected by JTE. For a given structure, only a sufficiently high ϵ value allows to reduce electric field peaks both at emitter and JTE extremities, by stretching space charge region outside the JTE [12]. Another advantage to use a high ϵ material is to significantly reduce the sensitivity on breakdown voltage with respect to the optimal dose of JTE. From the technological point of view, choice of such material (with high ϵ) and a compatible deposition method remains to be solved before obtaining experimental results. Among available and practical insulating materials, polyimide materials specifications exhibit good dielectric together with good thermal properties under usual conditions. Thus an experimental characterization using MIM and MIS structures has been launched in order to quantify their effective characteristics within an extended temperature range. For high voltage (up to $50kV$) and high temperature (up to $500\,^{\circ}C$) measurements, a specific set-up has to be developed.

1) Fabrication of high voltage thyristor: Since silicon based technology is reaching its physical limits concerning blocking and power handling capability, GTO thyristors based on SiC are under investigation for compact future pulsed power systems [13]. Reaching breakdown voltages of $19kV$ [14], the potential of SiC based devices appears very interesting. According to primary device simulations using the finite element code MEDICITM, the developed GTO-thyristors should be able to block voltages up to $6kV$. For the device realization, a n-type 4H-SiC wafer material is obtained from Cree ResearchTM, including a $PP-NP+$ (from the wafer up to the top) epitaxial layer structure (6). Anode P+ type

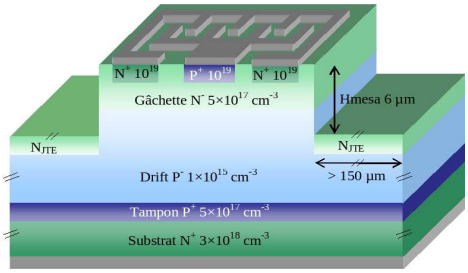

Fig. 6. Thyristor structure with planar electrodes for anode and gate and combined periphery protection: MESA and JTE

and gate N+ type layers were obtained by Aluminium (Al) and Nitrogen (N) ion implantation doping followed by a high temperature annealing in the $1700\,^{\circ}C/30min$ range in order to activate the dopants. Mesa structures were fabricated by Reactive Ion Etching with Ni masks with a particular attention to avoid micromasking formation and preserving the initial roughness of the surface. Ohmic contacts are formed by deposing layers composed on $Al/Ni/Ti$ alloys followed by a RTA annealing at $1000\,^{\circ}C$ during 1 to 2 min. Measurements have been performed on chip, in oil and as shown in Figure 7 a breakdown voltage of nearly $5kV$ has been reached.

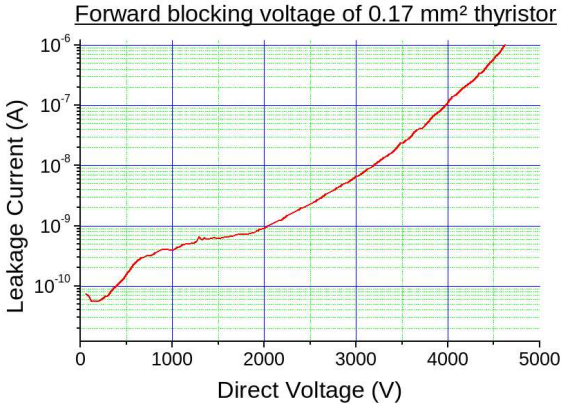

Fig. 7. Forward blocking characteristics of the device.

III. Specific Applications using SiC Devices

The ability for SiC devices to operate in the high temperature range, $250^\circ C$ up to $600^\circ C$ allows applications not possible with conventional silicon devices, especially for mains-operated systems.

A. Current limiting devices

To protect power electronic circuits against over-current or over-voltage either serial protection (SP) or a parallel protection (PP) can be used. For the serial protection (8, usually used components are Serial Protection Device (SPD) or Current Limiting Device (CLD), being either fuses, mechanical contactors, superconductors or polymers.

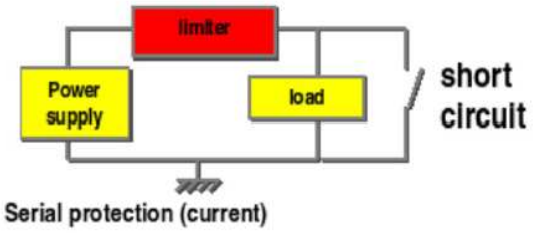

Fig. 8. Circuit using the protecting device

In all cases it is necessary to dissipate the overload energy through the protection device which has to sustain high voltage and high current simultaneously. These constraints imply a very fast temperature increase. So, when the protection device is active it has to sustain high junction temperature. All these constraints will globally define the electrical specifications of this kind of device. Up to now, only few semiconductor current limiter structures have been described in the literature [17], [16]. Although Current Regulative Diode components already exist, their voltage and current capabilities ($V_{BR} = 100V$, $I_{MAX} = 10mA$), do not allow to use them in power systems. A promising application of SiC-based devices is current limitation for power system protection, which benefits from its high thermal conductivity and wide band gap. In the steady state operating mode (or passive state), the voltage drop across the component must be as low as possible. In the active state, (limiting phase), the current limiter must sustain a high current, under high voltage bias. The resulting high power density must not cause the component failure. Two specific current limiting devices (CLD) have been studied [18], [20], [19] taking into account previous considerations.

Figure 9 shows a cross section schema of the VJFET and the main parameters to adjust. This device has a channel divided in two parts: a vertical one and a lateral one. The source is grounded and current flows from drain to source. P-buried layers are designed so that the VJFET is normally-on and presents a low specific resistance. When the drain voltage rises, the current saturates at a voltage corresponding to the pinch-off of both vertical and horizontal channels. In the saturation mode, the device

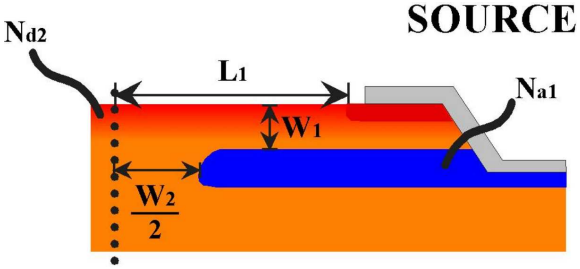

Fig. 9. VJFET parameters to be optimized.

presents an important on resistance (R_{ON}), resulting from the serial resistance of both parts of the channel and the drift resistance of the epitaxial layer. Due to self heating, current decreases as the voltage increases (since electron mobility decreases and induces a current reduction). This effect is amplified while increasing the limiting current density. When a negative bias is applied between gate and source, the PN junction formed by the Pwell and the epitaxial layer is reverse biased leading to current modulation. The device optimization job consists in the design of buried layer (the gate electrode of the devices, which is formed by either high energy implantation or epitaxial process), and the tuning of horizontal channel parameters. A trade off between specific resistance and blocking capabilities was investigated by means of analytical model and finite element simulations.

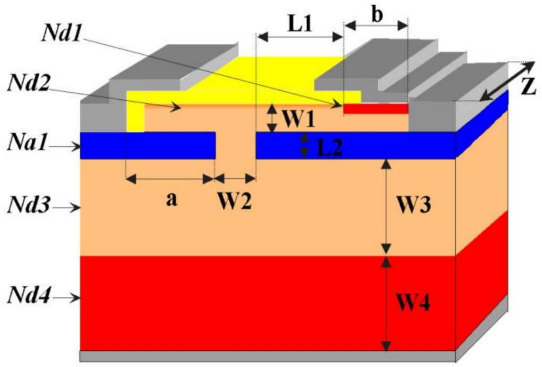

Fig. 10. JFET structure with its parameters.

Figure 10 presents the vertical JFET structure, 3 terminals device, with all parameters to be optimised by simulation with ISE TCAD. An AccuMOSFET, 2 terminals device, has also been designed and fabricated.

Fabrication process (7 level masks) complexity is similar to silicon power device one. The samples were manufactured at Centro Nacional de Microelectronica, in Barcelona. Key points of the device fabrication are high energy implantation, annealing activation and ohmic contact formation. Based on CNM- SiC technology, specific steps have been optimized: horizontal channel definition (implanted doses value as well as geometrical parameters) for both the VJFET and the AccuMOSFET. An

additional step has been tuned for the AccuMOSFET: the MOSFET channel oxide layer. First batch of small area devices has been fabricated. Figure 11 presents the

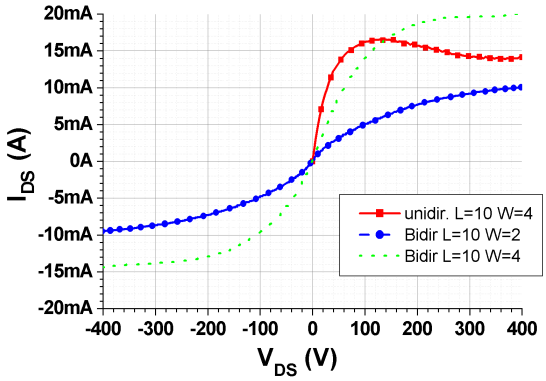

Fig. 11. Electrical measured characteristics for unidirectional and bi-directional limiter.

measured electrical characteristics for an unidirectional VJFET. Measurements were done by applying $0.5s$ pulse ($f = 2Hz$), with drain biased up to 400 V. The specific on-resistance varies from $176m\Omega.cm^2$ up to $237m\Omega.cm^2$. The maximum pulsed power density dissipated by the CLD in the limiting mode is $160kW/cm^2$. Limiting capabilities have also been measured for a bi-directional device made of two unidirectional devices connected head to tail (i.e. drain connected). This one exhibits a specific on-resistance of $700m\Omega.cm^2$. Highest breakdown in current limiting state were measured to be $810V$, corresponding to a high pulsed power density of $140kW/cm^2$. As it can be observed from Figure 12, the current limiting device is able to react in a very short time (less than $1\mu s$).

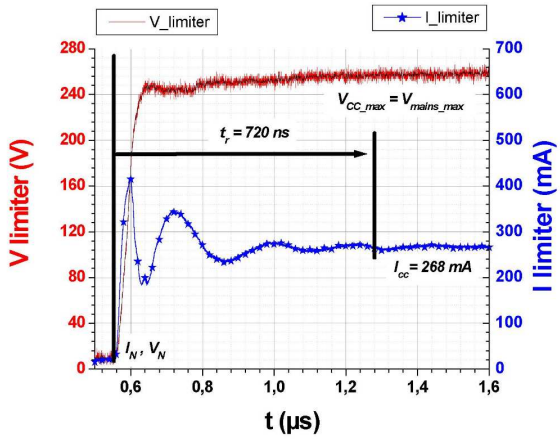

Fig. 12. Switching waveforms of the current limiter with gate control.

Based on small area devices optimization work, larger area AccuMOSFET ($S = 0.3cm^2$) have been fabricated. Static characterizations have been performed using a specific pulsed power measurement setup. Depending on the layout of the device (geometrical variation), saturation current in the range of $300A$ to $450A$ has been measured (Figure 13), with a pinch-off voltage around $V_P = 12V$.

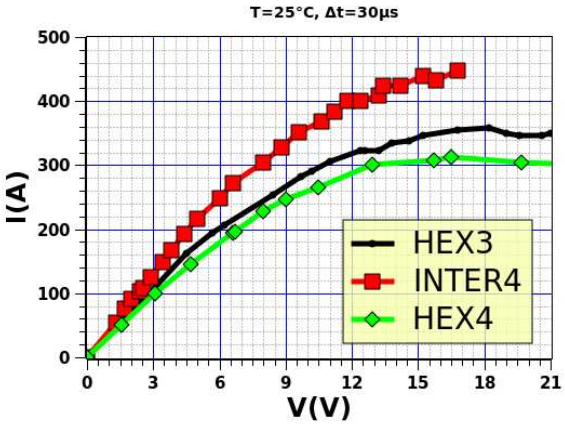

Fig. 13. Electrical measured characteristics for unidirectional high current liming AccuMOSFET device.

Self heating effect for short time pulses ($t_P = 100\mu s$) has been estimated by an analytical model. Mobility, i.e. current, reduction of 9% for a $100\mu s$ pulse gives an internal temperature increase estimation of $10\,^{\circ}C$. Based on experimental measurements, analytical modeling and electro-thermal finite element simulations, the short circuit energy capability of an AccuMOSFET CLD has been estimated to be $ECC_{max} = 35J$. We report on both simulation work, fabrication process and experimental results of a unidirectional and bi-directional current limiter structure based on a VJFET and ACCUMOSFET, with improved current capabilities (specific resistance as low as $40m\Omega$, and a saturation current between $200A < I_{SAT} < 450A$). The design was made using the ISE software with respect to the technological limitations. The first demonstrator exhibits optimistic dynamics characteristics. Bi-directional components were measured by associating two devices head to tail. Short circuit demonstration was done using $5W - 240V$ bulbs as a load on low current rating devices. Very low response time to short circuit has been measured (as low as $t_R = 1\mu s$). Using such a component with increased current ratings should permit a complexity reduction of classical mechanical device. Next challenges consist in both current sensing and current modulation in limiting state using the gate electrode so that to reduce short circuit power losses.

B. Monolithic converters

Hybrid approaches suffer from interconnection reliability. Integration appears to be a more effective approach providing capable power devices and passive components. Due to their physical properties, semiconductors with large band-gap are very interesting in this case. The integration allows to reduce considerably the switching

time and to reduce losses and parasitics related to the device interconnections. This integrated system based on the design of SiC lateral JFET with a breakdown voltage of 900V is presented in Figure 14.

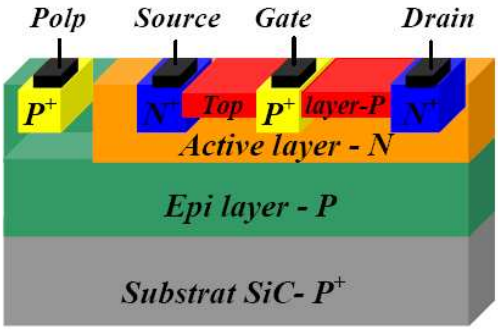

Fig. 14. Schematic presentation of the SiC lateral JFET with a double RESURF structure.

In order to improve the blocking voltage and to reduce the Ron-resistance, the RESURF technique [15] is applied in this work to design SiC lateral JFETs. The $P^{+}type$ region (gate), $N^{+}type$ region (source and drain), N type active layer and $P-type$ top layer are realized by ion implantation. The epitaxial layer at the top of the substrate is defined by a $P-type$ region with a uniform doping concentration. A double-junction is created in the top and the bottom of the active $n-type$ layer, improving its lateral depletion and allowing increasing of its doping. The $n-type$ active layer constituting the JFET channel, this technique allows to obtain a JFET with higher channel doping and so a lower on-resistance by keeping a high V_{BR}. A relationship between the doping concentration and the thickness of layers must be respected to vertically deplete both the $p-type$ top layer and $n-type$ channel layer before the lateral junction breakdown. The structure of these devices was studied with $MEDICI^{TM}$. In each area of the device structure, different parameters are defined such as profile and concentration of doping impurities which were estimated by Monte-Carlo simulations taking into account the 4H-SiC crystalline structure. The lateral JFET is a normally-on device. A negative gate voltage is required to turn the device off. The channel doping is $2.10^{17}cm^{-3}$ and its thickness is $0.40\mu m$ which is smaller than the thickness of the depleted region produced by the applied drain-to-source voltage. The thickness of the $p-type$ top layer is $0.12\mu m$ The potential line distributions in the double RESURF SiC JFET in forward blocking mode are shown in Figure 15 for different doping concentrations of the top layer varying from $5.10^{16}cm^{-3}$ to $5.10^{17}cm^{-3}$.

The V_{BR} variation is also presented in Figure 16. The potential lines are distributed mainly in the p-type epi-layer due to the low doping concentration of this layer. The presence of the top layer with a low doping concentration ($5.10^{16}cm^{-3}$ -Figure 15-a) generates a potential line distribution transversally at the device surface. In this

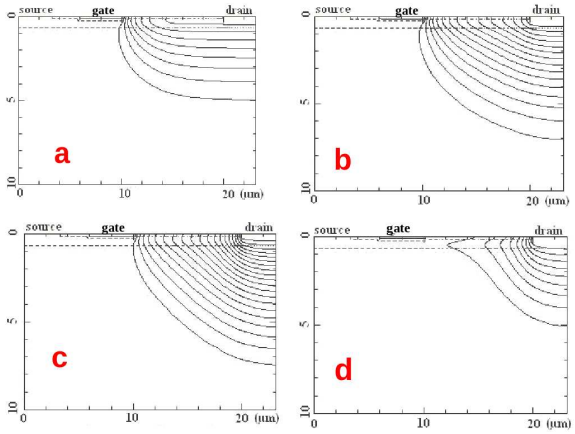

Fig. 15. Potential distribution for the lateral JFET with a doping concentration of the Ptop layer : $5.10^{16}cm^{3}(a), 1.10^{17}cm^{3}(b), 2.10^{17}cm^{3}(c) and 5.10^{17}cm^{3}(d)$

case, the value of blocking voltage is equal to $385V$. In the same way, a high doping concentration of the top layer with a high doping concentration ($5.10^{17}cm^{3}$ - Figure 15-d) makes difficult to deplete this layer. The maximum value of electric field is obtained at the drain side. In this case, the potential lines are concentrated that involves the device to reach prematurely the blocking voltage.

The potential distribution is optimum, when the doping concentration of the top layer ranges between $10^{17}cm^{-3}$ and $2.10^{17}cm^{-3}$, thus obtaining a trapezoidal electric field profile between the drain and the gate. In this case, the Space Charge Region (SCR) surface is wider when he VBR of the JFET is increased up to $1kV$, as presented in Figure 16.

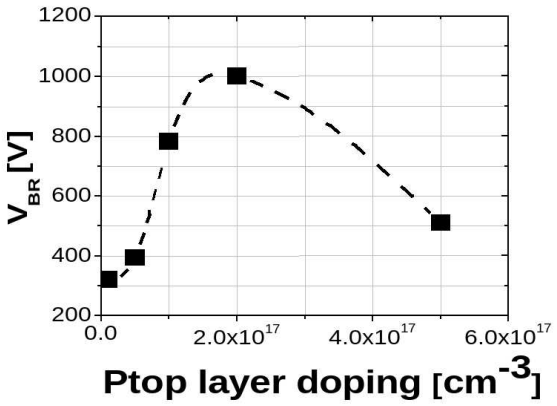

Fig. 16. V_{BR} versus top layer doping for the JFET structure.

The lateral JFETs run is performed (Figure 17). The first results show that in blocking state, the RESURF structures are validated in terms of voltage rating. Breakdown voltage values as high as $600V$ were obtained which is conform to the specific requirements for which these

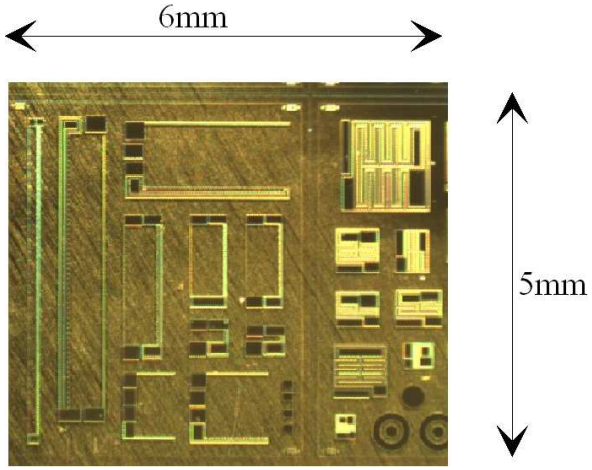

Fig. 17. Top view of the SiC lateral JFETs with different inter-digitated structures and different sizes.

devices have been designed.

IV. Conclusion

This paper shows the already existing devices and applications using SiC devices. Higher theoretical values could be reached but the environment of the devices remains a critical issue. Dealing with Current Limiting Devices, although we demonstrate they are able to sustain high current densities, the packaging and interconnections are limiting their performances. It seems to be clear that for high voltage devices, the periphery protection must now combine several classical techniques, and must take into account the passivation features (dielectric permittivity, thicknesses and interface states density). There is still works to be done to reach the real performances of SiC semiconductor material, for the fabrication of high voltage, high temperature and integrated power systems.

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