A Real Time Predictive Maintenance System of Aluminium Electrolytic Capacitors Used in Uninterrupted Power Supplies

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***Abstract*—This paper presents a low cost method to realize a real time condition monitoring and a predictive maintenance system of an electrolytic capacitor used in Uninterrupted Power Supplies (UPS). This method consists in detecting the changes on real time in equivalent series resistance (ESR) and the capacitance C values of the electrolytic capacitors. Simulation and experimental results are presented to illustrate the proposed monitoring technique. The proposed method can be used in UPS where waveforms are continuously varying in amplitude, frequency and versus temperature. The proposed on line failure prediction method has the merits of using only the existent resources in UPS and with the use of knower algorithms.**

***Index Terms*—Electrolytic capacitors, predictive maintenance, real time, identification, Kalman filter.**

I. Introduction

Electrolytic capacitors have been widely used in power electronic systems because they can achieve high capacitance and voltage ratings with volumetrically efficient and low cost. This type of capacitors have been traditionally used for filtering, coupling, timing networks, by-pass and many other applications in power electronics requiring a cost effective and volumetrically efficient component. It's known that the common faults in electrolytic capacitor include initial catastrophic failures due to manufacturing or misapplication defect, and wear-out faults which cannot be avoided. Unfortunately, electrolytic capacitors are one of the weakest components in power electronics converter [1-13]. For example [1], [4], in Uninterrupted Power Supplies (UPS), they are responsible in about 50% cases of power electronics component failures. Electrolytic capacitor has a number of root causes and failure modes. Degradation of this component is due to a combined effect of electrical, thermal, mechanical and environmental stresses. The main wear-out failure mechanism is the evaporation of the electrolyte solution which is accelerated with temperature rise during the operation and due to ripple currents. This causes a decrease in C and an increase of ESR which further increase temperature (losses). Standard [2] suggests that the capacitor should be considered as failed if there is a double increase of the initial ESR value and a 20% decrease in the capacitance one. Hence, the estimation of the ESR and the capacitance by taking into account the temperature is important for condition monitoring of the electrolytic capacitor. The purpose of this paper is to propose a method to detect in real time the changes in the value of the ESR and also the capacitance in order to create a real time predictive system of electrolytic capacitor failures. It is further shown in this paper that the proposed method can be applied even in the non-stationary system such as UPS where capacitor ripple voltage and current are continuously varying in amplitude and frequency. They also depend on the ambient temperature where the converter operates.

Many papers have proposed different methods or algorithms to determine the ESR and/or capacitance C of the electrolytic capacitor [2-13]. However, many parameters such as off-line additional measurements and many computations are required, which makes it complicated, difficult, expensive and impractical for actual application.

Nowadays, UPS dispose of many accurate sensors, numerical treatment systems and powerful computation resources which are used to control and regulate UPS in order to improve its performance and efficiency. The suggested method has the merits of making a real time predictive maintenance system of electrolytic capacitors by using existing resources in the UPS. This predictive maintenance system works in background task and without disturbing the regulation and the operating system.

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II. Electrolytic capacitor technology

A. Electrolytic capacitor modeling

The structure of a screw terminals electrolytic capacitor [16] is shown in Fig.1.

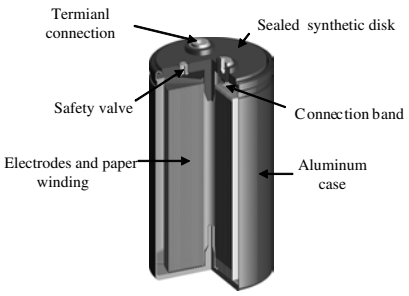

Fig. 1. Structure of a screw terminals electrolytic capacitor [16]

Due to the physical design elements and construction, aluminium electrolytic capacitors are modeled by the electrical equivalent circuit [14], [17] given in Fig.2. This model, which is the most used one, is rather simple and gives a good frequency response.

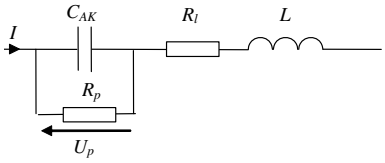

Fig. 2. Electrical equivalent circuit of an electrolytic capacitor

Where C_{AK} is the ideal capacitance between anode and cathode, R_p is the parallel resistance which represents all the losses in the dielectric and the leakage between the two electrodes, R_l is the connection and electrodes serial resistance and L is connection and winding equivalent series inductance. This circuit can be simplified with the normalized representation given in Fig.3. It is a serial combination of an Equivalent Series Resistance which represents all the component losses, a capacitance C and an equivalent serial inductance, ESL, which is due to the wound structure of the capacitor.

Fig. 3. Normalized electrical equivalent circuit of an electrolytic capacitor

From the impedance equality between the circuit elements represented in Fig.2 and those represented in Fig.3, we can conclude the following equations where ω is the electrical pulsation.

$$C = C_{AK}.\left(1 + \frac{1}{R_p^2 C_{AK}^2 \omega^2}\right) \quad (1)$$

$$ESR = R_l + \frac{R_p}{1 + R_p^2 C_{AK}^2 \omega^2} \quad (2)$$

$$ESL = L \quad (3)$$

This capacitor representation is important because it's directly given from the impedance frequency measurements. Therefore, the resonant frequency f_r of the capacitor is given by this equation.

$$f_r = \frac{1}{2.\pi.\sqrt{ESL.C}} \quad (4)$$

In addition, this simplified equivalent circuit can give a first approximation of the capacitor behavior without taking into account parameters' variation C, ESR and ESL versus frequency. This theory can be demonstrated by the figure given below (Fig.4) which represents the module Z of the complex impedance $\underline{Z}$ versus frequency, of an aluminum electrolytic capacitor of 4700 μF/ 500 V. As it can be observed from bode-plot, there exist three widely separated frequency bands. Capacitance of the capacitor is dominant in low frequency band. ESL is dominant in high frequency band and ESR is dominant in the mid frequency one.

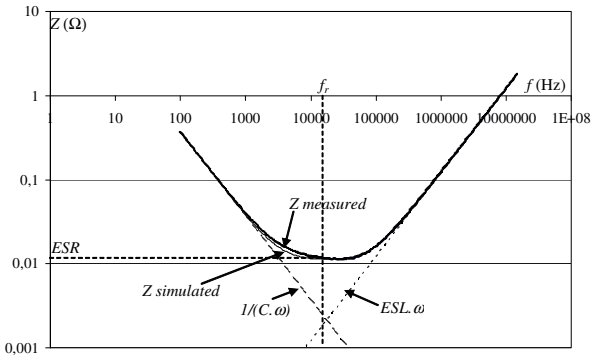

Fig. 4. Z(f) for aluminum electrolytic capacitor of 4700 μF / 500 V

The equations (1) and (2) show that ESR and C can be considered separately from the frequency when this latter is not too low. Therefore, the resistance R_p has an effect only on very low frequencies (less than several tens of Hz). This is shown in the Fig.5 which represents the effect of R_p versus frequency f on the ESR and C parameters. It is an example of an electrolytic capacitor with a nominal capacitance value of 4700 μF and a nominal equivalent serial resistance of 20 $m\Omega$.

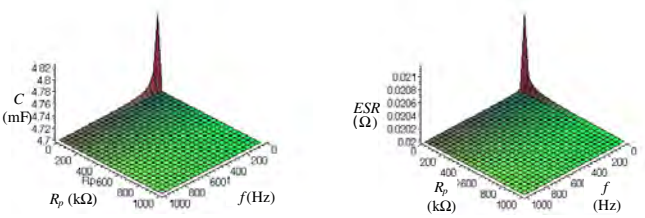

Fig. 5. Z(f) for aluminum electrolytic capacitor of 4700 μF / 500 V [17]

B. Electrolytic capacitors aging

The figure below [17] shows the majority of electrolytic capacitor root causes and failure modes. As it can be seen, the

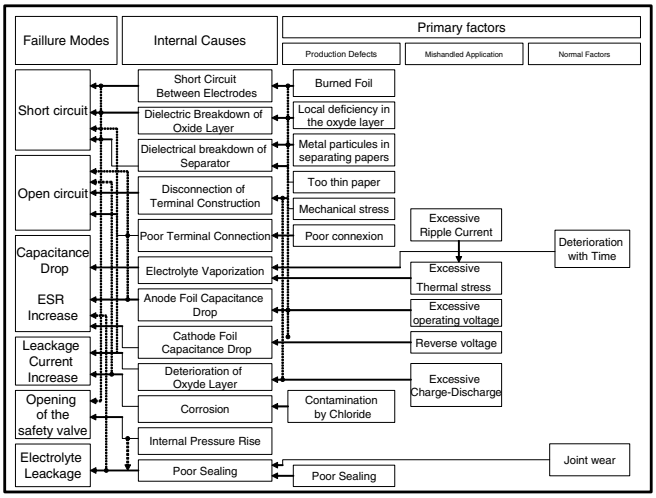

Fig. 6. Capacitor failures and their causes [17]

estimation of ESR and C can provide at least all the normal and uses failure defects. Therefore, the estimation of these two parameters is important to realize a real time predictive maintenance system of electrolytic capacitor.

III. Electrolytic capacitor monitoring

A. Estimation of ESR and C

As we have just seen before, the electrolytic capacitors can be modeled as a serial combination of a capacitance, an equivalent series inductance and an equivalent series resistance as showing in Fig.3. The bode-plot of an electrolytic capacitor with equivalent series resistance, $ESR = 74\ m\Omega$ equivalent series inductance $ESL = 10\ nH$ and the capacitance $C = 470\ \mu F$ is presented in Fig.8. Therefore, converters in UPS works at low frequency band compared with the resonant frequency's one (4), so ESL is usually neglected and the equivalent model of the capacitor is given through Fig.7.

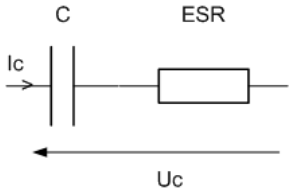

Fig. 7. Capacitor equivalent model for frequency range used in power converter

The transfer function of this model is given by:

$$H(p) = \frac{Uc(p)}{Ic(p)} = \frac{ESR.C.p + 1}{C.p} \tag{5}$$

However, converters are controlled by using digital treatments. We can consider the z-transform corresponding of equation (5) to represent the discrete time domain by using the bilinear method of Tustin and which is given by the following equation where Te is the sampling period.

$$H\left(z^{-1}\right) = \frac{b_0 + b_1.z^{-1}}{1 - z^{-1}} = \frac{\left(ESR + \frac{Te}{2.C}\right) + \left(\frac{Te}{2.C} - ESR\right).z^{-1}}{1 - z^{-1}} \tag{6}$$

The bode-plot in Fig.8 shows that, the continuous and discrete time domain for a sampling period of $Te = 10\ \mu s$, are equivalent if we use the bilinear method discrete time.

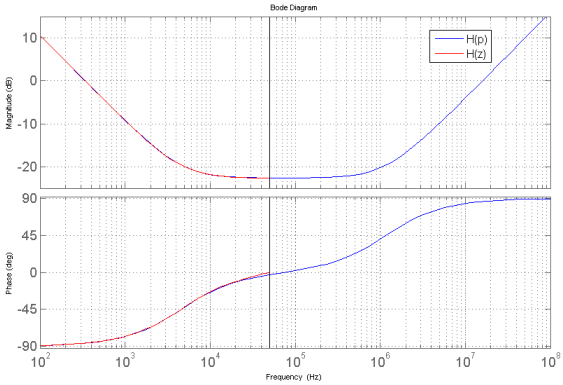

Fig. 8. Bode plot of electrolytic capacitor in continuous and discrete time domain

To identify b_0 and b_1 so the two parameters ESR and C, we use different forms of Kalman filter.
A Matlab simulation was performed using dynamic equation from equivalent circuit shown in Fig.9 a the boost-converter with 50 V DC voltage input, for a switching frequency of 5 kHz and which is regulated to have 200 V DC voltage output.

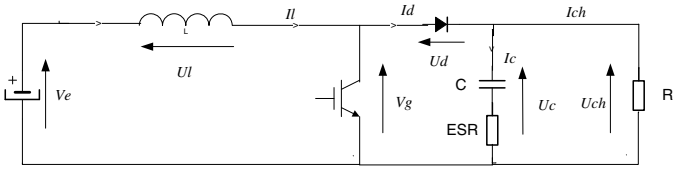

Fig. 9. Schematic of a boost converter circuit with a DC capacitor circuit

A Recursive Least Square Algorithm which is a particular case of Kalman filter was used like presented in Fig.10.
In practice, we don't have a capacitor current sensor, because it is difficult and expansive to implement in UPS. To perform and regulate the output voltage, we only dispose of one current sensor used to have the input current inductance L of the boost converter. However, we can identify the capacitor current with using Kirchhoff's laws referring to the schematic of the boost

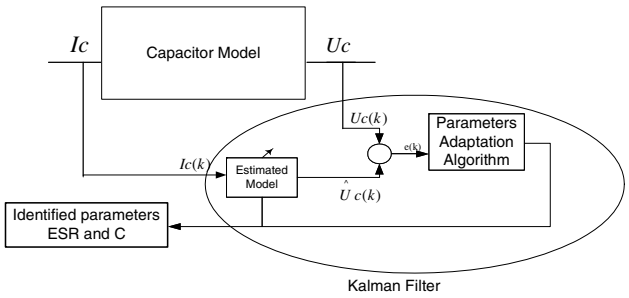

Fig. 10. Parameters identification with using Kalman filter

converter given in Fig.9.

$$Ic = Id - Ich \tag{7}$$

When the IGBT is off (the pulse width modular PWM=0), we have $Id = Il$, so we can conclude the following equation.

$$Id = Il * \overline{PWM} \tag{8}$$

In stationary process, the average capacitor current Ic is equal to zero, so for one regulation period Te, you have the following equation.

$$Ic = Il * \overline{PWM} - avg\left(Il * \overline{PWM}\right) \tag{9}$$

Respectively, simulation results of the capacitor ripple voltage, and capacitor current identified with the use of (9) are shown in Fig.11.

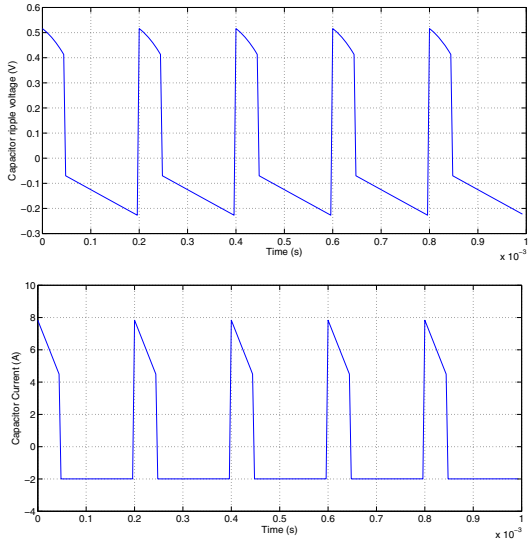

Fig. 11. Matlab Simulation results of capacitor ripple voltage ΔUc and capacitor current Ic

Simulation results presented in this section are summarized in Table I.

B. Aging Algorithm

The aging algorithm which takes into account the temperature is given below.

TABLE I
SIMULATION RESULTS FOR ESTIMATED PARAMETERS

ESR_{actual}	$\text{ESR}_{estimated}$	% error
74 $m\Omega$	74.2 $m\Omega$	0.2
C_{actual}	$\text{C}_{estimated}$	% error
470 μF	466 μF	0.7

Evolution of ESR and C versus ambient temperature T_a is given by the following equation [14] where α,β,γ and χ,ν,λ are experimental parameters and depend on the used capacitor.

$$ESR\left(T_a\right) = \alpha + \beta.\exp\left(-\frac{T}{\gamma}\right) \tag{10}$$

$$C\left(T_a\right) = \chi + \lambda.\exp\left(-\frac{T}{\nu}\right) \tag{11}$$

Time until failure compared to failure limits of ESR and C can be calculated by using the equations below [14].

$$\frac{t_{ESR}^{'}}{ta_{ESR}} = \exp\left[\frac{Ea_{ESR}}{k}.\frac{T^{'} - T_a}{\left(T^{'} + 273\right).\left(T_a + 273\right)}\right] \tag{12}$$

$$\frac{t_{C}^{'}}{ta_{C}} = \exp\left[\frac{Ea_{C}}{k}.\frac{T^{'} - T_a}{\left(T^{'} + 273\right).\left(T_a + 273\right)}\right] \tag{13}$$

$$ESR\left(t_{ESR}\right) = \left(ESR\left(0\right) + A_1\right).\exp\left(B_1.t_{ESR}\right) \tag{14}$$

$$C\left(t_C\right) = E.C\left(0\right) + F.t_C \tag{15}$$

T_a: Ambient temperature (25 °C for example).
$T^{'}$: Aging temperature (85 °C for example).
ta_{ESR}: Aging time for the ESR limit at T_a.
ta_C: Aging time for the C limit at T_a.
$t_{ESR}^{'}$: life time limit at $T^{'}$ with ESR aging indicator.
$t_C^{'}$: life time limit at $T^{'}$ with C aging indicator.
t_{ESR}: time until failure with ESR aging indicator.
t_C: time until failure with C aging indicator.
k = Boltzmann constant (8,617.10^{-5} eV/°K).
Ea_{ESR}: Activation energy with ESR aging indicator.
Ea_C: Activation energy with C aging indicator.
A_1, B_1, E and F are experimental parameters and also depend on the used capacitor.
The time until failure of the capacitor is given by the lower computed time between ESR time failure limit and C time failure limit as showing in Fig.12.

C. experimental study

1) Experimental setup: To verify the validity of the proposed method, an experimental study was performed on a Boost-converter with an input DC voltage of 50 V, 470 μF - 450 V filtering capacitor, an R-load of 100 Ω and a switching frequency of 5 kHz. Therefore a fixed point DSP controller (TMS320F2812) was used for Il, Uc, Ic and capacitor ripple voltage ΔUc acquisition measurements and switching operations required to perform 200 V DC output voltage. To do that, we choose the two imbricated loop principle, one fast current loop with a Proportional/ Integrator (PI) controller to perform

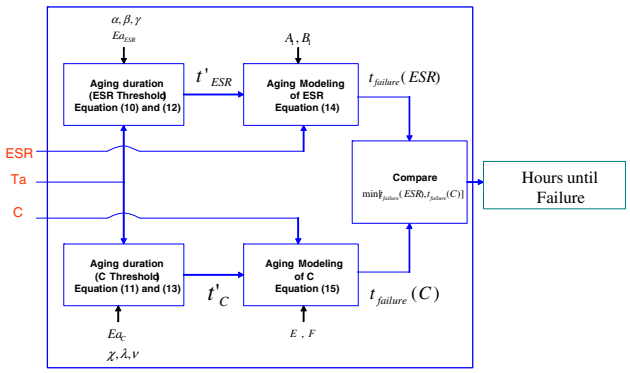

Fig. 12. Aging algorithm

the current reference and another external voltage loop with a Deadbeat controller to perform the 200 V DC output voltage. Moreover, a recursive least square algorithm (a particular case of Kalman filter) has been implemented to work in background task and to identify the two parameters ESR and C.

In literature [15], we know that using different cases of Kalman filter provides centered input and output system measurements which are respectively capacitor current and capacitor voltage. Therefore, the capacitor voltage and the capacitor current are passed through a high-pass filter with cut-off frequency of around $f_c = 200\ Hz$ to suppress DC component of voltage measurements and without including phase shift. Consequently, we have only the capacitor ripple voltage which is in phase with capacitor current.

An FFT analysis respectively on the capacitor ripple voltage and capacitor current is shown in Fig.13 and we see that the bandwidth of the system is about 30 kHz and 35 kHz. Therefore and to respect Shannon theorem we choose a sampling frequency $f_s = 80\ kHz$. To eliminate signal distortion an anti-

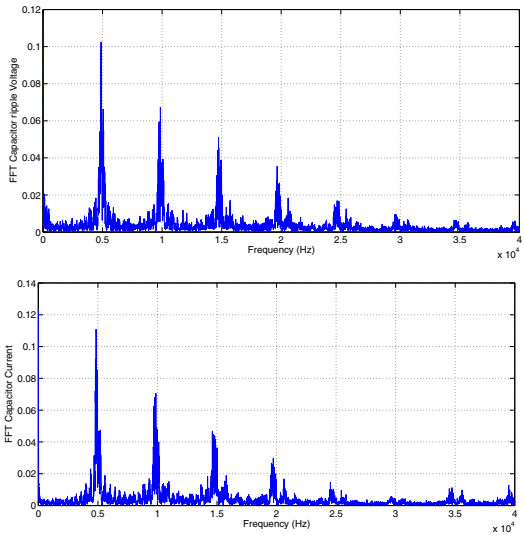

Fig. 13. FFT analysis of capacitor ripple voltage and capacitor voltage for a sampling frequency $f_s = 80\ kHz$

aliasing Filter [15] with a cut-off frequency $f_c = \frac{f_s}{2} \approx 40kHz$ is used as it is shown in the global capacitor condition monitoring scheme Fig.14.

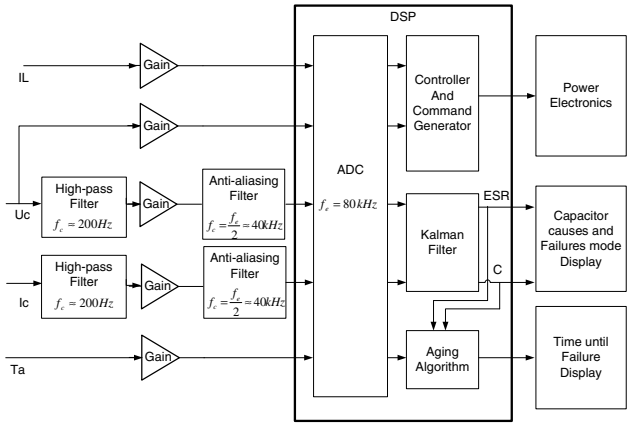

Fig. 14. Real time electrolytic capacitor condition monitoring in UPS

2) Experimental results: The experimental measurements on the scope of Capacitor ripple voltage, and capacitor current are shown in Fig.15

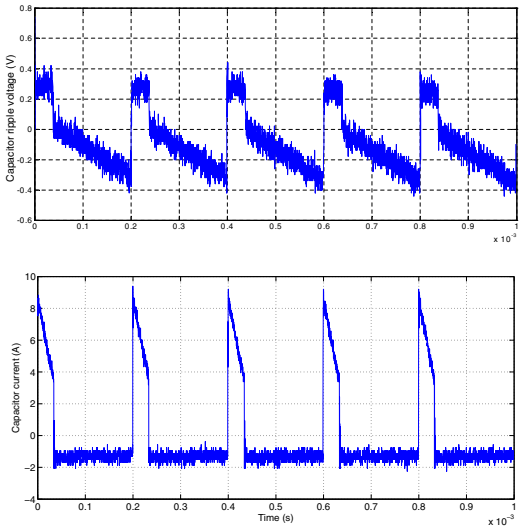

Fig. 15. Capacitor ripple voltage and capacitor current

The corresponding numerical DSP measurements (after the Analog to Digital Converter) of capacitor ripple voltage and capacitor current are given in Fig.16.

Experimental results for the estimated parameters are summarized in Table II.

TABLE II
EXPERIMENTAL RESULTS FOR ESTIMATED PARAMETERS

ESR_{actual}	$ESR_{identified}$= [ESR_{min};ESR_{max}]	% error
75.1 mΩ	[71.3 mΩ,78.8 mΩ]	$+/-5$
C_{actual}	$C_{identified}$=[C_{min};C_{max}]	% error
472 μF	[466 μF, 518 μF]	$+/-10$

It can be clearly seen that there is a non significant error

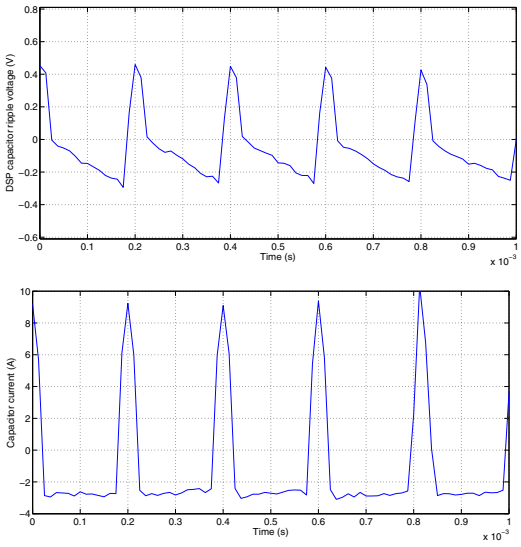

Fig. 16. Capacitor ripple voltage and Capacitor current on DSP with a sampling frequency $f_s = 80\ kHz$

between estimated and actual values of ESR and C.
These results are consistent with the measured value using an impedancemeter.

IV. Conclusion

Due to their large capacity and low cost, electrolytic capacitors with the abilities of energy storage and voltage regulation are used for almost all types of power electronics system. Electrolytic capacitors, which are usually affected by wear-out faults, plays a very important role for the quality and reliability of power-electronics system. Therefore it is important to monitor the condition of an electrolytic capacitor in real-time to predict the failure. A new method is proposed to detect in real time the changes in ESR and capacitance C value by taking into account the ambient temperature in order to create a real-time failure prediction of an electrolytic capacitor. For the proposed method, capacitor current and capacitor ripple voltage measurements using cheap and simple analog circuits are required. Simulation results and hardware experimental show that the proposed electrolytic capacitor failure-prediction technique can be applied to a power-electronics system successfully.

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