A CMOS Resizing Methodology for Analog Circuits: linear and non-linear applications

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Abstract:

This article proposes a CMOS resizing methodology for analog circuits during a technology migration. The scaling rules aim to be easy to apply and are based on the simplest MOS transistor model. This methodology represents a useful technique for resizing a design and may be used as a first-guess for an optimization procedure. The principle is to transpose one circuit topology from one technology to another, while keeping the main figures of merit, and the issue is to quickly calculate the new transistor dimensions. An optimization tool improves the results when it is necessary. This methodology is applied to both linear and non-linear examples: an OTA and a ring oscillator. The results are compared on four CMOS processes whose minimum length is respectively 0.8 µm, 0.35 µm, 0.25 µm and 0.12 µm.

Index term: Analog design, Design reuse, MOS technology, Resizing methodology, Technology migration

NOWADAYS ANALOG DESIGN FLOW is much less developed than digital counterpart. That's why analog design reuse is an important way to explore. The resizing of the design is an essential step for the reuse of analog circuits.

The main goals of a resizing methodology are to keep performances of the original design but also to reduce area and power consumption during a technology migration.

Recently, several methods have been proposed in the reuse of analog blocks, including resizing. The work of C. Galup-Montoro and M.C. Schneider [1] proposed an analytical approach of MOS transistor resizing and several strategies depending on the type of the original circuit. Scaling factors are defined. In this work, the used model of MOS transistor is the ACM model [2] and application circuits are OTAs.

This method was extended in [2], adding experimental results from a complete Miller OTA, and including additional performance aspects of analog circuits. And it was also extended in [3], [4], using a tuning procedure based on an optimization loop.

The main drawback of these works is the increase of chip area in the OTA examples.

Some EDA companies [5] have recently started to offer tools and services aimed at reuse and technology migration. [5] and [6] based their approaches on an optimization loop and intensive SPICE simulations in order to check and suitably modify circuit parameters to obtain the specified performances.

Analogue reuse is studied by University laboratories. The Cairo+ project [7] proposes an automatic sizing of a circuit, and the RuneII platform [8] includes analogue IPs [9] (Intellectual Property) and some sizing methodologies. [10] presents a framework for the reuse-based design of AMS circuits.

All of those works validated their results with an application on one OTA. To compare our results to the previous ones, we also study the OTA example and we add non-linear examples which are ring oscillators. The main difference is the use of a simple MOS transistor model which may be followed by an optimization procedure. The advantage is to quickly calculate W and L for each transistor of the target technology. The results give an appreciable decrease of the total area which could not be achieved by the previous works.

The paper is organized as follows. First we explain our methodology. Then we apply it on two different circuits, linear ones: OTAs and non-linear ones: ring oscillators, with four CMOS processes: from 0.8 µm to 0.12 µm.

Description of the proposed methodology

The principle of the resizing methodology could be summarized in three steps:

- Step 1: Definition of the figure(s) of merit to be preserved
- Step 2: Calculation of the technological scaling factors

- Step 3: Decision on some strategic aspects and computation of the new transistor sizes

The last computation step relies on MOS transistor model equations. In the present article, the Level 1 MOS transistor model is used and gives correct estimations. Naturally, it is possible to use more accurate equations like those of BSIM3V3 to determine the scaling rules and then the new sizes of transistors.

The scaling factors are defined in Table 1, considering a migration from a technology 1 to a technology 2 [11].

The first three factors are calculated from known technological parameters (Step 2).

The goal is to evaluate the factors K_L and K_W.

TABLE I. DEFINITION OF THE SCALING FACTORS

Parameters	Scaling factors
Supply voltage : V_{DD}	$K_V = V_{DD2} / V_{DD1}$
Oxide capacitance : C_{OX}	$K_{OX} = Cox_2 / Cox_1$
Mobility : μ_0	$K_\mu = \mu_{02} / \mu_{01}$
Effective gate voltage : $V_{EG} = V_{GS} - V_T$	$K_{EG} = V_{EG2} / V_{EG1}$
Bias current : I_{bias}	$K_I = I_{bias2} / I_{bias1}$
Length of the transistor : L	$K_L = L_2 / L_1$
Width of the transistor : W	$K_W = W_2 / W_1$

We notice that the scaling factors' values depend on the type of transistors (NMOS or PMOS).

The third step of the methodology is the most important. Indeed, we choose the strategy of redesign and decide which equations will be used to relate the figures of merit to the scaling factors. This choice of the strategy is doing by the designer and depending on the goals and the system specifications, a strategy is emerging.

Here are the main equations, derived from Level 1 MOS transistor model, which are carried out in the next paragraphs:

- the drain current in the saturation region

$$I_D = \frac{\mu_0 C_{ox} W}{2L} V_{EG}^{\ 2} \quad (1)$$

- the transconductance g_m

$$g_m = \left[\frac{\partial i_D}{\partial v_{GS}}\right]_{V_{GS}=const}^{I_D=const} = \frac{\mu_0 C_{ox} W}{2L} V_{EG} = \sqrt{\frac{\mu_0 C_{ox} W I_D}{L}} \quad (2)$$

- the average drain-to-source resistance [12]

$$R_N = \frac{V_{DD}}{\frac{\mu_{0N} C_{OXN}}{2} \frac{W}{L} (V_{DD} - V_{TN})^2} \quad (3)$$

$$R_P = \frac{V_{DD}}{\frac{\mu_{0P} C_{OXP}}{2} \frac{W}{L} (V_{DD} + V_{TP})^2} \quad (4)$$

Those equations are an estimate for the resistance between the drain and source of the MOSFET during switching.

- the simplified gate capacitance [13]

$$C_G = W\ L\ C_{OX} \quad (5)$$

Those equations have been chosen for the application examples.

Naturally those equations are approximations especially for the most recent technologies which have a small minimum length. To solve this problem, there are two solutions.

First, the results given by this methodology could be a basis of an optimization step to precisely tune the transistor sizes. Classical design platform software includes optimization algorithms. In this work, we choose the optimization function of Cadence. This tool by iteration gives an optimization of the performances based on variables.

Secondly, the model of transistor could be more relevant. Using accurate equations like the BSIM3V3 model, in this methodology will give better results and performances. The counterpart will be the complexity of the calculation of the scaling factors.

Applications of this methodology are proposed on linear and non-linear applications: an OTA and a ring oscillator, for a technology migration from CMOS 0.8 µm to CMOS 0.35 µm, to CMOS 0.25 µm and to CMOS 0.12 µm.

Application on linear examples

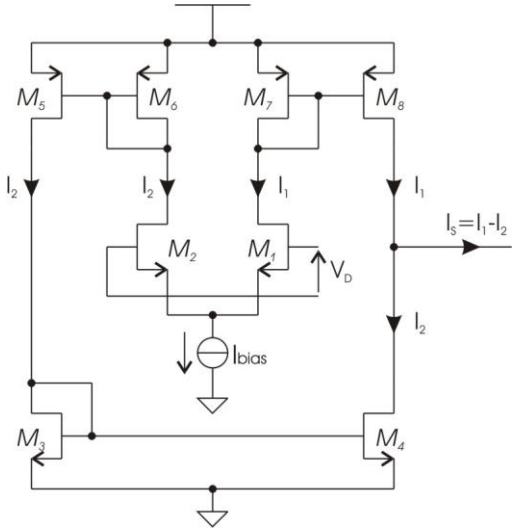

Figure 1. Schematic of the OTA

The original OTA has been designed in CMOS 0.8 µm technology with a supply voltage of 5 V and first scaled in CMOS 0.35 µm technology with a 3.3 V supply voltage, then in 0.25 µm technology with a 2.5 V supply voltage, and finally in 0.12 µm technology with a 1.2 V supply voltage. In this OTA, all the transistors are in saturation mode.

Our objective is the conservation of the transconductance gain of the OTA during technology migrations.

- Step 1: the figure of merit to be kept is the transconductance OTA gain.
- Step 2: K_V, K_{OX}, K_μ are deduced from technological information.
- Step 3: A simple way to conserve the transconductance OTA gain is to keep the same drain current, then from (1) and Table I, we obtain:

$$\frac{\mu_{01}C_{OX1}W_1}{2L_1}V_{EG1}{}^2 = \frac{\mu_{02}C_{OX2}W_2}{2L_2}V_{EG2}{}^2 \quad (6)$$

$$W_2 = \frac{\mu_{01}C_{OX1}W_1 2L_2}{\mu_{02}C_{OX2}2L_1}\frac{V_{EG1}{}^2}{V_{EG2}{}^2} \quad (7)$$

$$W_2 = \frac{K_L}{K_\mu K_{ox}K_{EG}{}^2}W_1 \quad (8)$$

$$K_W = \frac{K_L}{K_\mu K_{OX}K_{EG}{}^2} \quad (9)$$

At this step, both K_L and K_{EG} are unknown.

We decide to keep also the same value for V_{EG} (V_{EG1}=V_{EG2}), checking after if this decision is compatible with the decreasing V_{DD} values. Furthermore, we reduce the transistor length L in the same proportion as the minimum length of the technology, so K_L is equal to L_{MIN2} / L_{MIN1}.

Then we deduce K_W value. As the scaling factors are determined, the new transistor sizes could be calculated. Table II gives the numerical results of this resizing.

TABLE II. SIZES OF THE TRANSISTORS

Transistors W/L	0.8 µm 5 V	0.35 µm 5 V	0.25 µm 2.5 V	0.12 µm 1.2 V	0.12* µm 1.2 V
M_1 (µm)	20/10	8.75/4.4	3.6/3.15	0.8/1.5	1.05/2.65
M_2 (µm)	20/10	8.75/4.4	3.6/3.15	0.8/1.5	1.05/2.65
M_3 (µm)	40/10	17.5/4.4	7.25/3.15	1.55/1.5	2.65/1.1
M_4 (µm)	40/10	17.5/4.4	7.25/3.15	1.55/1.5	2.65/1.1
M_5 (µm)	40/10	19.75/4.4	6.45/3.15	2.45/1.5	2.75/1.35
M_6 (µm)	40/10	19.75/4.4	6.45/3.15	2.45/1.5	2.75/1.35
M_7 (µm)	40/10	19.75/4.4	6.45/3.15	2.45/1.5	2.75/1.35
M_8 (µm)	40/10	19.75/4.4	6.43/3.15	2.45/1.5	2.75/1.35

**In technology 0.12 µm, we notice a decrease of the DC gain voltage. Then with the optimization function of Cadence environment, we determine the new sizes of transistors (Table II) and then the new performances which are given in Table III.*

The I_{BIAS} current of the OTA is 30 µA.

To evaluate the performances of the methodology we compare the DC transconductance gain G_0 (the slope of DC transfer characteristic in linear region).

To obtain the DC voltage gain, the Gain-Bandwidth product and the phase margin, an output capacitance has been added. Its value is fixed at 50 pF.

All of the simulations are made with Cadence Environment with Spectre simulator. The transistor model is the BSIM3V3 model where the channel length modulation and the short channel effect are included.

TABLE III. RESULTS OF THE SIMULATIONS

Technology (µm) Supply Voltage (V)	0.8 5	0.35 5	0.35 3.3	0.25 2.5	0.12 1.2	0.12* 1.2
G_0 (µA.V^{-1})	**38**	**39**	**38**	**40**	**38**	**38**
DC voltage Gain (dB)	54	54	54	54	49	54
Gain-Bandwidth product (MHz)	6.5	6.5	6.5	6.5	6.1	6.5
Phase Margin	88°	89°	89°	89°	89	89
Power Consumption (µW)	302	302	198	150	72	72
Area (µm^2)	2800	580	580	150	22	29

Table III describes the results of the simulations of the OTA, with the resizing methodology. We observe a small variation of the gains and the gain-bandwidth product but there is a huge decrease of the area and the consumption, then a reduction of the chip cost.

Now, we want to characterize the robustness of the obtained designs. The MonteCarlo simulations determine the behaviour of a design with parameters variation. It can change uniformly the parameters (change of wafer): it is the MonteCarlo simulation with process. It can change the parameters for each component (on the same wafer): it is the MonteCarlo simulation with mismatch.

Figure 2 describes the behavior of the OTA DC gain in a closed loop with MonteCarlo simulations including mismatch and process. The simulated circuit is a voltage amplifier based on the OTA with a feedback resistive network. The initial simulated DC gain voltage value is 61 dB.

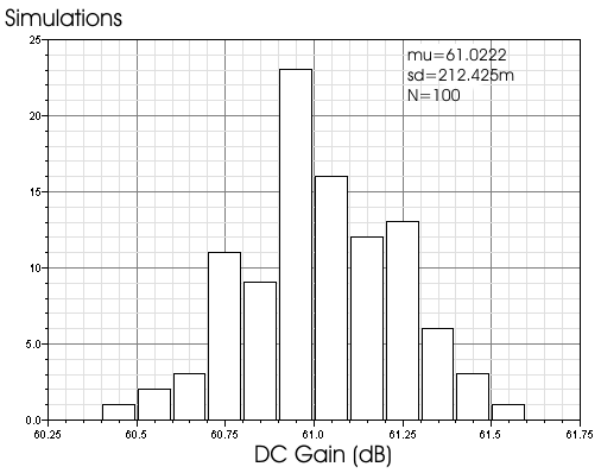

Figure 2. MonteCarlo simulation of the DC voltage gain of the OTA in technology 0.35 µm with 3.3 V

The gain mean-value is maintained and the standard deviation (□0.2 dB) is very low during the technology migration.

For 0.8 µm 5 V, 0.35 µm 3.3 V and 0.12 µm 1.2 V, all values of the simulated voltage gain are included between 98 and 102 % of the initial value, proving the robustness of the design along this resizing.

Simulation results describe that the methodology keeps the chosen figure of merit: G_0. But it also maintains other performances as AC figures of merit (DC voltage gain and gain-bandwidth product) except for a few technologies where the optimization tool is needed. It conserves the robustness of the design and reduces the cost with the decrease of area (80 % between 0.8 µm and 0.35 µm, 75 % between 0.35 µm and 0.25 µm and 85 % between 0.25 µm and 0.12 µm) and the power consumption (a K_V ratio depending of the decrease of the supply voltage).

Our second example starts from the same OTA (figure 1) but we change the third step of the methodology. Indeed the strategy changes, the designer wants to preserve the transconductance gain and to reduce the power consumption even if the dynamic range of the OTA decreases.

- Step 1: the figures of merit to be kept are the transconductance OTA gain and the decreasing of the power consumption.
- Step 2: K_V, K_{OX}, and $K\mu$ are deduced from technological information.
- Step 3: We want to conserve the transconductance OTA gain g_m. To reduce the power consumption, we choose to reduce the bias current by a K_I factor. In our application we choose 2/3 for the K_I value. K_I choice depends on the specifications we have and the goals that we want to reach.

As shown on equation (2), to maintain the same g_m and reduce the power consumption of the design by a factor K, we multiplied the transistors width (W) and the length L by this K factor and divided the biasing current by the same factor.

$$I_{D2} = K_I I_{D1} \tag{10}$$

$$K_I^{\,2} = \frac{K_\mu K_{ox} K_{EG}^{\,2} K_W}{K_L} \tag{11}$$

$$K_L = \frac{L_{MIN2}}{K_I L_{MIN1}} \tag{12}$$

$$K_W = \frac{K_L}{K_I K_\mu K_{ox} K_{EG}^{\,2}} \tag{13}$$

The results of this methodology are given by the figure 3 and table V.

TABLE IV. SIZES OF THE TRANSISTORS

Transistors	0.8 µm	0.35 µm	0.25 µm	0.12 µm
W/L	5 V	3.3 V	2.5 V	1.2 V
M_1 (µm)	10/2	9.85/1.3	5.6/0.85	2.5/0.55
M_2 (µm)	10/2	9.85/1.3	5.6/0.85	2.5/0.55
M_3 (µm)	10/2	9.85/1.3	5.6/0.85	2.5/0.55
M_4 (µm)	10/2	9.85/1.3	5.6/0.85	2.5/0.55
M_5 (µm)	10/2	11.1/1.3	4.95/0.85	3.9/0.55
M_6 (µm)	10/2	11.1/1.3	4.95/0.85	3.9/0.55
M_7 (µm)	10/2	11.1/1.3	4.95/0.85	3.9/0.55
M_8 (µm)	10/2	11.1/1.3	4.95/0.85	3.9/0.55
I_{BIAS} (µA)	45	30	20	13

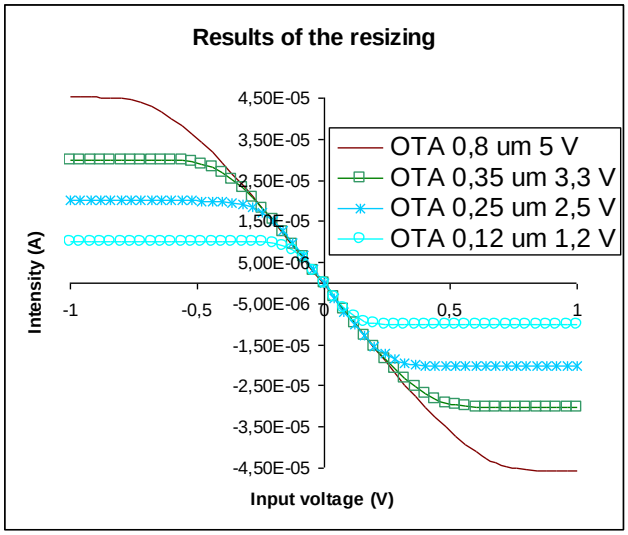

Figure 3. DC transfert characteristic of the OTA

TABLE V. RESULTS OF THE SIMULATIONS

Technology (µm) Supply Voltage (V)	0.8 5	0.35 3.3	0.25 2.5	0.12 1.2
G_0 (µA.V^{-1})	**78**	**80**	**81**	**80**
Power Consumption (µW)	**459**	**200**	**100**	**32**
Area (µm^2)	160	109	36	14

Simulation results (figure 3 and Table V) describe that the methodology keeps the transconductance (G_0), the offset and the slope, and reduces the cost with the decrease of area (32 % between 0.8 µm and 0.35 µm, 67 % between 0.35 µm and 0.25 µm and 62 % between 0.25 µm and 0.12 µm) and the power consumption (57 % between 0.8 µm and 0.35 µm, 50 % between 0.35 µm and 0.25 µm and 68 % between 0.25 µm and 0.12 µm). We do not give in this paper the MonteCarlo simulations of this OTA because the conclusions of these simulations are similar to those for the MonteCarlo simulations of the OTA described previously.

Let us discuss the results obtained for these linear examples. First we applied the methodology on an OTA, with a strategy of the conservation of transconductance gain. And in a second time, we changed the strategy (third step of the methodology) of resizing and the designer's specifications, and we decided to conserve the transconductance gain and also to reduce the

power consumption. We notice that the application on the two linear examples proves the flexibility of the methodology. In both case the transconductance gain is kept and the area is reduced whatever the CMOS processes. And for the second application, the power consumption is also decreased.

Application on non-linear examples

For a non-linear application, the resizing methodology has been applied to a ring oscillator which is built with inverters. The CMOS inverter is a basic building block for circuit design.

A ring oscillator is built with an odd number of inverters which forms a closed loop with positive feedback. The inverters are identical. In our application, we use minimum size CMOS inverters. It means that the widths and lengths of the two devices are taken as equal ($W_P=W_N$ and $L_P=L_N$).

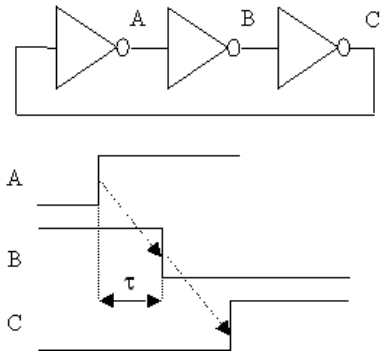

Figure 4. A ring oscillator

The main characteristic of the ring oscillator is the oscillation frequency.

- Step 1: the figure of merit to keep is the oscillation frequency. It is given by [14].

$$f_{osc} = \frac{1}{2n(t_{PHL} + t_{PLH})} \quad (14)$$

Where $t_{PHL} + t_{PLH} = (R_N + R_P)C_{tot}$.

R_N and R_P are given by (3) and (4) while the total capacitance C_{tot} is calculated just after.

- Step 2: K_V, K_{OX}, K_μ are deduced from technological information.

- Step 3: A simple way to conserve the oscillation frequency is to keep the same resistances and capacitances associated with the inverter.

The inverter input capacitance is given by

$C_{IN} \approx C_{GN}+C_{GP} = (W_NL_N+W_PL_P)\, C_{OX}$ (15)

Where the NMOS total capacitance is named C_{GN} and the PMOS one is named C_{GP}.

The input gate capacitance of the inverter is dominant over the output capacitance, then $C_{IN} + C_{OUT} \approx C_{IN}$ [14]. To conclude, the total capacitance with n inverters is equal to nC_{IN}.

$C_{TOT} = n\, C_{IN} = n\, (W_NL_NC_{OXN} + W_PL_PC_{OXP})$ (16)

To determine the scaling factors, we maintain the total capacitance and resistance, as chosen in step 3, and decide that:

NMOS: $W_{N2}L_{N2}C_{OXN2} = W_{N1}L_{N1}C_{OXN1}$ (17)

PMOS: $W_{P2}L_{P2}C_{OXP2} = W_{P1}L_{P1}C_{OXP1}$ (18)

So with (17) and (18), we obtain:

$$W_2L_2 = \frac{W_1L_1}{K_{ox}} \quad (19)$$

Because of $R_{N2} = R_{N1}$ and $R_{P2} = R_{P1}$ then

$$\frac{L_2}{W_2} = \frac{L_1}{W_1}\frac{K_{ox}K_\mu}{K_V}\frac{(V_{DD2}-V_{T2})^2}{(V_{DD1}-V_{T1})^2} \quad (20)$$

With (19) and (20) we have:

$$K_WK_L = \frac{1}{K_{ox}} \quad (21)$$

$$\frac{K_L}{K_W} = \frac{K_{ox}K_\mu}{K_V}\frac{(V_{DD2}-V_{T2})^2}{(V_{DD1}-V_{T1})^2} \quad (22)$$

Then the scaling factors K_W and K_L are determined.

$$K_W = \frac{1}{K_{ox}}\sqrt{\frac{K_V}{K_\mu}}\frac{(V_{DD1}-V_{T1})}{(V_{DD2}-V_{T2})} \quad (23)$$

$$K_L = \sqrt{\frac{K_\mu}{K_V}}\frac{(V_{DD2}-V_{T2})}{(V_{DD1}-V_{T1})} \quad (24)$$

After determining the scaling factors, three experiments have been made on ring oscillators with different characteristics during a technology migration. Two applications are made on the same topology of ring oscillator but with different transistor sizes and one experiment is on a ring oscillator with different number of inverters. The initial technology was CMOS 0.8 µm and the target technology was CMOS 0.35 µm, CMOS 0.25 µm and CMOS 0.12 µm.

For the CMOS 0.12 µm, we notice that (3), (4) and (16) are not valid in this technology. Indeed the channel of the transistor in this technology with 1.2 V as a supply voltage is not completely closed and we have some short channel effects [15]. Then the transistor is more in linear mode than in saturation mode and then the new equation for this technology are:

$$C_{TOT} = nC_{IN} = n\frac{2}{3}(W_NL_NC_{OXN} + W_PL_PC_{OXP}) \quad (25)$$

$$R_N = \frac{V_{DD}}{\frac{2\mu_{0N}C_{OXN}}{3}\frac{W}{L}(V_{DD}-V_{TN})^2} \quad (26)$$

$$R_P = \frac{V_{DD}}{\frac{2\mu_{0P}C_{OXP}}{3}\frac{W}{L}(V_{DD}+V_{TP})^2} \quad (27)$$

The 2/3 factor arises from the calculation of channel charge, and inherently comes from integrating the triangular distribution in the square-law regime.

All of these applications validate the methodology. We present here just the first application which is a ring oscillator with 5 inverters.

From the previous equations defining the total capacitance and resistance, we determine the theoretical oscillation frequency.

NMOS and PMOS initial sizes in technology 0.8 µm with a supply voltage of 5 V are:

$L_{1N} = L_{1P} = 2$ µm and $W_{1N} = W_{1P} = 50$ µm.

Using the scaling factors of (23), (24), we determine the new transistor sizes in 0.35 µm and 0.25 µm technology with different supply voltages (Table VI).

TABLE VI. NEW SIZES OF TRANSISTORS

Size	0.35 µm 5 V	0.35 µm 3.3 V	0.25 µm 2.5 V	0.12 µm 1.2 V	0.12* µm 1.2 V
L_N	1.95 µm	1.25 µm	1.00 µm	1.00 µm	1.00 µm
L_P	1.75 µm	1.40 µm	1.05 µm	0.73 µm	0.70 µm
W_N	47.85 µm	75.45 µm	34.10 µm	21.95 µm	24.60 µm
W_P	53.70 µm	64.30 µm	32.15 µm	29.9 µm	21.00 µm

**the values given in technology 0.12 µm were obtained by the optimization tool.*

The theoretical and experimental oscillation frequencies are given by Table VII. The theoretical values are calculated by our methodology, and the experimental values are given by simulations.

TABLE VII. OSCILLATION FREQUENCIES

L_{MIN} (µm)	0.8	0.35	0.35	0.25	0.12	0.12*
V_{DD} (V)	5	5	3.3	2.5	1.2	1.2
f_{osc} theo (MHz)	267	268	267	268	267	242
f_{osc} exp (MHz)	267	268	266	270	293	268
Area (µm²)	1000	936	930	339	229	196

We observe that the oscillation frequencies of the three ring oscillators are similar.

The figure 5 describes the behavior of the ring oscillator's frequency with MonteCarlo simulations with mismatch and process.

For these simulations, as the ratio between the length of the transistors and the minimal length of the technology is nearly 3 for the technology 0.8 µm, 5 for the technology 0.35 µm and 8 for the technology 0.12 µm, we expect that the robustness of the design increases with the technologies.

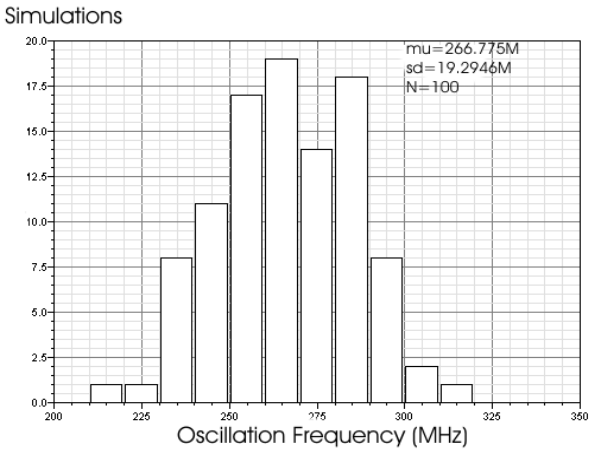

Figure 5. MonteCarlo simulation of the oscillation frequency of the ring oscillator in technology 0.8 µm with 5 V

The oscillation frequency mean-value and the standard deviation are maintained during the technology migration. For 0.8 µm 5 V, 0.35 µm 3.3 V and 0.12 µm 1.2 V, all of the simulated frequencies are included between 96 and 104 % of the initial value.

Then the robustness of this design is also conserved by this resizing methodology. And we notice that the robustness is better in technology 0.12 µm and 0.35 µm than 0.8 µm because of the ratio between transistor's length and minimal length of the technology.

Simulation results (Table VII) describe that the methodology keeps the figure of merit we want to maintain (oscillation frequency) except for the 0.12 µm technology where the optimization tool is needed. And we notice that the robustness of the design with the MonteCarlo simulations (figure 5) is conserved. Furthermore the cost with the decrease of area (7 % between 0.8 µm and 0.35 µm, 64 % between 0.35 µm and 0.25 µm and 42 % between 0.25 µm and 0.12 µm) is reduced. Then this methodology improves the three main performance criteria: area, power and speed.

We notice that for the technology 0.12 µm the methodology reaches its limits and the performances are kept with the help of the optimization tool.

THE WORK PRESENTED HERE defines a resizing methodology for analog circuit design reuse. The goal is to obtain a scaled circuit with the same performances of the initial one and to reduce area. It was applied to a linear circuit (OTA) to compare with others resizing works and on a non-linear circuit (ring oscillator) to extend the methodology. The different topologies are designed in a 0.8 µm, 5 V voltage supply standard CMOS technology and they were scaled down to a 0.12 µm, 1.2 V. This methodology decomposes the resizing process into three steps. This work clearly highlights which parameters are deduced from technological information and which ones are determined thanks to different strategic decisions.

Calculation and simulations were checked against the original design. The results of this technological migration

support the success of this redesign technique: conservation of the performances and reduction of the area. The limits and the extension of this methodology are described. The methodology could be improved by using BSIM3V3 model for the ultimate calculation step.

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